AEMB 32-bit Microprocessor Core Datasheet

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1 Introduction

The AEMB is a clean room implementation of the EDK3.2 software compatible Microblaze core using information from the Internet. It is cycle and instruction compatible to the MB for most software commands. It is not meant as a drop in replacement for the Microblaze as it is not architecturally compatible. It uses the WISHBONE bus instead of OPB.

This is a CPU core that is capable of moving and manipulating data to and from memory. It does not have any peripherals nor interrupt controllers although support for both external interrupts and breaks are provided. Any peripherals and their respective registers should be mapped to the data memory space. It has a separate instruction and data bus.

This core is fairly similar to the original from the point of view of software. Therefore, this list of features are mainly for the benefit of people unfamiliar with the original Some of the main features are:

1. Harvard architecture with a separate 32-bit instruction and data busses. The address space for each bus can be separately configured with core parameters.
2. Pipelined operation with a 3-stage integer pipeline. The pipeline is capable of executing one instruction per clock. This short pipeline allows it to context switch quickly.
3. Small core size with an excellent performance. It has an equivalent gate count of about 33k gates at 72 MHz in a Xilinx Spartan3 FPGA.
4. Mature software development toolchain as it is software compatible with the original. Operating system support for the original core includes uClinux.

2 External Signals

The core uses a WISHBONE compatible bus for it's on-chip bus. This allows the core to be quickly integrated with many other devices that use this bus. It supports the main legacy bus signals. In addition to this, it also uses some other signals that are described below.

2.1 Ports

The core ports are broken into three groups: Instruction Bus, Data Bus and System signals. They are all listed in table 2.1 with short descriptions. All the signals are active high except for the SYS_RST_I signal.

The signal functions should all be quite self explanatory. For detailed cycle arbitration and timings, please refer to the official WISHBONE specifications. Some of the WISHBONE signals are missing as they may not be necessary like the write-enable signal for the instruction bus.

NAME	SIZE	I/O	DESCRIPTION
IWB_ADR_O	32	Out	Instruction bus address
IWB_STB_O	1	Out	Instruction bus request/strobe
IWB_DAT_I	32	In	Instruction bus data word
IWB_ACK_I	1	In	Instruction bus acknowledge
DWB_ADR_O	32	Out	Data bus address
DWB_DAT_O	32	Out	Data bus data write word
DWB_STB_O	1	Out	Data bus request/strobe
DWB_WE_O	1	Out	Data bus write/read enable
DWB_DAT_I	32	In	Data bus data read word
DWB_ACK_I	1	In	Data bus acknowledge
SYS_INT_I	1	In	Positive edge triggered interrupt
SYS_EXC_I	1	In	Positive edge hardware exception
SYS_CLK_I	1	In	Master clock signal
SYS_RST_I	1	In	Master active low reset

Table 2.1: External signal names and descriptions.

3 Architecture Blocks

There are two top-level cores supplied. Either top-level designs can be used as a processor core. Alternatively, chip desigers may base their own top-level designs on these ones. The two cores are called AEMB_CORE and AEMB_UCORE. In fact, AEMB_UCORE integrates the AEMB_CORE as a sub-block.

The first top-level core has a separate instruction and data memory bus without cache memory. This can be used as part of an SoC with internal devices attached to the data memory bus. It is also the main top-level core as it contains all the functional sub-blocks.

The second top-level core has a unified instruction and data memory bus. This can be used as a stand alone microprocessor with external devices attached to the main system bus. It integrates a direct-mapped cache for faster execution. This is meant as an example of how the system core can be integrated in a wrapper. **!** → This top-level will unlikely be actively maintained.

4 Functional Operation

Although functionally similar to the Microblaze, the AEMB is not a drop-in substition. The AEMB can be used as an alternative core that can execute compatible code. This chapter documents some of the operation details of the core.

4.1 Reset Operation

The asynchronous, active low reset signal for the core is SYS_RST_I. During reset, all the internal registers for the core are set to their reset values. After reset, the processor begins to fetch instructions from memory location 0x00000000.

4.2 Pipeline Operation

The integer pipeline for the AEMB is a single issue and in-order execution pipeline. It consists of three main stages: *FETCH*, *DECODE* and *EXECUTE*. Each stage is also broken into two substages that run on different clock edges.

Stalls The pipeline is stalled for *any* incomplete memory operation. This means that, unless the memory is fast enough, the processor will stall the entire pipeline. This includes both instruction and data memory access. During a branch it is possible for the AEMB to use a branch delay slot.

4.3 Interrupt Operation

! → Current implementation of the interrupt is non clean. It can introduce a potential control hazard if any branch/imm instruction is in the pipeline.

5 Software & Simulation

The AEMB core is capable of executing C code compiled with the Microblaze GCC toolchain. Development of the core was simulated using GPLCVER 2.11a and Icarus Verilog 0.8.2 simulators. Simulatio code was compiled with GCC 3.4.1 (Xilinx EDK 8.1 Build EDK_I.17 090206). However, since the core does not implement certain instructions, certain compilation flags should be used.

```
$ mb-gcc -g -mxl-soft-div -mxl-soft-mul -msoft-float
```

An example compilation script is provided in the */sw/gccrom* shell script. This script takes any optional GCC arguments including the C filename. It will generate a suitable simulation ROM and place it in the */sim/aeMB.rom* file. The */sw/c/aeMB_testbench.c* file shows an example C algorithm to calculate Fibonnaci numbers.

```
$ ./gccrom c/aeMB_testbench.c
```

The */sim/verilog/testbench.v* verilog file is an example simulation testbench. This simulation will load and run the software that is located in the rom file. It is highly tailored to run tests based on the example testbench C code. The */sim/cversim* and */sim/iversim* are scripts to run the simulation with either CVER or Icarus verilog. These scripts take the programme arguments as well as the simulation testbench file to use.

```
$ ./cversim verilog/testbench.v
```

! → All these files are provided as examples and should be used as a baseline. For user applications, custom C software and testbench code should be written, which can be based on these files and scripts.

6 Implementation

! → These non-constrained synthesis results from Xilinx ISE v9.1i are for the core. These are not a benchmark but are useful as an estimate of chip resources and performance.

The core has been envisioned to be used as part of a larger SoC. Hence, it has been designed with a small size as an objective.

It is possible to further optimise the design as the critical path runs through the main ALU. About 44% of this critical path is due to routing, not logic.

```
Device utilization summary:
---------------------------

Selected Device : 3s400fg456-4

 Number of Slices:                      622  out of   3584    17%
 Number of Slice Flip Flops:            284  out of   7168     3%
 Number of 4 input LUTs:               1305  out of   7168    18%
    Number used as logic:               921
    Number used as RAMs:                384
 Number of IOs:                         169
 Number of bonded IOBs:                 167  out of    264    63%
 Number of GCLKs:                         1  out of      8    12%

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 13.877ns (Maximum Frequency: 72.062MHz)
   Minimum input arrival time before clock: 14.059ns
   Maximum output required time after clock: 8.406ns
   Maximum combinational path delay: No path found
```

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