AHB – WISHBONE BRIDGE

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Authors

TooMuch Semiconductor Solutions (info@toomuchsemi.com)

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1.0

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Introduction

The AHB-Wishbone bridge is an RTL implementation of a synthesisable bridge to interconnect AHB Master to Wishbone Slave.

Limitations of Design

- This design will not work for Sequential transfers (ie for wrap and incremental type of transfers).
- No error, retry and split cases have been considered in the design.
- Word size is 32 bits. It can be modified as per requirement.
- All transfers has been considered as non-sequential type.

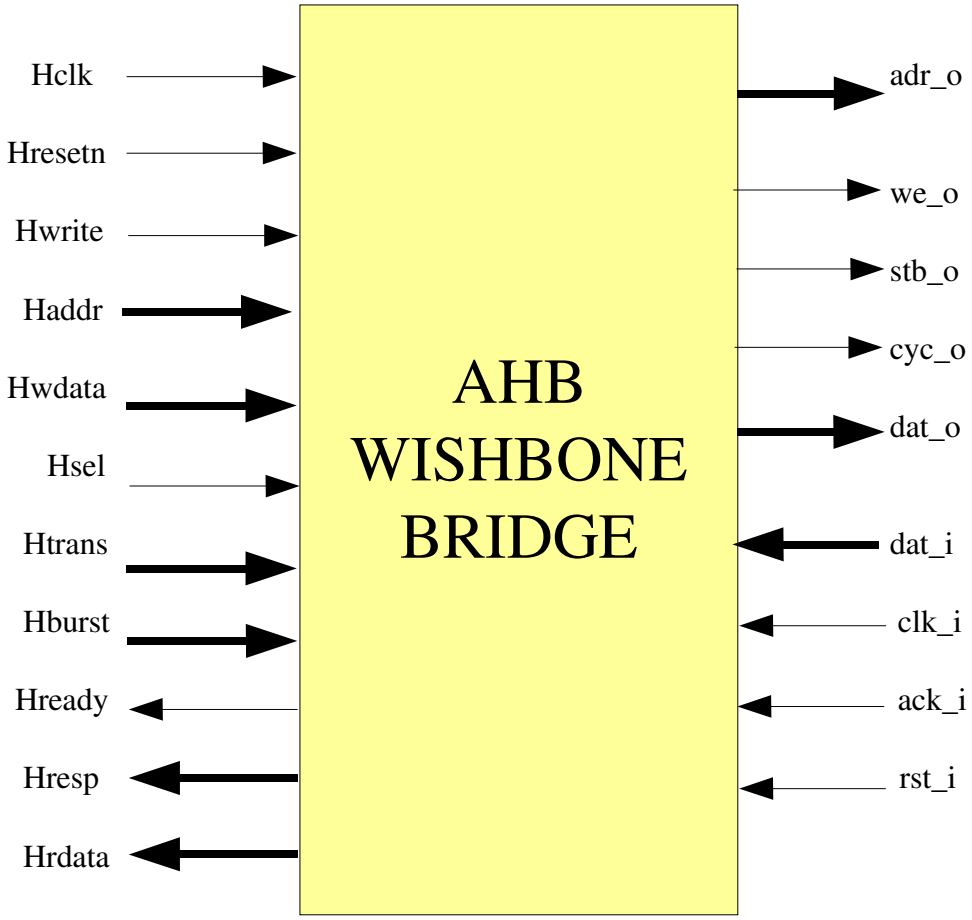
Synthesizability

This code is completely synthesizable. The only care that has to be taken is that the wishbone clock(clk_i) and reset(rst_i) signals have been left unconnnected inside the design. The whole design is working on AHB clock and reset signals that should be provided by AHB master.

Port Definitions

Port Name	*Direction*	*Size*	*Source*	*Description*
Hclk	in	1	AHB Master	Bus Clock
Hresetn	in	1	AHB Master	Active Low Sync. Reset
Hwdata	in	32	AHB Master	Write data bus
Hwrite	in	1	AHB Master	Read/Write enable
Hburst	in	3	AHB Master	Burst Type
Hsize	in	3	AHB Master	not used
Htrans	in	2	AHB Master	Transfer Type
Hsel	in	1	AHB Decoder	Slave select signal
Haddr	in	16	AHB Master	Address bus
dat_i	in	32	WB Slave	Data Bus
ack_i	in	1	WB Slave	To indicate current transfer status
clk_i	in	1	WB Slave	unconnected
rst_i	in	1	WB Slave	unconnected
adr_o	out	16	Bridge	Address bus
dat_o	out	32	Bridge	Data bus
cyc_o	out	1	Bridge	To indicate valid bus cycle
we_o	out	1	Bridge	Read/Write enable
stb_o	out	1	Bridge	To indicate valid data transfer cycle
Hrdata	out	32	Bridge	Read Data Bus
Hresp	out	2	Bridge	Response
Hready	out	1	Bridge	To indicate bridge is ready.

Block Representation



Reset operation

The AHB reset signal is active LOW and is used to reset the system and the bus. This reset has been asserted and deasserted synchronously after the rising edge of Hclk. The reset is required to be asserted atleast for one clock cycle (AHB Clock).

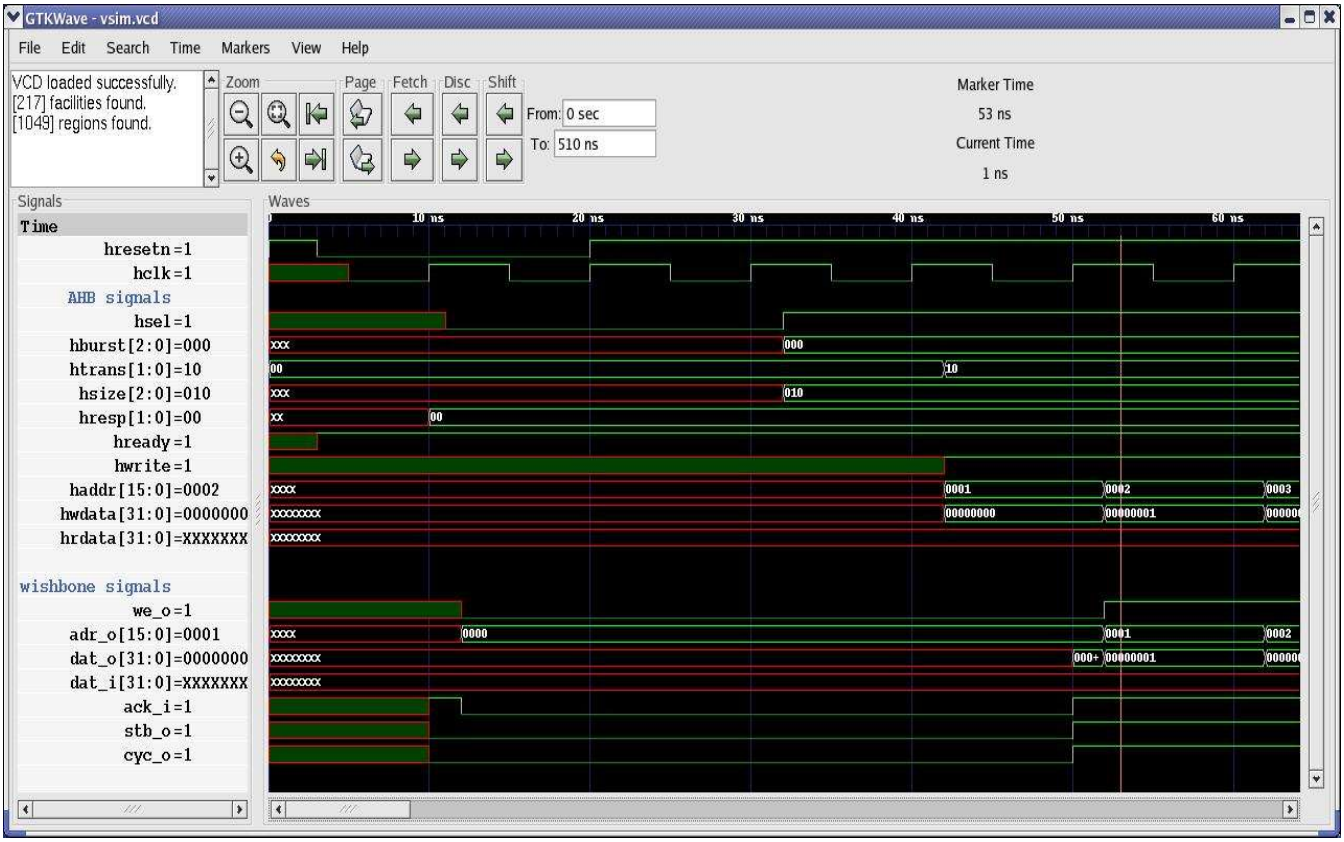


Fig. 1 : Reset operation

Write Cycle

When Hwrite is HIGH, this signal indicates a write transfer and the Master will broadcast data on the write data bus(Hwdata) when Hready signal is HIGH.

1) At 1st clock edge the address(A1) is sampled by the AHB Slave on Haddr
2) This address sampled is transfered synchronously to the wishbone Slave on adr_o.
3) Data(D1) for this address is sampled asynchronously by AHB Slave on Hwdata.
4) This data is written into the WISHBONE Slave asynchronously on dat_o bus.
5) At 2nd clock edge address(A2) for next transfer is sampled by AHB Slave on Haddr.
6) At 2nd clock edge address(A1) and data (D1) is sampled by WISHBONE Slave on adr_o and dat_o bus respectively.
7) At 2nd clock edge ack_i is also asserted.

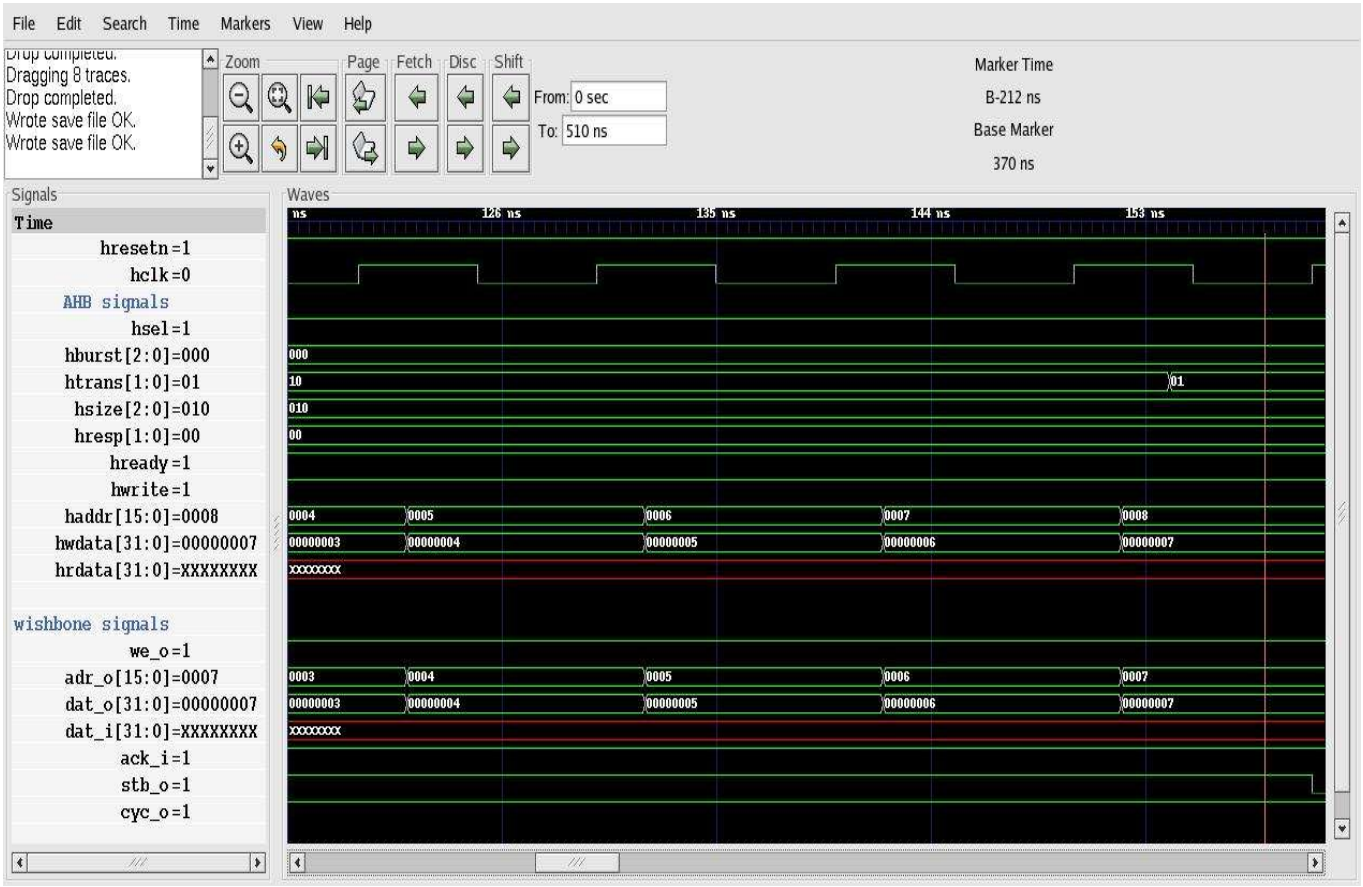


Fig 2 : Write Cycle

Read Cycle

When Hwrite is LOW, this signal indicates a read transfer and the Master will receive data on the read data bus (Hrdata) provided the Hready signal is HIGH.

1) At 1st clock edge the address(A1) is sampled by the AHB Slave on Haddr.
2) This address will be transfered synchronously to WISHBONE Slave on adr_o.
3) Data(D1) for this address is sampled asynchronously by WISHBONE Master on dat_i.
4) This data is transfered asynchronously to AHB Master on Hrdata.
5) This data (D1) is sampled by AHB Master on 2nd clock edge.
6) At 2nd clock edge address(A2) for next transfer is sampled by AHB Slave on Haddr.
7) At 2nd clock edge ack_i is asserted.

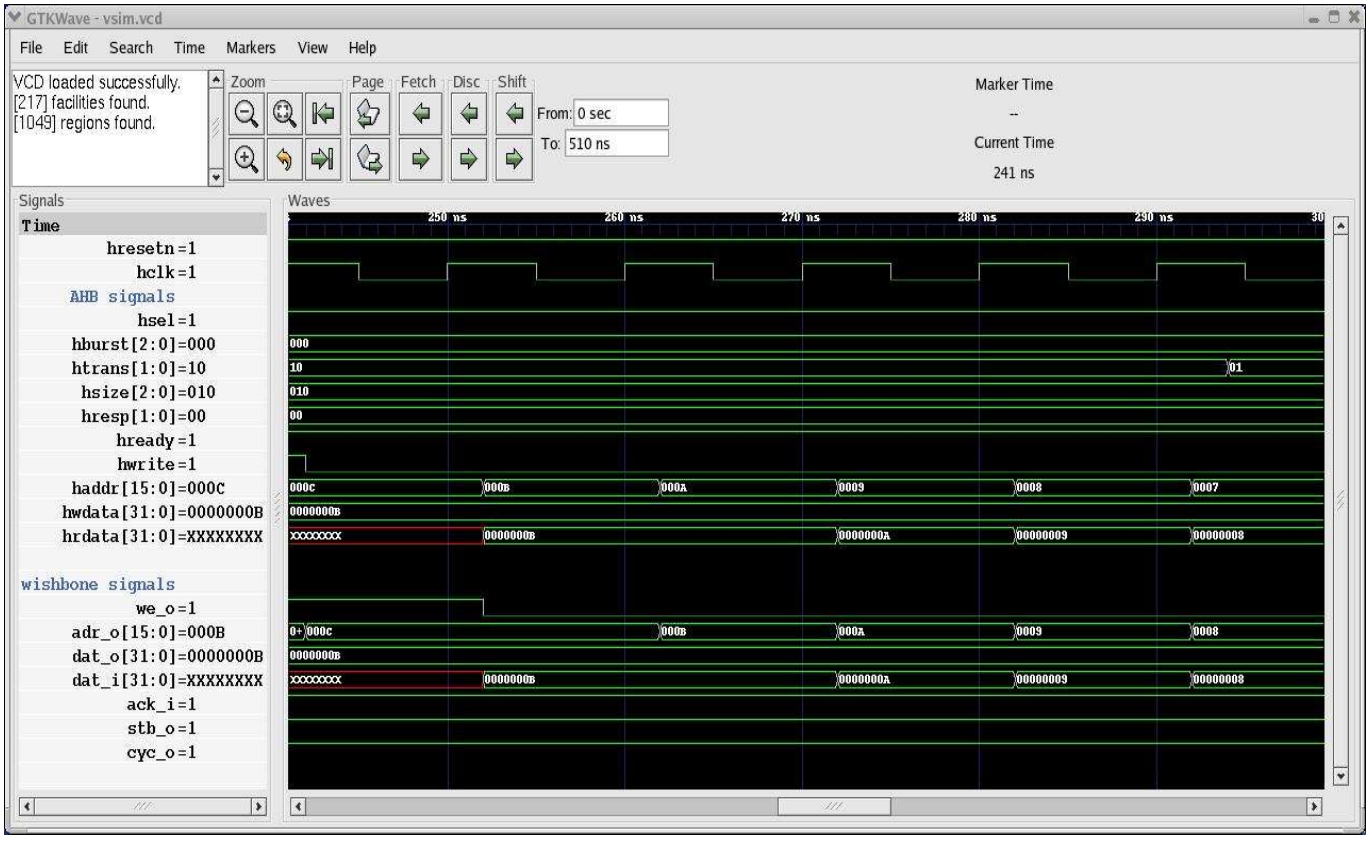


Fig. 3 : Read Cycle

Write with Wait states

Inserted by Wishbone Slave

1) At 1st clock edge the address(A1) is sampled by the AHB Slave on Haddr
2) This address sampled is transfered synchronously to the wishbone Slave on adr_o.
3) Data(D1) for this address is taken asynchronously by AHB Slave after 1st clock edge on Hwdata.
4) This data is latched asynchronously on dat_o bus.
5) Address (A2) is sampled at 2nd clock edge.
6) Ack_i signal is pulled LOW by the wishbone Slave after 2nd clock edge.
7) Hready signal is pulled down asynchronously, to indicate that the AHB Slave and hence wishbone Slave is not ready to complete its current transfer.
8) Address(A3) at next rising clock edge is sampled by AHB Slave when ack_i and hence Hready is asserted again.
9) Data (D2) is latched on dat_o bus when Hready is asserted.

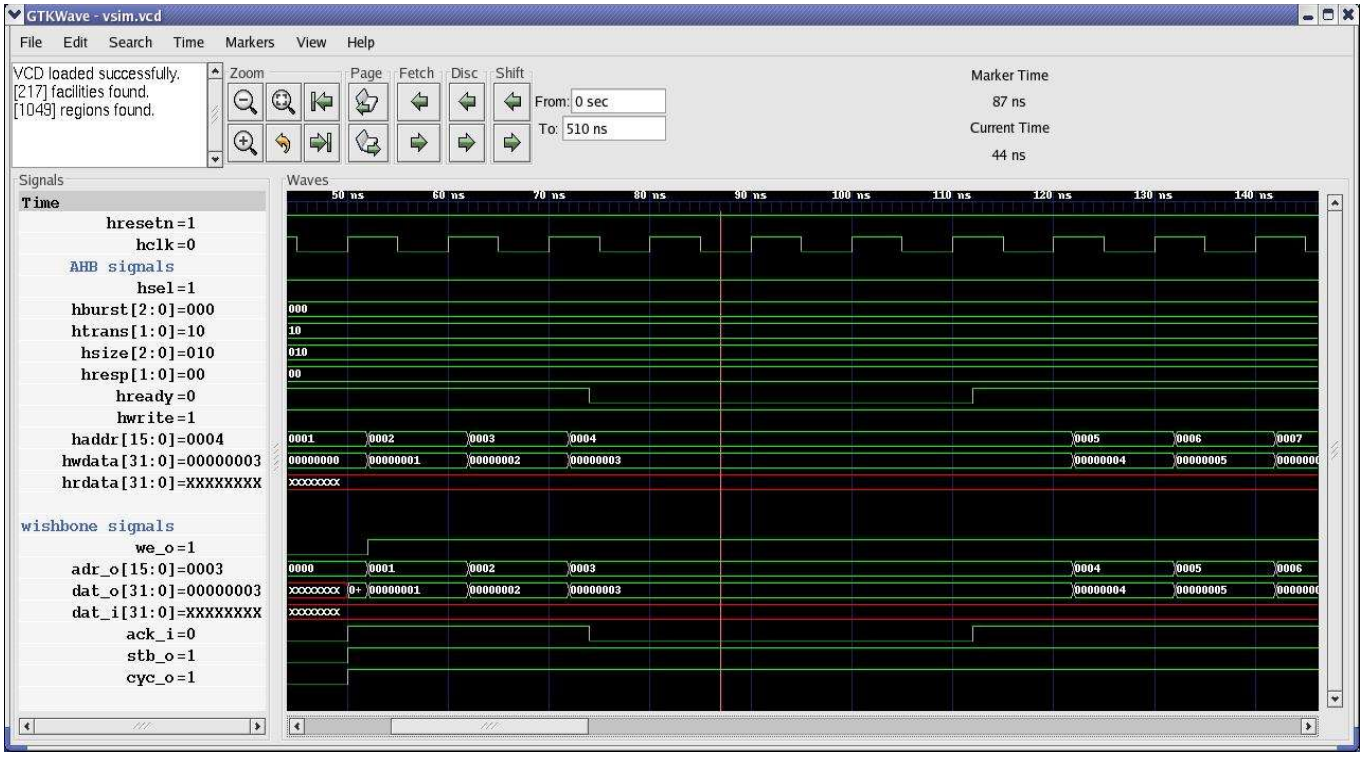


Fig. 4 : Write cycle with wait state inserted by wishbone Slave

Inserted by AHB Master

This is when AHB Master is busy, so that it can not continue its next bus transfer operation.

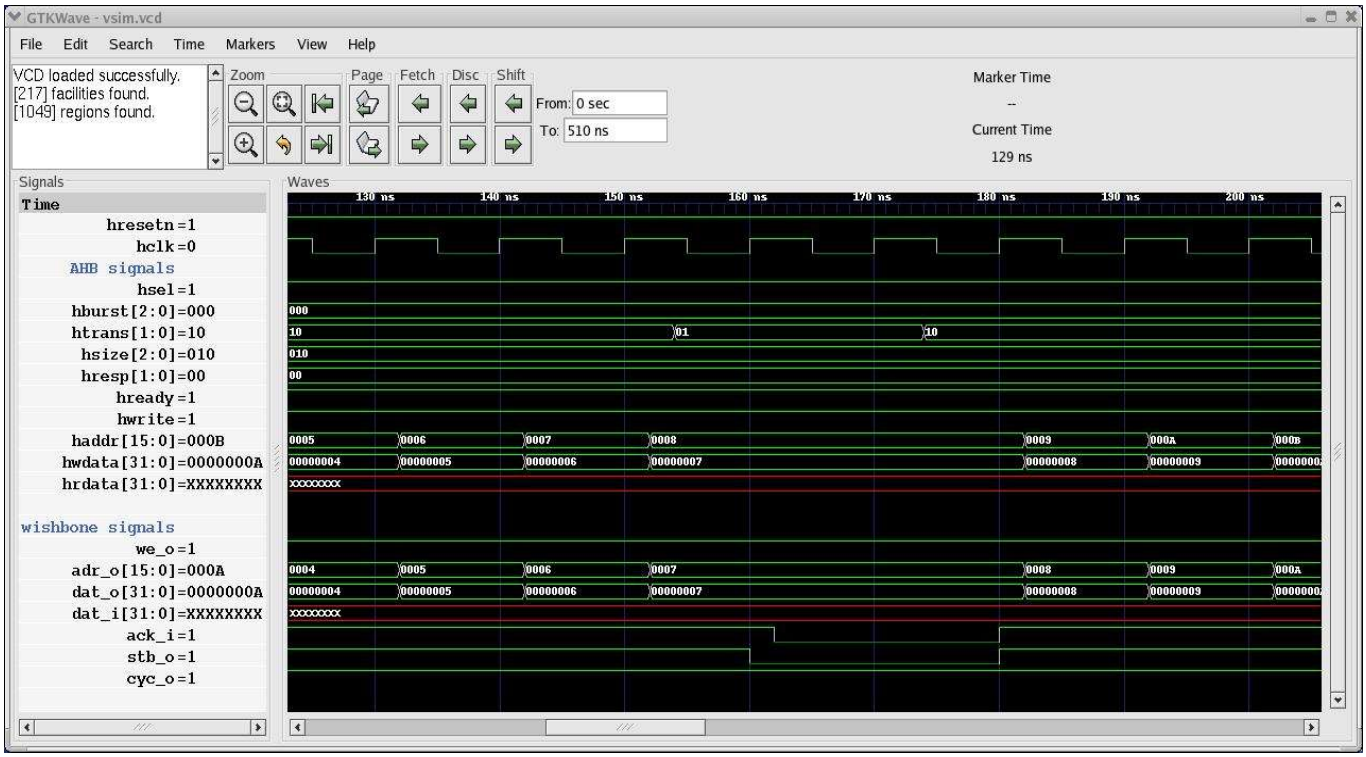


Fig. 5 : Write Cycle with wait state inserted by AHB Master

1) At 1st clock edge the address(A1) is sampled by the AHB Slave on Haddr
2) This address sampled is transfered synchronously to the wishbone Slave on adr_o.
3) Data(D1) for this address is taken asynchronously by AHB Slave after 1st clock edge on Hwdata.
4) This data is latched asynchronously on dat_o bus.
5) Address (A2) is sampled at 2nd clock edge.
6) Assert Htrans to “busy(01)” after 1st clock edge.
7) At 2nd clock edge the bridge will sample the Htrans signal.
8) Deassert “stb_o” signal synchronously.
9) Ack_i signal will also be deasserted asynchronously by Wishbone Slave in response to stb_o signal.
10) Htrans is asserted to “Non – Seq (10)” transfer type at clock edge after clock edge 4
11) At 4th clock edge the bridge will sample the Htrans signal.

12) Stb_o is asserted synchronously at clock edge 4

13) Ack_i is asserted asynchronously with response to stb_o.

14) Data (D2) is latched asynchronously on dat_o bus .

15) Address(A3) at 5^{th} clock edge is sampled by AHB Slave

Read with wait states

Inserted by Wishbone Slave

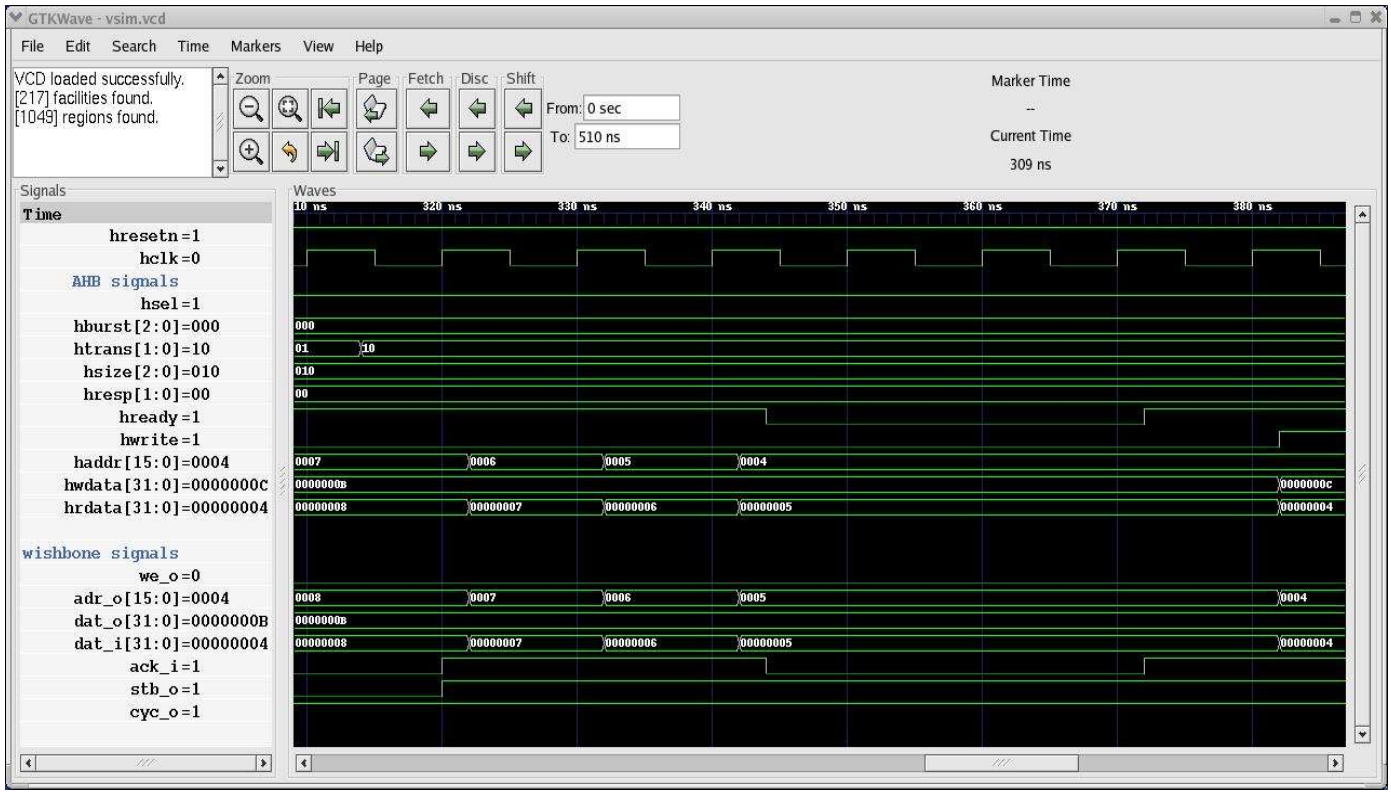


Fig. 6 : Read cycle with wait state inserted by wishbone Slave

1) At 1st clock edge the address(A1) is sampled by the AHB Slave on Haddr
2) This address sampled is transfered synchronously to the wishbone Slave on adr_o.
3) Data(D1) for this address is latched asynchronously by wishbone Slave after 1st clock edge on dat_i.
4) This data is latched asynchronously on Hrdata bus.
5) Address (A2) is sampled at 2nd clock edge.
6) Ack_i signal is pulled LOW by the wishbone Slave after 2nd clock edge.
7) Hready signal is pulled down asynchronously, to indicate that the AHB Slave and hence wishbone Slave is not ready to complete its current transfer.
8) Address(A3) at next rising clock edge (6th) is sampled by AHB Slave when ack_i and hence Hready is asserted again.
9) Data (D2) is latched on dat_i bus asynchronously when Hready is asserted.
10) Data (D2) is latched on Hrdata asynchronously at the same time.

Inserted by AHB Master

This is when AHB Master is busy, so that it can not continue its next bus transfer operation.

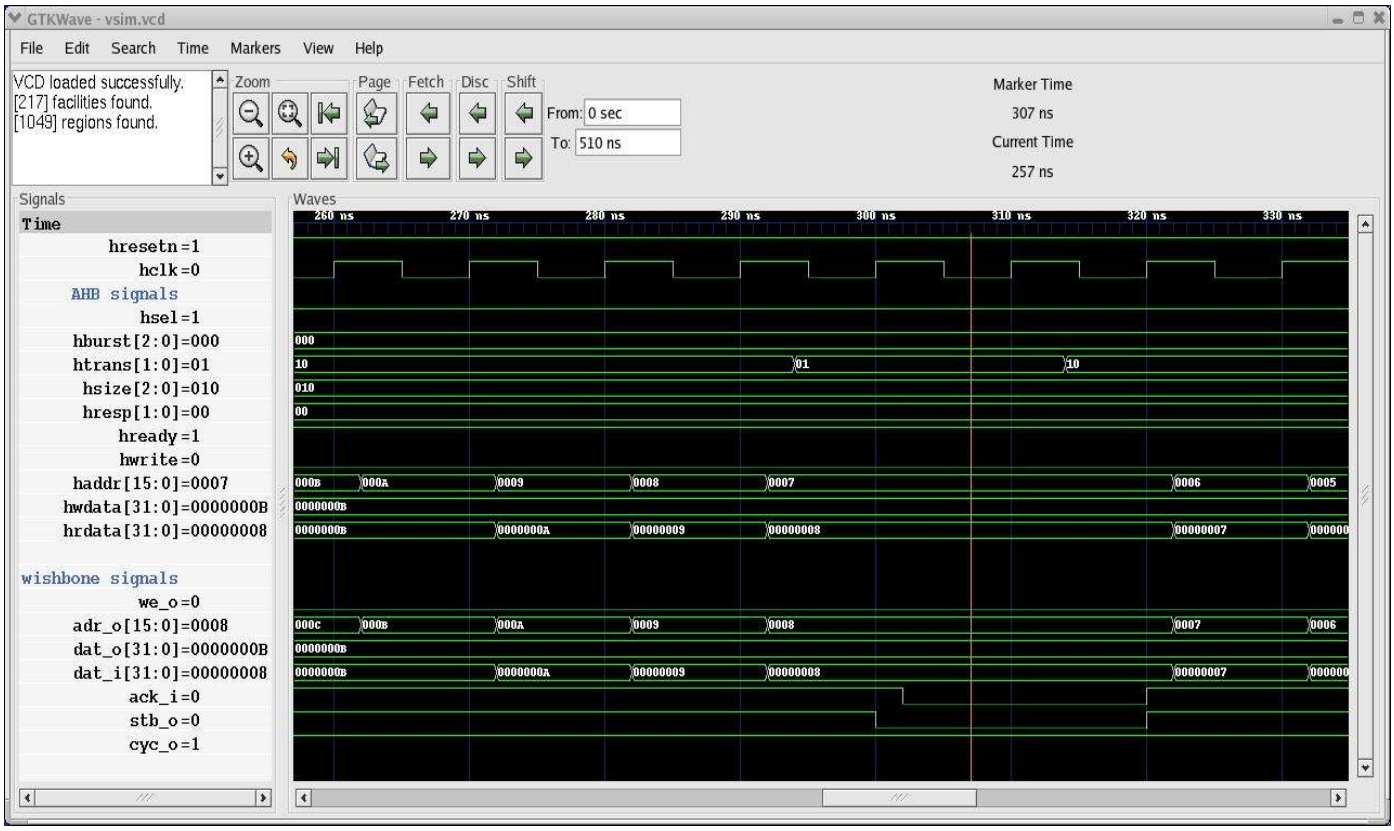


Fig. 7: Read cycle with wait state inserted by AHB Master

1) At 1st clock edge the address(A1) is sampled by the AHB Slave on Haddr
2) This address sampled is transfered synchronously to the wishbone Slave on adr_o.
3) Data(D1) for this address is latched asynchronously by wishbone Slave after 1st clock edge on dat_i.
4) This data is latched asynchronously on Hrdata bus.
5) Address (A2) is sampled at 2nd clock edge.
6) Assert Htrans to "busy(01)" after 1st clock edge.
7) At 2nd clock edge the bridge will sample the Htrans signal.
8) Deassert "stb_o" signal synchronously.
9) Ack_i signal will also be deasserted asynchronously by Wishbone Slave in response to stb_o signal.
10) Htrans is asserted to "Non – Seq (10)" transfer type at clock edge after clock edge 4

11) At 4th clock edge the bridge will sample the Htrans signal.

12)] Stb_o is asserted synchronously at clock edge 4

13) Ack_i is asserted asynchronously in response to stb_o.

14) Address(A3) at 5th clock edge is sampled by AHB Slave

15) Data (D2) is latched asynchronously on dat_i bus

16) Data (D2) is latched asynchronously at the same time on Hrdata bus.

Read after Write

1) At 1st clock edge the address(A1) is sampled by the AHB Slave on Haddr along with Hwrite signal and other control signals.
2) This address sampled is transfered synchronously to the wishbone Slave on adr_o.
3) Data(D1) for this address is sampled asynchronously by AHB Slave on Hwdata.
4) Hwrite signal is pulled down to LOW (for read operation) after clock edge 1.
5) Data(D1) is latched into the WISHBONE Slave asynchronously on dat_o bus.
6) At 2nd clock edge address(A2) for next transfer is sampled by AHB Slave on Haddr along with Hwrite signal and is latched synchronously on adr_o bus.
7) we_o signal is pulled LOW synchronously at 2nd clock edge.
8) At 2nd clock edge address(A1) and data (D1) is sampled by WISHBONE Slave on adr_o and dat_o bus respectively.
9) Wishbone Slave will latch data(D2) for address (A2) asynchronously on dat_i bus
10) Bridge will latch data(D2) asynchronously on Hrdata at the same time.

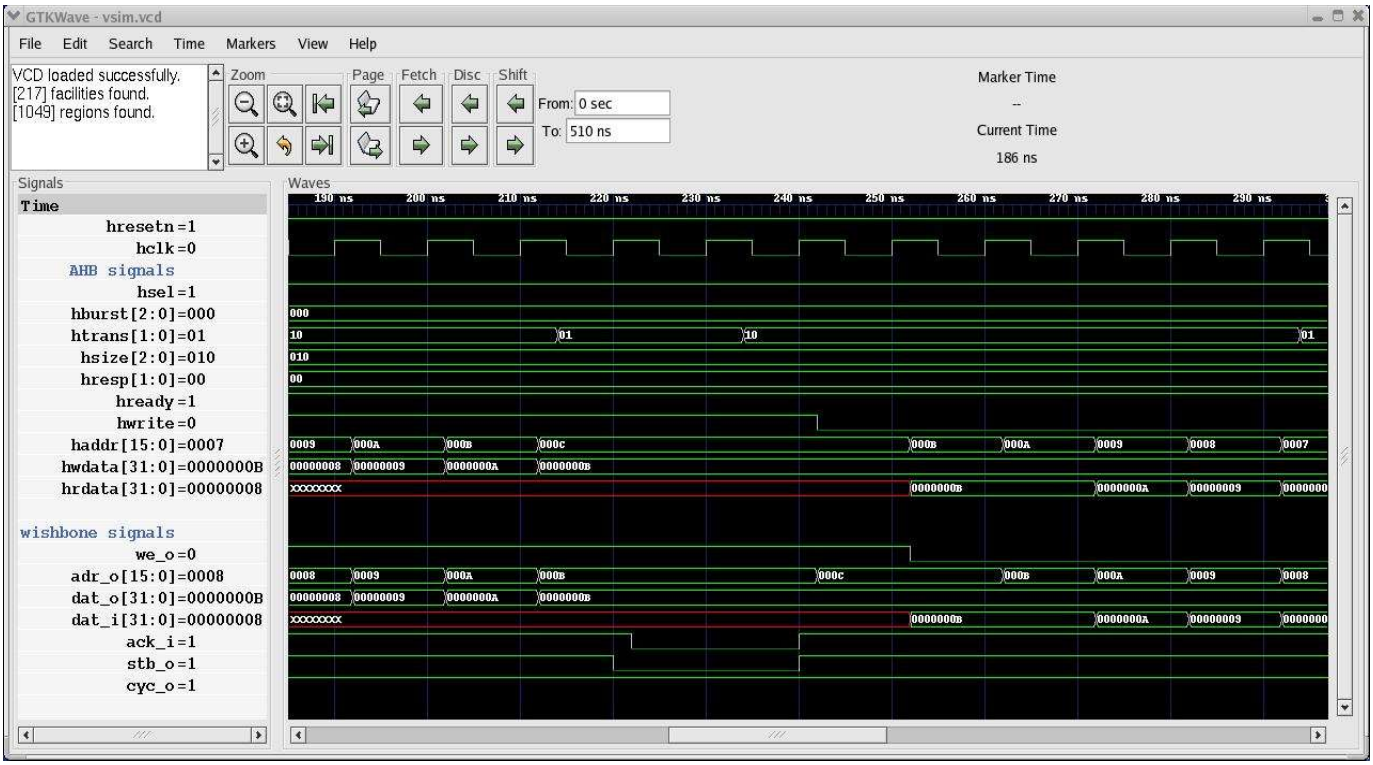


Fig. 8: Read after write cycle with wait state inserted by AHB Master during write operation

Write after Read

1) At 1st clock edge the address(A1) is sampled by the AHB Slave on Haddr .
2) This address will be transfered synchronously to WISHBONE Slave on adr_o.
3) Data(D1) for this address is sampled asynchronously by WISHBONE Master on dat_i.
4) D1 is transfered asynchronously to AHB Master on Hrdata
5) Hwrite signal is pulled to HIGH logic(for write operation) after 1st rising edge of clock.
6) Hwrite logic is transfered synchronously on we_o port.
7) At 2nd clock edge address(A2) is sampled by AHB Slave along with Hwrite signal.
8) A2 is transfered synchronously from Haddr to adr_o.
9) Bridge transfers data (D2) asynchronously after 2nd clock edge from Hwdata to dat_o.

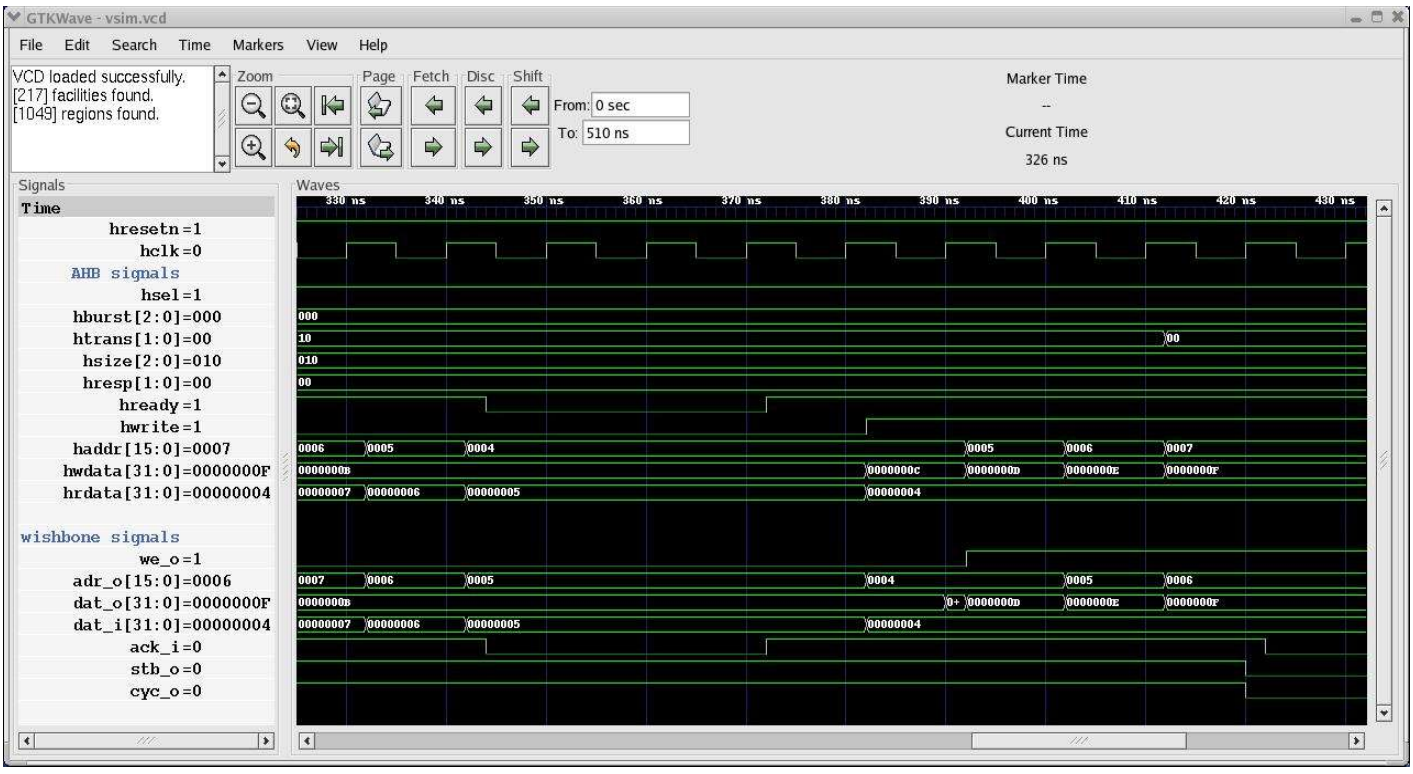


Fig. 9: Write after Read cycle with wait state inserted by wishbone Slave during read operation