# AMBA AHB ARBITER

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## Revision No.

1.0

## Disclaimer

## Introduction

This ARBITER is AMBA AHB complaint. It is designed for generic number of Masters. The priority of the master increments from 8 to 0 (number of master are taken as 9 and can be changed by changing the value of parameter “size”) . The default bus grant goes to master with lowest priority. The address and data bus are taken as 8 bit wide. The **burst** supported by arbiter are Single, Inc, Inc4, Wrap4, Inc8, Wrap8, Inc16 and Wrap16. The transfer type supported by arbiter are Sequential, Non-Sequential, Idle and Busy.

## Limitations of Design

- No error, retry and split cases have been considered in the design.
- Word size is 8 bits. It can be modified as per requirement.
- The change over of the master requires 1 clock cycle.

## Synthesizability

This code is completely synthesizable in Xilinx 6.3 i .

## Port Definitions

| *Port Name* | *Direction* | *Size* | *Source* |
|---|---|---|---|
| haddr | in | 8 | AHB Master |
| htrans | in | 2 | AHB Master |
| hwrite | out | 1 | AHB Master (not supported ) |
| hsize | out | 3 | AHB Master (not supported) |
| hburst | in | 3 | AHB Master |
| hwdata | out | 8 | AHB Master |
| hrdata | out | 32 | AHB Master (not supported) |
| hready | in | 1 | AHB Slave |
| hresp | in | 2 | AHB Slave (not supported) |
| hgrant | out | 4 | Arbiter output |
| data_out | out | 8 | Arbiter output |
| addr_out | out | 8 | Arbiter Output |
| hburst_out | out | 3 | Arbiter Output |
| htrans_out | out | 2 | Arbiter Output |
| hmaster | out | 4 | Arbiter Output |
| hmaster_lock | out | 1 | Arbiter Output |
| hclk | in | 1 | AHB Master |
| hresetn | in | 1 | AHB Master |

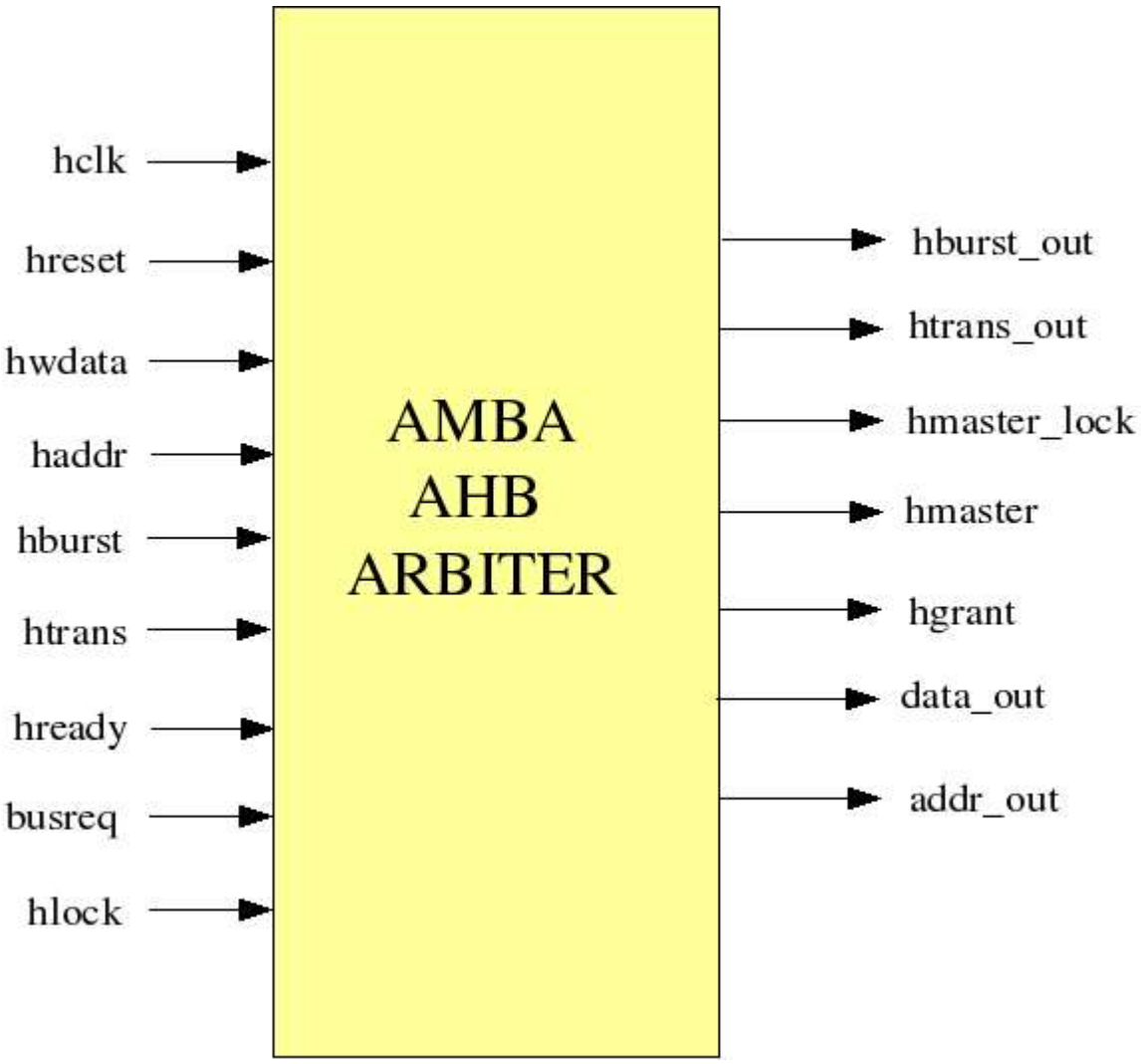


**Fig 1: Black Box**

**Representing Arbiter inputs and outputs**

## Reset operation

The WISHBONE Reset signal is active Low and is used to reset the system and bus. This reset has been asserted and deasserted synchronously after the rising edge of Clock.

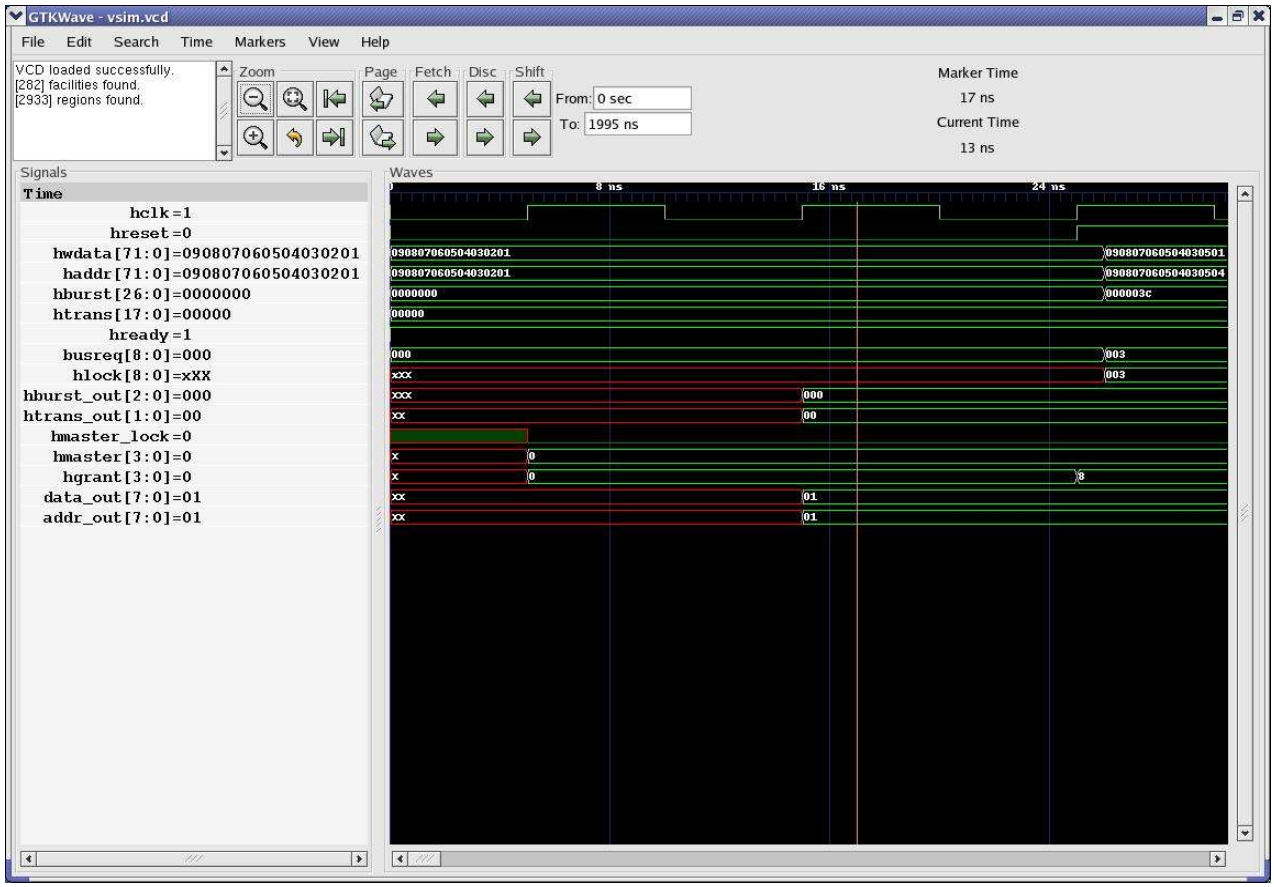


**Fig 2 : Reset Operation**

## Default Master

The default master is the master with the lowest priority so when ever there will not be any request for the bus, from any of the master, then by default the bus will be granted to the the master with the lowest priority.

In fig 3 , at the first positive clock edge as the busreq & hlock signal are low and no locked transfer is going on so the bus is granted to the master 8 as it is the default master.

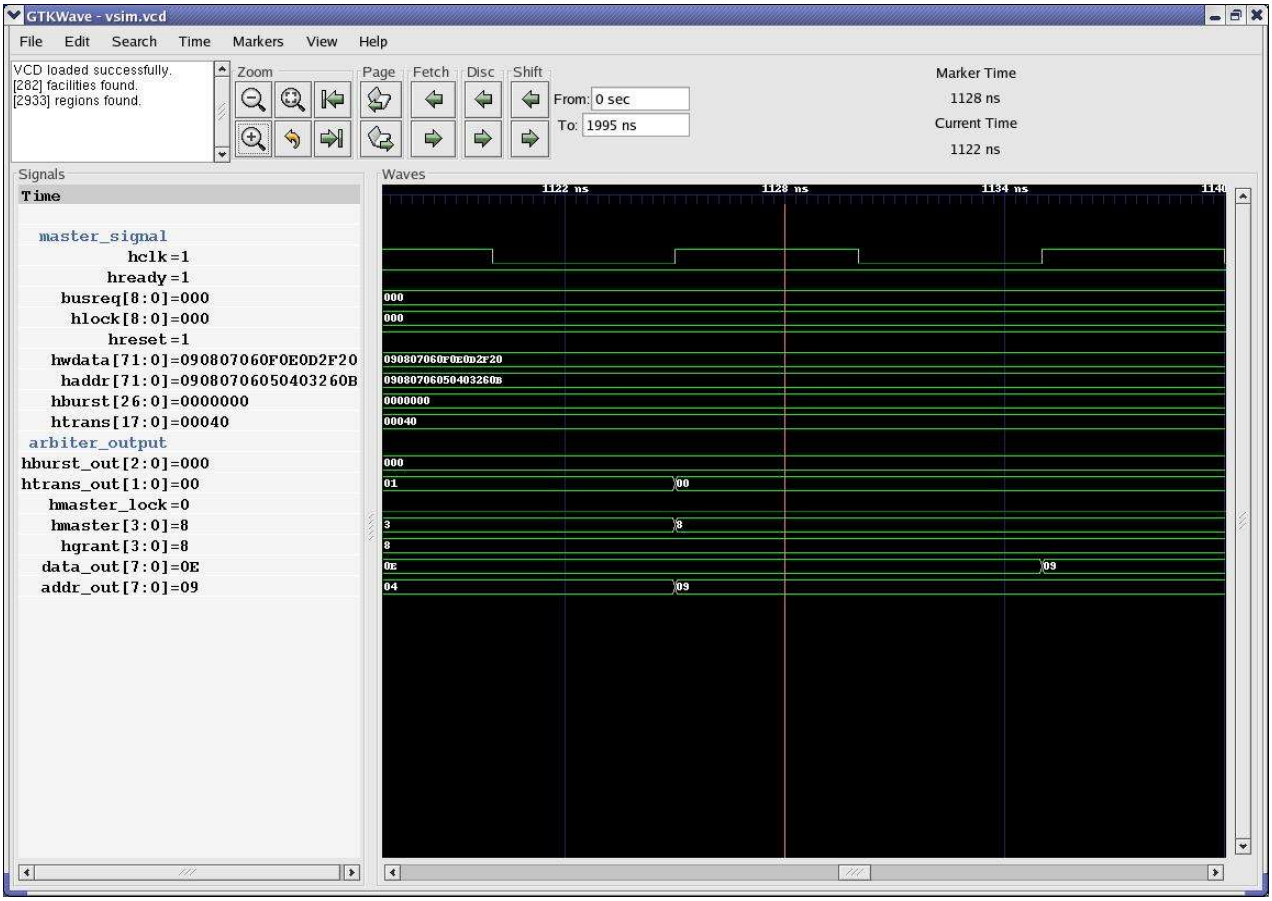


**Fig 3 : Default Master**

## Master switchover

If the Master which is currently granted the bus has completed the transfer and its corresponding lock signal is low, then the bus is granted to master of the highest priority, among the master which are requesting for the bus.

In Fig 4, the master 0 was currently granted the  bus, but as at the first positive edge of clock the hmaster signal is going low and at the same time the master 1 is requesting for the bus, the bus is granted to the master 1.

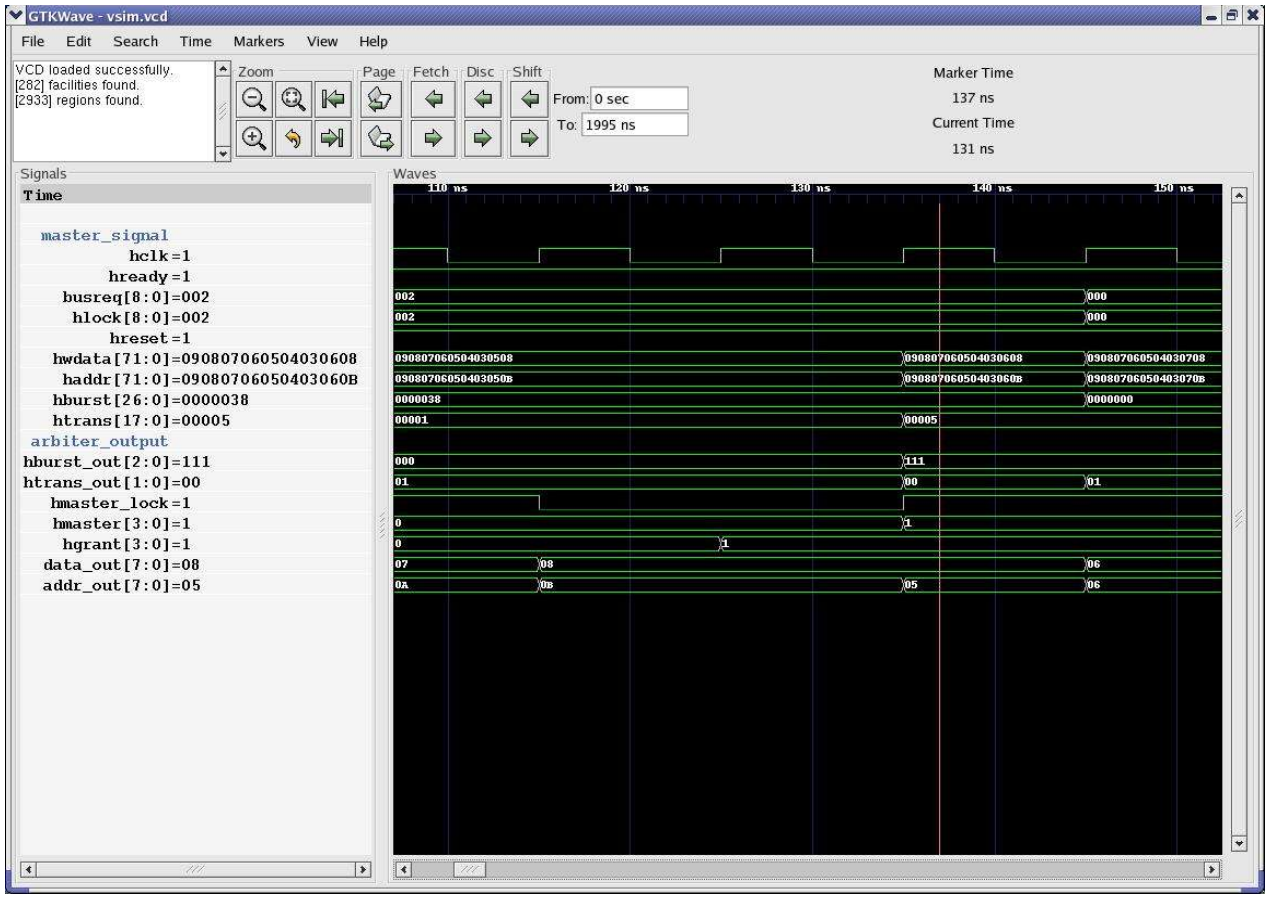


**Fig 4 :Master Switch Over**

## Clock Delay in Master Switchover

If the master switch over is going on, after locked transfer ,this release of our design takes a delay of the 1 cycle to give the control of the bus from current master to next master.

In Fig 5, at the third positive edge of clock the address phase of the first master is over. But this version of design will take a delay of 1 clock cycle, to start the address phase of the next master. So the address phase of the next master will start at the 5$^{th}$ clock edge.

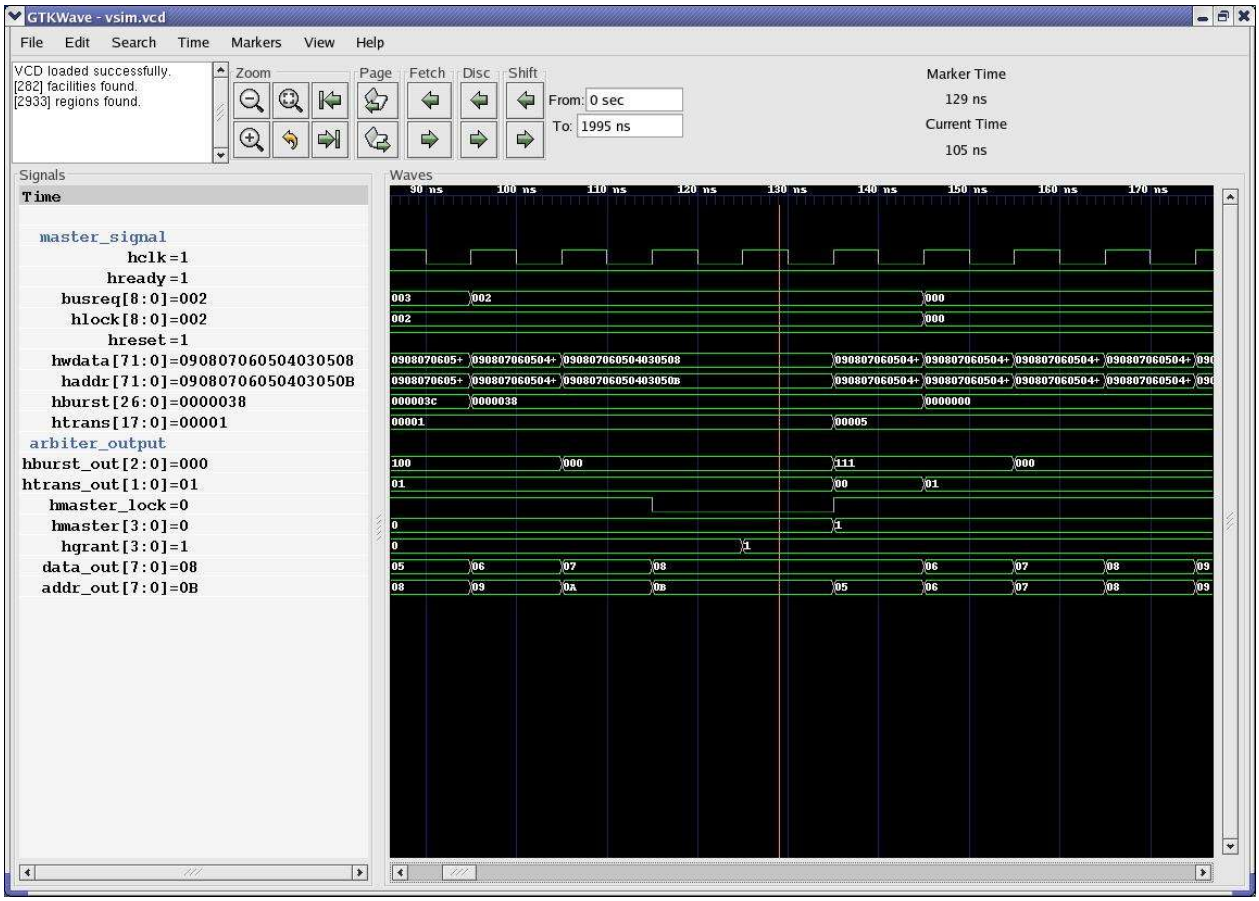


**Fig 5 :Clock Delay in Master Switch Over**

## Wrap Cycle With Wait State and Idle State

This version of the design supports  wait and idle state. For both wait and idle state the data is not sampled by the slave.

In fig 6, at 4th and 5th positive clock edge the idle signal comes and hence no address or data phase occurs in these two cycles and on the 6th positive clock edge the address and the data phase of the master starts as htrans is now sequential.

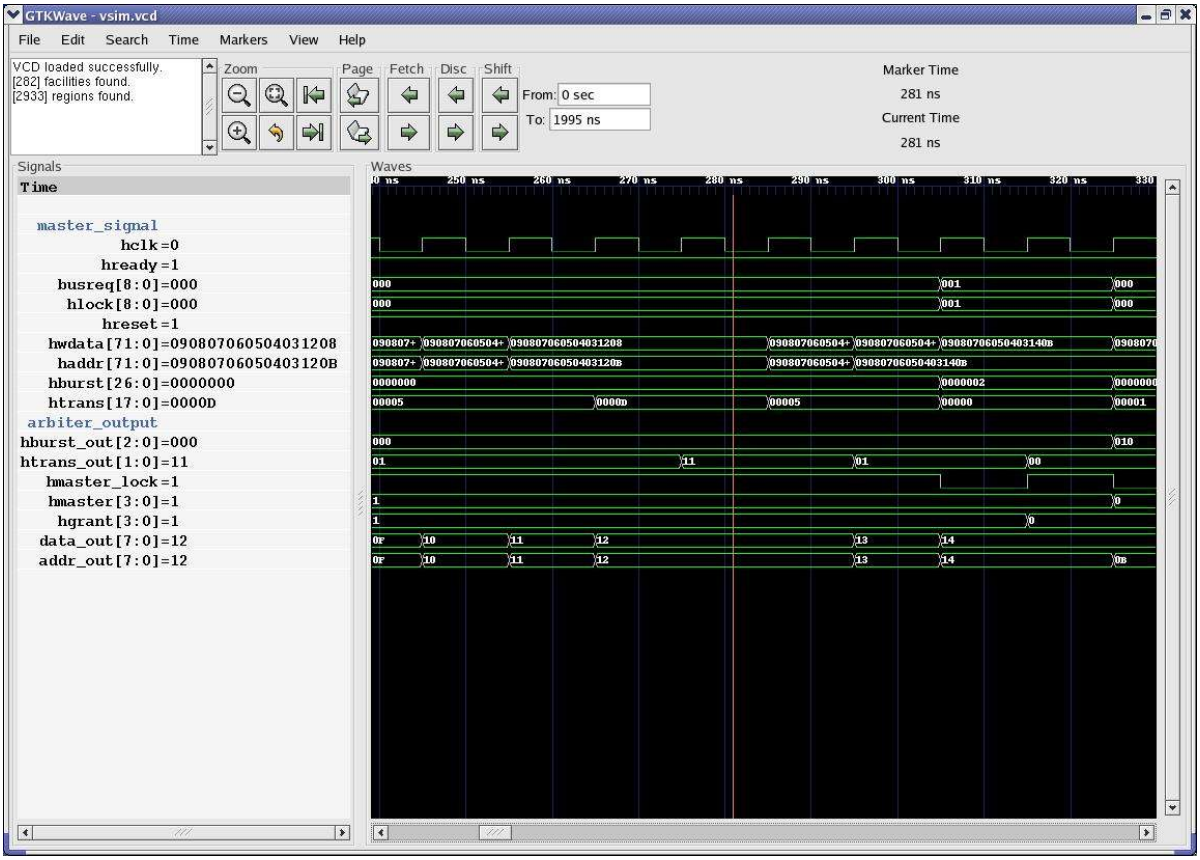


**Fig 6 : Wait State While Burst**

## General Doubts Related to AHB Specification

Under written are the doubts which designers have while making AMBA AHB Design.

1. As per AMBA AHB specification Master switch over should be done in zero cycle delay and hence the next slave should always be ready for the next master's address cycle.

2. An AHB slave must have the Hready signal both as input and output. Hready is required as an output from a slave so that the slave can extend the data phase of a transfer. Hready is also required as an input so that the slave can determine when the previously selected slave has completed its final transfer and the first data phase transfer for this slave is about to commence.

## References


1. http://www.arm.com AMBA Specification (Rev. 2.0)
2. http://www.arm.com/support/AMBA.html