

AltRISC Business Case

The typical RISC processor, such as MIPS or RISC-V has 32 32-bit registers and an instruction with three register fields. And relatively low code density. Three five bit register fields is 15-bits. That and an 8-bit op-code make for 23 bits. Why not have a 24-bit instruction thereby increasing the code density to typical levels? Cons are loss of word alignment of instructions and loss of 16-bit immediates.

Author's preference is to provide variable length immediates. And prefix instructions as a means to support additional op-codes and additional register fields (useful for multi-media instructions).

A further issue is that RISC is a poor abbreviation: A better choice is ROIS (Register Oriented Instruction Set), meaning that most instructions are register to register rather than MOIS (Memory Oriented Instruction Set, as in historical accumulator machines) or MROIS (Memory-Register Oriented Instruction Set, as in X86)