alt_MSP430-24_16 James Brakefield 2020 `iiiiiidddmmssss`

instruction				inst read cycle			immediate read cycle					
memonic	binary opcode	mode	binary	mem read	reg write	mem write	mem read	reg write	mem write	PC update	CCR update	comment
BCC		PC+2	0xx000xxddddddddd							PC+2		conditional branch, branch not taken
BCC		PC+d	0xx000xxddddddddd							PC+signed delta		conditional branch, branch taken
Register to register operations												s bits less than 1100
LDB	000001	RS	100dddd00ssss		0--0&Rs7-0					PC+2		zero extend low byte of Rs
LDHS	000010	RS	100dddd00ssss		0--0&Rs15-0					PC+2		sign extend low 16 bits of Rs
LDW	000011	RS	100dddd00ssss		Rs					PC+2		move Rs to Rd
DADB	000100	RS	100dddd00ssss		bcd(Rs+Rd)					PC+2	all	low byte decimal add Rs to Rd
LDI	000101	RI	100dddd00ssss		neg 8 to +7					PC+2		remapped to load immediate of -8 to 7
LDI	000110	RI	100dddd00ssss		ssss+8/-16					PC+2		remapped to load immediate of 8-15 or neg 9-16
LDI	000111	RI	100dddd00ssss		ssss+16/-24					PC+2		remapped to load immediate of 16-23 or neg 17-24
ORB	001001	RS	101dddd00ssss		0--0&Rs7-0 OR Rd					PC+2	not CV	OR low byte of Rs with Rd
ORH	001010	RS	101dddd00ssss		0--0&Rs15-0 OR Rd					PC+2	not CV	OR low half of Rs with Rd
ORW	001011	RS	101dddd00ssss		Rs OR Rd					PC+2	not CV	OR Rs with Rd
BITB	001100	RS	101dddd00ssss							PC+2	not CV	set CCR to AND(Rs, Rd)
ORI	001101	RI	101dddd00ssss		Rd OR neg 8 to +7					PC+2	not CV	remapped to OR of Rd and immediate of -8 to 7
ORI	001110	RI	101dddd00ssss		Rd OR ssss+8/-16					PC+2	not CV	remapped to OR of Rd and immediate of 8-15 or neg 9-16
ORI	001111	RI	101dddd00ssss		Rd OR ssss+16/-24					PC+2	not CV	remapped to OR of Rd and immediate of 16-23 or neg 17-24
XORB	010001	RS	110dddd00ssss		0--0&Rs7-0 XOR Rd					PC+2	not CV	XOR low byte of Rs with Rd
XORH	010010	RS	110dddd00ssss		0--0&Rs15-0 XOR Rd					PC+2	not CV	XOR low half of Rs with Rd
XORW	010011	RS	110dddd00ssss		Rs XOR Rd					PC+2	not CV	XOR Rs with Rd
BITH	010100	RS	110dddd00ssss							PC+2	not CV	set CCR to AND(Rs, Rd)
XORI	010101	RI	110dddd00ssss		Rd XOR neg 8 to +7					PC+2	not CV	remapped to XOR of Rd and immediate of -8 to 7
XORI	010110	RI	110dddd00ssss		Rd XOR ssss+8/-16					PC+2	not CV	remapped to XOR of Rd and immediate of 8-15 or neg 9-16
XORI	010111	RI	110dddd00ssss		Rd XOR ssss+16/-24					PC+2	not CV	remapped to XOR of Rd and immediate of 16-23 or neg 17-24
ANDB	011001	RS	111dddd00ssss		0--0&Rs7-0 XOR Rd					PC+2	not CV	XOR low byte of Rs with Rd
ANDH	011010	RS	111dddd00ssss		0--0&Rs15-0 XOR Rd					PC+2	not CV	XOR low half of Rs with Rd
ANDW	011011	RS	111dddd00ssss		Rs XOR Rd					PC+2	not CV	XOR Rs with Rd
BITW	011100	RS	111dddd00ssss							PC+2	not CV	set CCR to AND(Rs, Rd)
ANDI	011101	RI	111dddd00ssss		Rd XOR neg 8 to +7					PC+2	not CV	remapped to XOR of Rd and immediate of -8 to 7
ANDI	011110	RI	111dddd00ssss		Rd XOR ssss+8/-16					PC+2	not CV	remapped to XOR of Rd and immediate of 8-15 or neg 9-16
ANDI	011111	RI	111dddd00ssss		Rd XOR ssss+16/-24					PC+2	not CV	remapped to XOR of Rd and immediate of 16-23 or neg 17-24
LDSB	100000	RS	000dddd00ssss									
ADDB	100001	RS	000dddd00ssss		0--0&Rs7-0 + Rd					PC+2	all	ADD low byte of Rs with Rd
ADDSH	100010	RS	000dddd00ssss		signed Rs15-0 + Rd					PC+2	all	ADD low half of Rs with Rd
ADDW	100011	RS	000dddd00ssss		Rs + Rd					PC+2	all	ADD Rs with Rd
ANDCW	100100	RS	000dddd00ssss		NOT Rs AND Rd					PC+2	not CV	AND NOT Rs with Rd
ADDI	100101	RI	000dddd00ssss		Rd + neg 8 to +7					PC+2	all	remapped to ADD of Rd and immediate of -8 to 7
ADDI	100110	RI	000dddd00ssss		Rd + ssss+8/-16					PC+2	all	remapped to ADD of Rd and immediate of 8-15 or neg 9-16
ADDI	100111	RI	000dddd00ssss		Rd + ssss+16/-24					PC+2	all	remapped to ADD of Rd and immediate of 16-23 or neg 17-24
LDH	101000	RS	001dddd00ssss									
ADCB	101001	RS	001dddd00ssss		0--0&Rs7-0 + Rd					PC+2	all	ADD with carry low byte of Rs with Rd
ADCSH	101010	RS	001dddd00ssss		signed Rs15-0 + Rd					PC+2	all	ADD with carry low half of Rs with Rd
ADCW	101011	RS	001dddd00ssss		Rs + Rd					PC+2	all	ADD with carry Rs with Rd
CMPB	101100	RS	001dddd00ssss							PC+2	not V	set CCR to Rd - Rs
ADCI	101101	RI	001dddd00ssss		Rd + neg 8 to +7					PC+2	all	remapped to ADC of Rd and immediate of -8 to 7
ADCI	101110	RI	001dddd00ssss		Rd + ssss+8/-16					PC+2	all	remapped to ADC of Rd and immediate of 8-15 or neg 9-16
ADCI	101111	RI	001dddd00ssss		Rd + ssss+16/-24					PC+2	all	remapped to ADC of Rd and immediate of 16-23 or neg 17-24
1-OP	110000	RS	010dddd00ssss									Rd used as op-code
SUBB	110001	RS	010dddd00ssss		0--0&Rs7-0 - Rd					PC+2	all	ADD low byte of Rs with Rd
SUBSH	110010	RS	010dddd00ssss		signed Rs15-0 - Rd					PC+2	all	ADD low half of Rs with Rd
SUBW	110011	RS	010dddd00ssss		Rs - Rd					PC+2	all	ADD Rs with Rd
CMPH	110100	RS	010dddd00ssss							PC+2	not V	set CCR to Rd - Rs
ROTI	110101	RI	010dddd00ssss		Rd << neg 8 to +7					PC+2	not V	remapped to rotate of Rd by immediate of -8 to 7
ROTI	110110	RI	010dddd00ssss		Rd << ssss+8/-16					PC+2	not V	remapped to rotate of Rd by immediate of 8-15 or neg 9-16
ROTI	110111	RI	010dddd00ssss		Rd << ssss+16/-24					PC+2	not V	remapped to rotate of Rd by immediate of 16-23 or neg 17-24
PFX	111000	RS	011dddd00ssss									remainder of instruction used with next instruction for expanded instru
SBCB	111001	RS	011dddd00ssss		0--0&Rs7-0 - Rd					PC+2	all	ADD with carry low byte of Rs with Rd
SBCSH	111010	RS	011dddd00ssss		signed Rs15-0 - Rd					PC+2	all	ADD with carry low half of Rs with Rd
SBCW	111011	RS	011dddd00ssss		Rs - Rd					PC+2	all	ADD with carry Rs with Rd
CMPW	111100	RS	011dddd00ssss							PC+2	not V	set CCR to Rd - Rs
ASLI	111101	RI	011dddd00ssss		Rd << neg 8 to +7					PC+2	not V	remapped to arithmetic shift of Rd by immediate of -8 to 7
ASLI	111110	RI	011dddd00ssss		Rd << ssss+8/-16					PC+2	not V	remapped to arithmetic shift of Rd by immediate of 8-15 or neg 9-16
ASLI	111111	RI	011dddd00ssss		Rd << ssss+16/-24					PC+2	not V	remapped to arithmetic shift of Rd by immediate of 16-23 or neg 17-24
Register indirect operations												s bits less than 1100
LDB	000001	R(S)	100dddd01ssss		unsigned (Rs)7-0					PC+2		zero extend low byte of Rs
LDHS	000010	R(S)	100dddd01ssss		signed (Rs)15-0					PC+2		sign extend low 16 bits of Rs
LDW	000011	R(S)	100dddd01ssss		(Rs)					PC+2		move Rs to Rd

DADB	000100	R(S)	00dddd01ssss	bcd((Rs)+Rd)	PC+2	all	low byte decimal add (Rs) to Rd
STB	000101	R(S)	00dddd01ssss	(Rs)	PC+2		store low byte of RD at (RS)
STH	000110	R(S)	00dddd01ssss	(Rs)	PC+2		store Rd15-0 at (Rs)
STW	000111	R(S)	00dddd01ssss	(Rs)	PC+2		store Rd at (Rd)
ORB	001001	R(S)	01dddd01ssss	Rd OR unsigned (Rs)7-0	PC+2	not CV	OR low byte of Rs with Rd
ORH	001010	R(S)	01dddd01ssss	Rd OR signed (Rs)15-0	PC+2	not CV	OR low half of Rs with Rd
ORW	001011	R(S)	01dddd01ssss	Rd OR (Rs)	PC+2	not CV	OR Rs with Rd
BITB	001100	R(S)	01dddd01ssss		PC+2	not CV	set CCR to AND of (Rs) and Rd
RORB	001101	R(S)	01dddd01ssss		PC+2	not CV	store Rd OR (Rs) at (Rs)
RORH	001110	R(S)	01dddd01ssss		PC+2	not CV	store Rd OR (Rs) at (Rs)
RORW	001111	R(S)	01dddd01ssss		PC+2	not CV	store Rd OR (Rs) at (Rs)
XORB	010001	R(S)	10dddd01ssss	Rd XOR unsigned (Rs)7-0	PC+2	not CV	XOR low byte of (Rs) with Rd
XORH	010010	R(S)	10dddd01ssss	Rd XOR signed (Rs)15-0	PC+2	not CV	XOR low half of (Rs) with Rd
XORW	010011	R(S)	10dddd01ssss	Rd XOR (Rs)	PC+2	not CV	XOR (Rs) with Rd
BITH	010100	R(S)	10dddd01ssss		PC+2	not CV	set CCR to AND of (Rs) and Rd
RXORB	010101	R(S)	10dddd01ssss		PC+2	not CV	store Rd XOR (Rs) at (Rs)
RXORH	010110	R(S)	10dddd01ssss		PC+2	not CV	store Rd XOR (Rs) at (Rs)
RXORW	010111	R(S)	10dddd01ssss		PC+2	not CV	store Rd XOR (Rs) at (Rs)
ANDB	011001	R(S)	11dddd01ssss	Rd AND unsigned (Rs)7-0	PC+2	not CV	XOR low byte of Rs with Rd
ANDH	011010	R(S)	11dddd01ssss	Rd AND signed (Rs)15-0	PC+2	not CV	XOR low half of Rs with Rd
ANDW	011011	R(S)	11dddd01ssss	Rd AND (Rs)	PC+2	not CV	XOR Rs with Rd
BITW	011100	R(S)	11dddd01ssss		PC+2	not CV	set CCR to AND(Rs, Rd)
RANDB	011101	R(S)	11dddd01ssss	Rd XOR unsigned (Rs)7-0	PC+2	not CV	store Rd AND (Rs) at (Rs)
RANDH	011110	R(S)	11dddd01ssss	Rd XOR signed (Rs)15-0	PC+2	not CV	store Rd AND (Rs) at (Rs)
RANDW	011111	R(S)	11dddd01ssss	Rd XOR(Rs)	PC+2	not CV	store Rd AND (Rs) at (Rs)
LDSB	100000	R(S)	00dddd01ssss				
ADDB	100001	R(S)	00dddd01ssss	0--0&Rs7-0 + Rd	PC+2	all	ADD low byte of Rs with Rd
ADDSH	100010	R(S)	00dddd01ssss	signed Rs15-0 + Rd	PC+2	all	ADD low half of Rs with Rd
ADDW	100011	R(S)	00dddd01ssss	Rs + Rd	PC+2	all	ADD Rs with Rd
ANDCW	100100	R(S)	00dddd01ssss		PC+2	not CV	AND NOT Rs with Rd
RADDB	100101	R(S)	00dddd01ssss	Rd + neg 8 to +7	PC+2	all	store Rd + (Rs) at (Rs)
RADDH	100110	R(S)	00dddd01ssss	Rd + ssss+8/-16	PC+2	all	store Rd + (Rs) at (Rs)
RADDW	100111	R(S)	00dddd01ssss	Rd + ssss+16/-24	PC+2	all	store Rd + (Rs) at (Rs)
LDH	101000	R(S)	01dddd01ssss				
ADCB	101001	R(S)	01dddd01ssss	0--0&Rs7-0 + Rd	PC+2	all	ADD with carry low byte of (Rs) to Rd
ADCSH	101010	R(S)	01dddd01ssss	signed Rs15-0 + Rd	PC+2	all	ADD with carry low half of (Rs) to Rd
ADCW	101011	R(S)	01dddd01ssss	Rs + Rd	PC+2	all	ADD with carry (Rs) to Rd
CMPB	101100	R(S)	01dddd01ssss		PC+2	not V	set CCR to Rd - (Rs)
RADCB	101101	R(S)	01dddd01ssss	Rd + neg 8 to +7	PC+2	all	store ADC of Rd and (Rs) at (Rs)
RADCH	101110	R(S)	01dddd01ssss	Rd + ssss+8/-16	PC+2	all	store ADC of Rd and (Rs) at (Rs)
RADCW	101111	R(S)	01dddd01ssss	Rd + ssss+16/-24	PC+2	all	store ADC of Rd and (Rs) at (Rs)
1-OP	110000	R(S)	10dddd01ssss				Rs used as op-code for single operand instructions
SUBB	110001	R(S)	10dddd01ssss	0--0&Rs7-0 - Rd	PC+2	all	SUB low byte of (Rs) from Rd
SUBSH	110010	R(S)	10dddd01ssss	signed Rs15-0 - Rd	PC+2	all	SUB low half of (Rs) from Rd
SUBW	110011	R(S)	10dddd01ssss	Rs - Rd	PC+2	all	SUB (Rs) from Rd
CMPH	110100	R(S)	10dddd01ssss		PC+2	not V	set CCR to Rd - (Rs)
RSUBB	110101	R(S)	10dddd01ssss	Rd << neg 8 to +7	PC+2	all	subtract Rd from (Rs) and store at (Rs)
RSUBH	110110	R(S)	10dddd01ssss	Rd << ssss+8/-16	PC+2	all	subtract Rd from (Rs) and store at (Rs)
RSUBW	110111	R(S)	10dddd01ssss	Rd << ssss+16/-24	PC+2	all	subtract Rd from (Rs) and store at (Rs)
PFX	111000	R(S)	11dddd01ssss				remainder of instruction used with next instruction for expanded instru
SBCB	111001	R(S)	11dddd01ssss	0--0&Rs7-0 - Rd	PC+2	all	SBC low byte of (Rs) from Rd
SBCSH	111010	R(S)	11dddd01ssss	signed Rs15-0 - Rd	PC+2	all	SBC low half of (Rs) from Rd
SBCW	111011	R(S)	11dddd01ssss	Rs - Rd	PC+2	all	SBC (Rs) from Rd
CMPW	111100	R(S)	11dddd01ssss		PC+2	not V	set CCR to Rd - (Rs)
RSBCB	111101	R(S)	11dddd01ssss	Rd << neg 8 to +7	PC+2	all	subtract with carry Rd from (Rs) and store at (Rs)
RSBCH	111110	R(S)	11dddd01ssss	Rd << ssss+8/-16	PC+2	all	subtract with carry Rd from (Rs) and store at (Rs)
RSBCW	111111	R(S)	11dddd01ssss	Rd << ssss+16/-24	PC+2	all	subtract with carry Rd from (Rs) and store at (Rs)

Register indirect auto increment operations

					s bits less than 1100
LDB	001000dddd10ssss	0--0&Rs7-0	PC+2		zero extend low byte of Rs
LDHS	010000dddd10ssss	0--0&Rs15-0	PC+2		sign extend low 16 bits of Rs
LDW	011000dddd10ssss	Rs	PC+2		move Rs to Rd
DADB	100000dddd10ssss	bcd(Rs+Rd)	PC+2	all	low byte decimal add Rs to Rd
STB	101000dddd10ssss	neg 8 to +7	PC+2		store low byte of Rs at (Rd)
STH	110000dddd10ssss	ssss+8/-16	PC+2		store Rs15-0 at (Rd)
STW	111000dddd10ssss	ssss+16/-24	PC+2		store Rs at (Rd)
ORB	001001dddd10ssss		PC+2	not CV	OR low byte of Rs with Rd
ORH	010001dddd10ssss		PC+2	not CV	OR low half of Rs with Rd
ORW	011001dddd10ssss		PC+2	not CV	OR Rs with Rd
BITB	100001dddd10ssss		PC+2	not CV	set CCR to AND(Rs,(Rd))
RORB	101001dddd10ssss		PC+2	not CV	remapped to OR of Rd and immediate of -8 to 7
RORH	110001dddd10ssss		PC+2	not CV	remapped to OR of Rd and immediate of 8-15 or neg 9-16
RORW	111001dddd10ssss		PC+2	not CV	remapped to OR of Rd and immediate of 16-23 or neg 17-24

Register indirect auto decrement operations

						s bits less than 1100
LDB	**001000dddd11ssss**	0--0&Rs7-0		PC+2		zero extend low byte of Rs
LDHS	**010000dddd11ssss**	0--0&Rs15-0		PC+2		sign extend low 16 bits of Rs
LDW	**011000dddd11ssss**	Rs		PC+2		move Rs to Rd
DADB	**100000dddd11ssss**	bcd(Rs+Rd)		PC+2	all	low byte decimal add Rs to Rd
STB	**101000dddd11ssss**	neg 8 to +7		PC+2		store low byte of Rs at (Rd)
STH	**110000dddd11ssss**	ssss+8/-16		PC+2		store Rs15-0 at (Rd)
STW	**111000dddd11ssss**	ssss+16/-24		PC+2		store Rs at (Rd)
ORB	**001001dddd11ssss**			PC+2	not CV	OR low byte of Rs with Rd
ORH	**010001dddd11ssss**			PC+2	not CV	OR low half of Rs with Rd
ORW	**011001dddd11ssss**			PC+2	not CV	OR Rs with Rd
BITB	**100001dddd11ssss**			PC+2	not CV	set CCR to AND(Rs,(Rd))
RORB	**101001dddd11ssss**			PC+2	not CV	remapped to OR of Rd and immediate of -8 to 7
RORH	**110001dddd11ssss**			PC+2	not CV	remapped to OR of Rd and immediate of 8-15 or neg 9-16
RORW	**111001dddd11ssss**			PC+2	not CV	remapped to OR of Rd and immediate of 16-23 or neg 17-24

1-OP instructions

CALL	**110000**	**S**	**00000000ssss**		Rs	
CALL	**110000**	**(S)**	**00000001ssss**		Rs	Indirect call
CALL	**110000**	**(S++)**	**00000010ssss**		(Rs)	DTC call
CALL	**110000**	**(--S)**	**00000011ssss**		(Rs)	DTC call?
CALL	**110000**	**(S+d)**	**000000ss11ss**	PC+2	(--Rs)	Dispatch call
CALL	**110000**	**d**	**000000111100**	PC+2	d	Absolute call
CALL	**110000**	**(d)**	**000000111101**	PC+2	(d)	Absolute indirect call
CALL	**110000**	**(SP)**	**000000111110**		(SP)	Swap PC with (SP)
CALL	**110000**	**PC+d**	**000000111111**	PC+2	(PC+2)	Relative call
CALLR	**111000**		**11100010dddddddd**		mm(Rs)	nearby relative call

Branches	x=1	x=0	
000x	BRA	NOP	NOP is a one by
001x	BCS, BHS	BCC, BLO	
010x	BZ, BEQ	BNZ, BNE	
011x	BMI, BLT	BPL, BGE	
100x	BHI	BLS	BHI: C & ~Z BOI
101x	BGT	BLE	
110x	BLT	BGE	BLT: N ^ V == 1
111x	BVS	BVC	

Addressing modes		
RS	00ssss	ssss<12
RI	00ssss	short signed immediate
R(S)	01ssss	ssss<12
R(S++)	10ssss	ssss<12
R(--S)	11ssss	ssss<12
R(S+d)	ss11ss	ssss<12
RI	111100	
R(I)	111101	
R(SP)	111110	
R(PC+d)	111111	