Alternative VAX ISA

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Abstract:

Limit ISA to at most one memory location per instruction. Keep most of the VAX addressing modes. Encoding is as three register fields, addressing mode field and location of its register field. A 24-bit instruction is possible with 16 registers and a 32-bit instruction with 32 registers. PC, frame pointer and stack pointer part of the register file. A 32-bit instruction has room for a predicate field.

Prefix instructions used to specify a scaled index register
Immediate fields contain a size code
Single operand/destination instructions in 16-bits: CLR, INC, etc.
Single operand with immediate in 16 bits plus size of immediate: ADDI, LDI, etc.

16-bit instructions:

8 bits Op-code (also encodes data size)
4 bits Register
Log2(5) Addressing mode: Register, register indirect, (R)++, (--R), (R+offset); no double indirection
1 bit Immediate present for the second operand

24-bit encoding:

8 bits Op-code (also encodes data size)
4 bits Register 1
4 bits Register 2
4 bits Register 3
Log2(5) Addressing mode: Register, register indirect, (R)++, (--R), (R+offset); no double indirection
Log2(3) Memory reference location (first, second or third register)

32-bit encoding:

8 bits Op-code (also encodes data size)
4 bits Predication field
1 bit Status register update enable
5 bits Register 1
5 bits Register 2
5 bits Register 3
Log2(5) Addressing mode: Register, register indirect, (R)++, (--R), (R+offset); no double indirection
Log2(3) Memory reference location (first, second or third register)