ProNoC

Timer

Summary

A simple, general purpose, Wishbone bus-based, 32-bit timer. Includes:

- Clear timer on compare match value with auto-reload
- Clock prescaler
- Compare match interrupt source

Timer block diagram:

Figure1 depicts the functional block diagram of NI-master module.

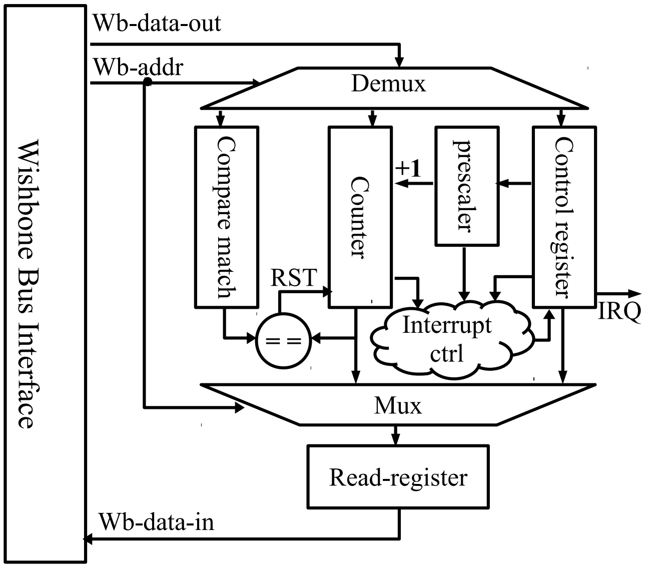

Figure 1: 32-bit timer block diagram.

Parameters Description

Table 1: Timer GUI Parameters.

Name	Description	Permitted values	Default
MAX_PRESCALER	This parameter defines the maximum possible prescaler value. It must be power of 2.	$n \in 2^m$, $1 \leqslant m$	256

Slave wishbone bus registers

The 32-bit timer can be controlled using wishbone bus slave interface. Table 2 shows the 32-bit timer internal registers. All 32-bit timer registers are memory mapped.

Table 2: 32-bit timer memory map registers.

Address	Register Name	Description
0	TCSR	Timer Control Status Register
1	TLR	Timer Load Register
2	TCMR	Timer Compare Match Register

TCSR Timer control status register.

Bit	PRESCALER_WIDTH+3	4	3
	Prescaler value		timer_isr
Read/Write	RW		RW
Initial Value	0		0

Bit	2	1	0
	reset_enable_on_tcmr	interrupt_enable_on_tcmr	timer_enable
Read/Write	RW	RW	RW
Initial Value	0	0	0

Prescaler value: This value is used as a compare match value for prescaler timer. When the match happens, the main timer value is incremented by one at the posedge of system clock.

timer_isr: The timer interrupt service routing is a one-bit register that is used for acknowledging the compare match interrupt. This interrupt is acknowledged by writing logic one on this register.

reset enable on tcmr: If this register is asserted, then the timer is auto-reset when reaches the compare match value.

interrupt enable on tcmr: If this register is asserted, then the timer intterupt is asserted when the timer reaches the compare match value.

timer_enable The timer is enabled when this register is one.

TLR Timer load register. The timer value can be read by this register. Writing on this register initializes the timer's counter register.

Bit	31	0
	TLR	
Read/Write	RW	
Initial Value	0	

TCMR Timer compare match register. The timer can be configured to be auto-reseted or to assert an interrupt when the timer reaches the compare match value.

Bit	31	0
	TCMR	
Read/Write	RW	
Initial Value	0	

Tmer Sample C code

```
#define EN          (1 << 0)
#define INT_EN      (1 << 1)
#define RST_ON_CMP  (1 << 2)

// Enable the timer, reset on compare value, and interrupt
void int_init ( unsigned int compare ){
    TCMR    =   compare;
    TCSR   =    ( EN | INT_EN | RST_ON_CMP);
}

void isr(void){
    //write your interrupt code here

    TCSR=TCSR; //ack int
    return;
}

int main(){
    int_init ( 50000 );
    while(1){


}}
```