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READERS SOLVE DESIGN PROBLEMS

Compact, four-quadrant lock-in amplifier generates two analog outputs

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The circuit in this Design Idea realizes a simple, low-cost lock-in amplifier employing an Analog Devices (www.analog.com) AD630 balanced modulator-demodulator IC (**Reference 1**). The device uses laser-trimmed thin-film resistors, yielding accuracy and stability and, thus, a flexible commutation architecture. It finds use in sophisticated signal-processing applications, including synchronous detection. The amplifier can detect a weak ac signal even in the presence of noise sources of much greater amplitude when you know the signal's frequency and phase.

As an analog multiplier, the AD630 reveals the component of the input-voltage signal in a narrow band around the frequency of the reference signal. The lowpass filter at the AD630's output allows you to gain information on the weak signal amplitude, which the uncorrelated noise originally masked. When the input voltage and the reference voltage are in phase, the lowpass filter's output, V_{OUT}, assumes the maximum amplitude. Conversely, if the input voltage and the reference voltage are in quadrature, the output voltage would ideally be 0V. In this way, if both in-phase and quadrature reference signals are available, two balanced demodulators reveal the in-phase output voltage to be 0° and the in-quadrature output voltage to be 90°. You can calculate the module and phase shift as follows:

$$|V_{OUT}| = \sqrt{V^2_{OUT0°} + V^2_{OUT90°}};$$

$$\angle V_{OUT} = \tan^{-1}\left(\frac{V_{OUT90°}}{V_{OUT0°}}\right).$$

The two AD630s have a gain of ±2 and receive the amplified signal, V_{IN}, through two identical amplifiers, A_1 and A_2. At Pin 7 of IC_1, a bipolar ±5V squared signal appears in phase with

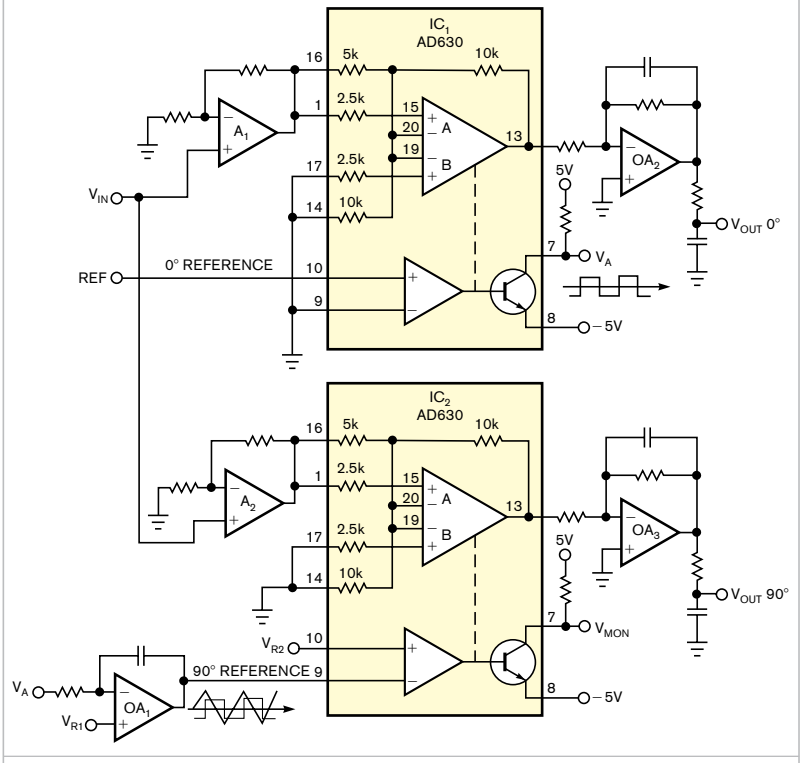

Figure 1 OA_1 integrates the bipolar V_A signal and creates a triangular wave. V_{R1} and V_{R2} obtain a 90°-shifted reference voltage with respect to V_A.

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the reference signal. OA_1 integrates the amplifier voltage, which generates a triangular wave that IC_2's comparator compares with the V_{R2} voltage. You must regulate V_{R1} and V_{R2} to obtain a perfect 90°-shifted command for IC_2. You can monitor the voltage at IC_2's Pin 7. Measurement accuracy and repeatability depend strongly on the RC time constant of the integrator and the values of V_{R1} and V_{R2}.

You can use a different approach to generate in-phase and in-quadrature reference signals. **Figure 2** shows an all-digital circuit, which you can implement in a small CPLD (complex programmable-logic device) to generate the 0 and 90° reference signals in **Figure 1**. Counter 1 measures the reference-signal time in terms of the N number of digital clock pulses, where the reference time can be different from 50%. It receives a preset command at the $N_1=1$ value at each positive front edge of the reference signal. D-type flip-flop IC_1 generates such pulses. At each positive edge of the reference signal, IC_2 acquires the N/4 value. Meanwhile, Counter 2 counts the clock periods and receives a restart command at the $N_2=1$ value when its value reaches the comparator-measured N/4 quantity.

AN INCREASE IN THE NUMBER OF BITS DECREASES THE MAXIMUM REFERENCE FREQUENCY.

To overcome the lack of the last EQ signal when the reference time is greater than approximately four times the N/4 integer value, the OR combination of the two RST and EQ pulses yields four almost-equidistant positive-edge commands in each reference-time period. The N/4 integer division, a logical right shift by 2 bits of N_1, gives a maximum error of three on the last pulse position. These pulses generate the in-phase and in-quadrature signals, 0 and 90°, respectively, resulting from simple commutations on the positive or negative edges of the signal. T-type flip-flop IC_3 generates a signal with twice the frequency of the reference signal. In this way, the accuracy is equal to $3/N_1$.

To maintain accuracy at least comparable with that of the AD630, the N_1 output of Counter 1 would be the highest. However, an increase in the number of bits decreases the maximum reference frequency for a given digital-clock frequency if you want N_1 to reach high values. For example, if N is 15 bits, the N_1 output assumes the 32,767 maximum value with an accuracy of approximately 0.01%. If the reference-time period decreases, you can assume a minimum value of 3277—that is, one-tenth of the maximum value—for N_1, with a correspondingly lower accuracy of 0.1%, which is comparable to the gain accuracy of the AD630. To increase the reference frequency, divide the digital clock's frequency to select low values when the reference time becomes too long. EDN

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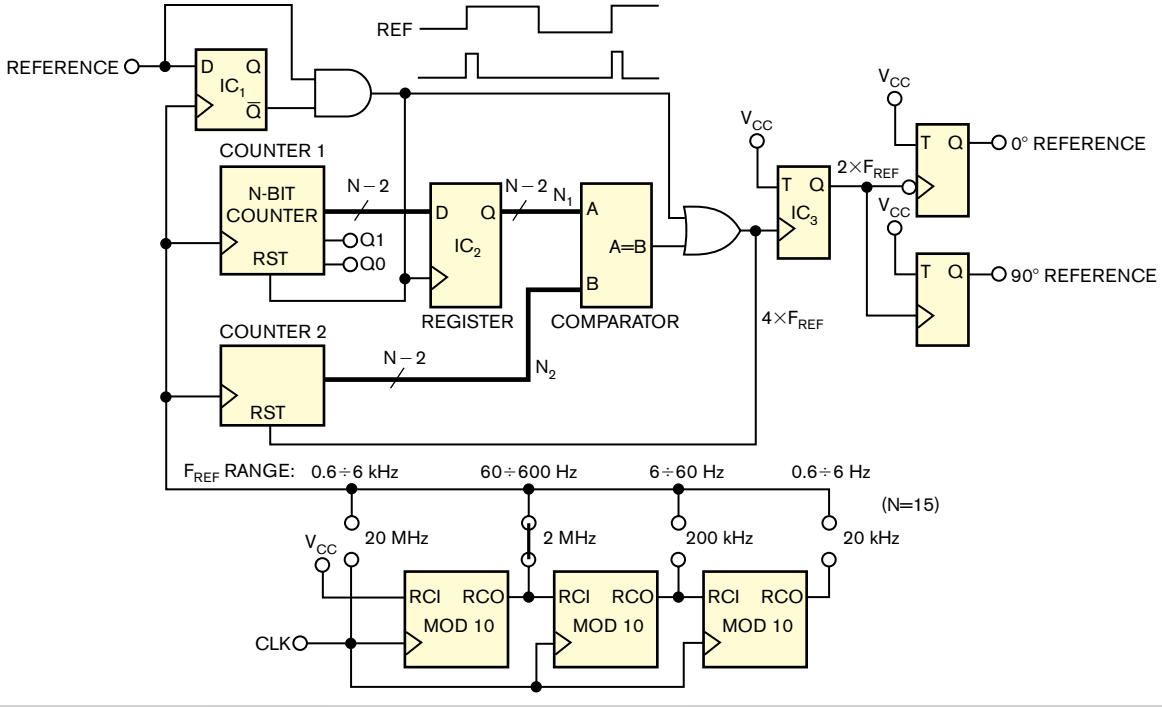

Figure 2 You can implement this all-digital circuit in a small CPLD.

Eight-function remote uses one button, no microcode

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Many people with significant physical disabilities can't operate everyday mechanisms, such as TV remote controls. To make matters worse, adaptive technologies are often unaffordable unless insurance covers them. This Design Idea describes an interface circuit that lets a disabled person control eight remote-control functions. The design uses older, small-scale-integration ICs because of their simplicity, low power requirements, affordability, and availability at stores such as Radio Shack (www.radioshack.com). Because the circuit uses no microcontroller, you need not do any programming.

Power for the circuit in **Figure 1** comes from four 1.5V AA batteries in series. Diodes D_1 through D_4 reduce the battery power from 6V to approximately 3.4V, and they protect against accidental reverse polarity of the batteries. IC_1, a 555 timer, and associated discrete components form a repetitive-pulse generator. Potentiometer R_1 adjusts the pulse speed. This pulse feeds directly into decade counter, IC_2, which causes indicator LEDs LED_1 through LED_4 to sequence on and off. Each output of the decade counter feeds one input of CMOS gate IC_3 and AND gate IC_4.

Normally, the output of the NAND gate is low because both inputs must be logic one to produce a logic-one output to close one of the CMOS switches, IC_5 and IC_6.

If the user presses the control switch while the desired LED is lit, both inputs to one of IC_3's AND gates are at logic one, causing the output to be logic one and closing a 4066 switch, which is effectively the same as pressing one of the buttons on the remote control. As long as the control switch remains closed, the 555 pulses remain disabled and LED_1 through LED_4 remain in their current state. This characteristic is important because a person can continue to hold the control switch closed to continuously increment the changing of a channel or increase or decrease the volume. EDN

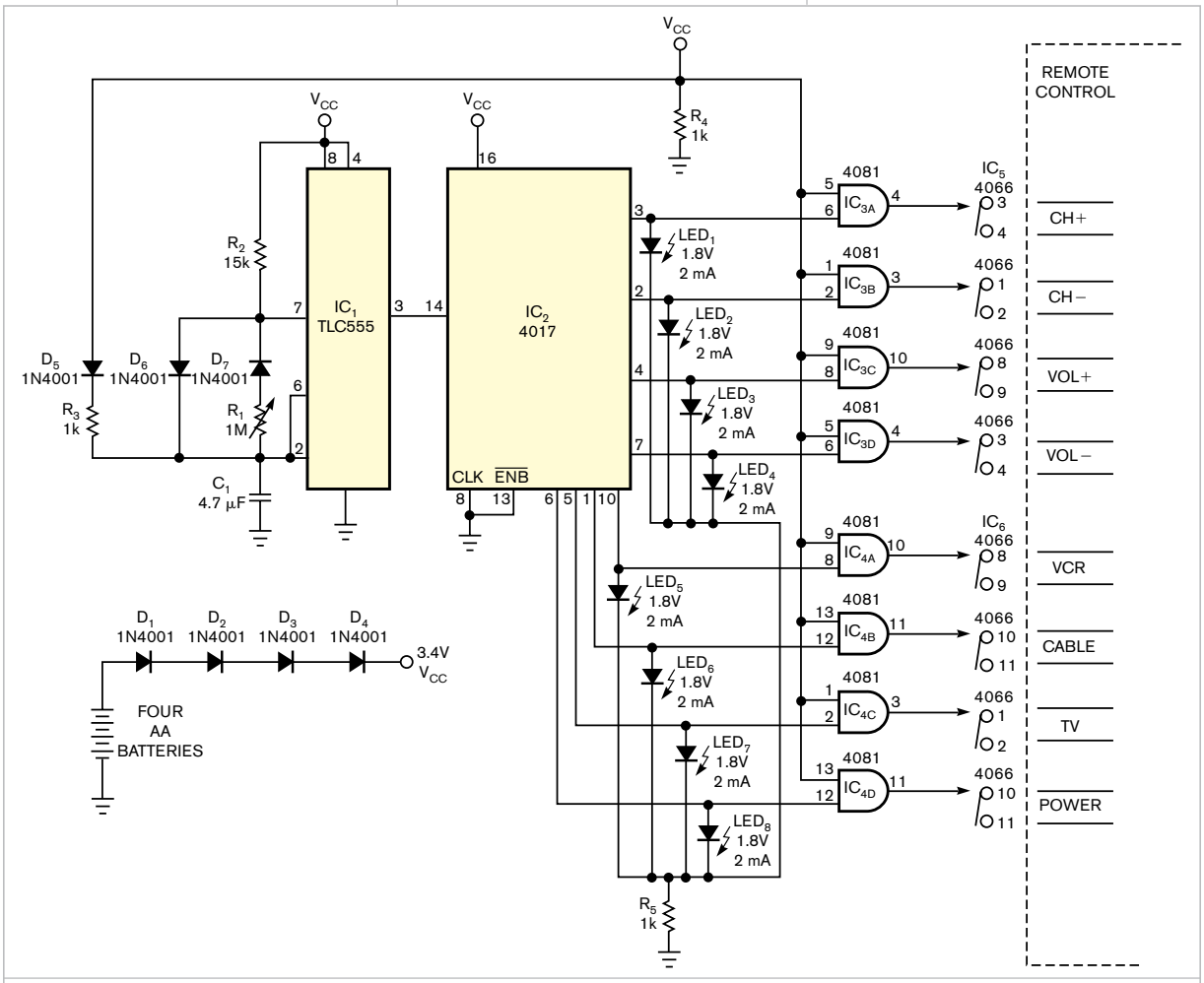

Figure 1 This interface circuit allows a disabled person to control eight remote-control functions.

Doorbell transformer acts as simple water-leak detector

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Shortly after installation, the simple water-leak-detector circuit in this Design Idea saved the day and hundreds of dollars. The average life expectancy of a hot-water heater is about 10 years. It's not a question of whether it will leak; it is simply a matter of when it will leak. The builders of new homes in the Midsouth region of the United States have been installing hot-water heaters in attics. This approach saves valuable space; however, if you only infrequently visit the attic, you may not discover that your hot-water heater is leaking until it is too late. By that time, it may cost you hundreds of dollars to repair the water damage to ceilings and walls.

The circuit in **Figure 1** detects hot-water-heater leakage, and you can also use it for detecting leaks in dishwashers, garbage disposals, ice makers, swimming pools, hot tubs, and waterbeds. **Figure 2** shows the completed circuit.

Most doorbell transformers produce

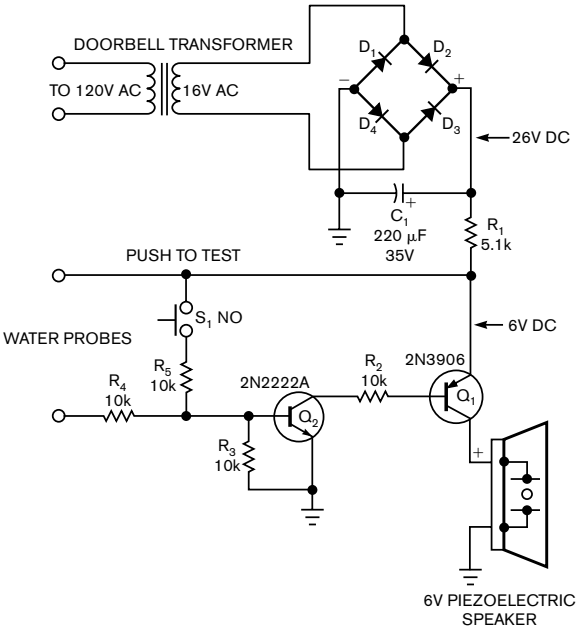

Figure 1 A transformer and a bridge provide power for the speaker.

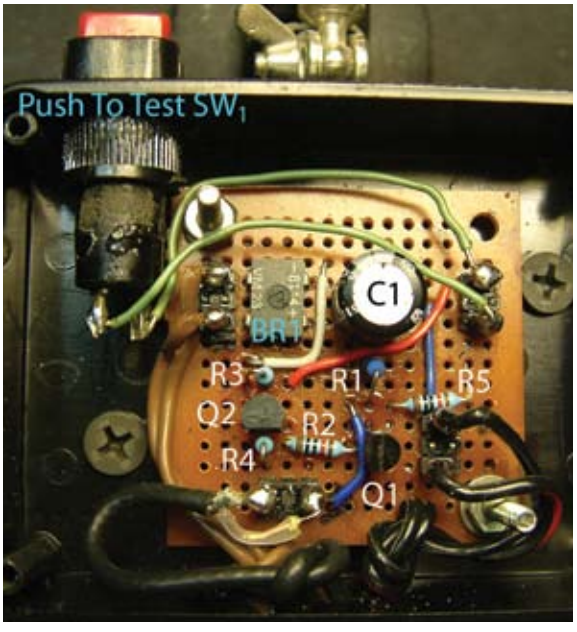

Figure 2 The circuit includes a push-to-test button.

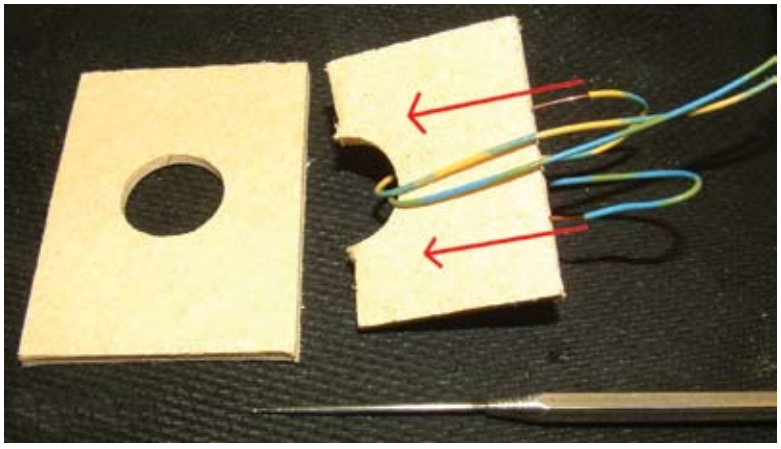

Figure 3 Use a sponge and copper wire to form a water probe.

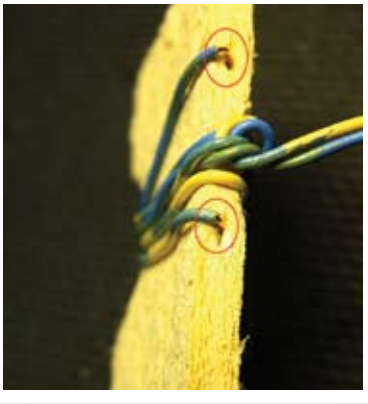

Figure 4 The completed probe with bare wire inside senses water through a change in resistance.

16 to 20V ac. To drive the buzzer, you must convert the ac voltage to dc: Multiply the ac voltage by 1.414 to yield the dc-rms voltage. Connect the wires to the secondary side of the transformer to a bridge rectifier and then into a filtering electrolytic capacitor. Your power supply should now be providing about 26V dc. The 5.1-kΩ resistor, R_1, limits the current to the buzzer. When the system detects water or when you press the push-to-test switch, you have about 6V dc to operate the circuit and sound the piezoelectric speaker. Mount the speaker so that you'll hear it when it sounds.

Transistors Q_1 and Q_2 can be any general-purpose NPN and PNP types, respectively. The water probes use copper wires about 1 in. apart from each other. You then pierce two holes, about 1 in. apart, into a sponge from a soldering station. Insert bare copper wire into these holes (**Figure 3**). Take some of the remaining wire but leave the insulation on it and wrap it around the sponge so that the bare copper wire does not come out (**Figure 4**).

You can now place this sponge in the metal overflow tray underneath the hot-water heater. When the hot water leaks, the sponge absorbs it. The resistance between the two bare copper wires then drops to about 1 MΩ or less, which forward-biases the two transistors and enables the piezoelectric speaker. The cost for this circuit shouldn't exceed $25. If you have more than one hot-water heater in the same area, you can make another water probe and tie the two probes together in parallel. EDN

Inverted regulator increases choice and reduces complexity

David McCracken, Aptos, CA

Most circuits are referenced to ground, where relatively low-voltage components can monitor and control the low side of a load but not the high side. For example, nearly any low-voltage rail-to-rail-input op amp can detect a voltage increase indicating overcurrent through a resistor that connects between the load and ground. To do the same thing on the high side, you typically select a differential amplifier that tolerates high common-mode voltage. This approach limits the component choices for the

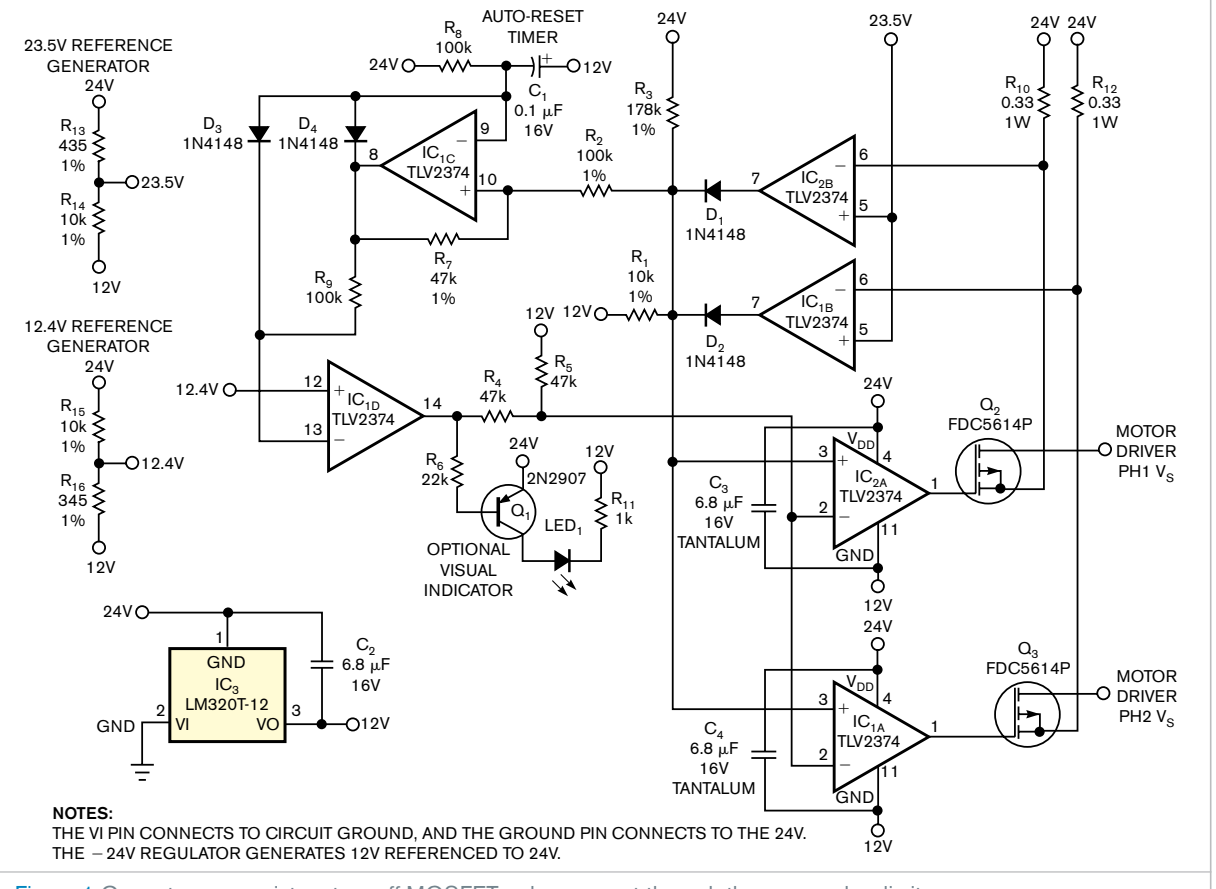

Figure 1 Current-sense resistors turn off MOSFETs when current through them exceeds a limit.

input amplifier and brings up the question of how to respond to an overcurrent. The differential amp produces a low ground-referenced signal from a high-side event, but you can prevent a high-side overcurrent resulting from a short to ground only by turning off the high-side power. In effect, the differential amp translates the high-side signal into the low-side domain in which you must then translate the response back into the high-side domain.

A simpler approach for any high-side overcurrent-protection circuit references the entire circuit to the high-side rail. Such circuits typically consume little power, which a small, three-terminal linear regulator can easily supply. However, this approach requires an unusual configuration employing a negative regulator whose ground pin connects to the high-side rail and whose input connects to system ground. There are no other connections to system ground. All "ground" points of the overcurrent-protection circuit connect to the regulator's out pin.

Figure 1 shows a two-phase-stepper-motor, fast-acting, self-resetting high-side circuit breaker with a 24V power supply to the motor and a 12V power supply to the circuit breaker that is referenced to 24V. The circuit breaker sees the 24V motor's power rail as 12V referenced to its local ground, which the regulator's output provides. Like all negative linear regulators, the circuit requires a 6.8-µF tantalum capacitor.

R_{10} and R_{12}, both 0.33Ω, 1W resistors, provide current sensing for the two phases. High-side power flows through a sense resistor and a P-channel MOSFET to the high-side input of an H bridge (not shown), which drives one motor winding. Current in either phase can cause the sense voltage to increase to 0.5V, triggering the breaker. The circuit responds by turning off both MOSFETs. It then waits 20 msec and turns them back on, automatically clearing momentary shorts. EDN

Debug a microcontroller-to-FPGA interface from the FPGA side

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Microcontrollers and FPGAs often work together in embedded systems. As more functions move into the FPGA, however, debugging the interface between the two devices becomes more difficult. The traditional debugging approach comes from the microcontroller side, which relies on a serial-port printout. This approach adds overhead and may cause timing problems. Furthermore, this approach cannot guarantee uninterrupted and exclusive access to certain addresses because of operating-system multitasking. Thus, a serial-port printout doesn't accurately describe the actions on the microcontroller/FPGA interface.

Instead, you can approach the problem from the FPGA side using a JTAG (Joint Test Action Group) interface as a communication port. This approach uses the internal logic of the FPGA to capture the read/write transactions on the microcontroller/FPGA interface. This method is nonintrusive because the circuit that captures transactions sits between the microcontroller and the FPGA's functioning logic and monitors the data without interfering with it. It stores the captured transaction in the FPGA's RAM resources in real time. You can transfer the data to a PC through the JTAG port's download cable.

The debugging tool comprises the data-capture circuit, the JTAG communication circuit, and the GUI (graphical user interface). The data-capture circuit uses standard HDL (hardware-description language) and instantiates a FIFO (first-in/first-out) buffer in the FPGA. Whenever you read or write to a register, the debugging tool records the corresponding value of the address and data on the bus and stores it in the FIFO buffer. You can retrieve the data through the JTAG's download cable to the PC (**Listing 1**, which is available in the online version of this Design Idea at www.edn.com/091215dia).

Because the FPGA has limited on-chip RAM resources, you must keep the FIFO buffer shallow. To efficiently use the FIFO buffer, the design includes filter and trigger circuits. With inclusive address filtering, the circuit monitors only several discontinuous spans of addresses instead of the whole address space. Exclusive-address filters can filter out several smaller address spans from the inclusive-address spans, enabling finer control of the filter settings (**Listing 2**, which is also available in the online version of this Design Idea at www.edn.com/091215dia).

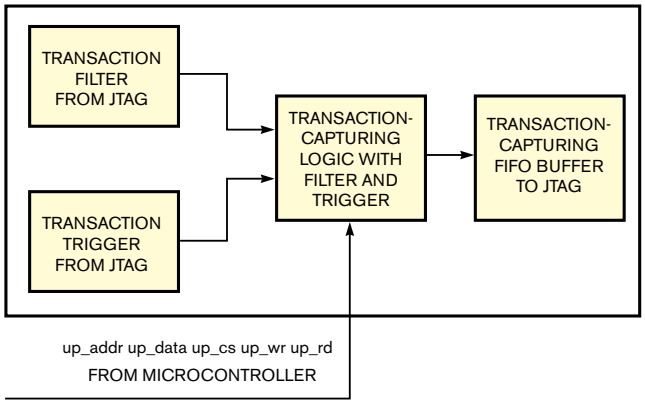

Figure 1 The JTAG's vendor-supplied, customizable communication circuit has two interfaces.

With transaction triggering, the circuit starts when you read from or write to a certain address. You can add certain data values to the triggering condition (**Listing 3**, which is available in the online version of this Design Idea at www.edn.com/091215dia). You can dynamically reconfigure the settings of address filters and transaction triggers through the JTAG's vendor-supplied, customizable communication circuit without recompilation of the FPGA design (**Figure 1**). The circuit has two interfaces, one of which is written in HDL to form a customized JTAG chain. It communicates with the user logic (**listings 1**, **2**, and **3**). The circuit is accessible through specific programming interfaces on the PC and communicates with the user program or GUI (**Listing 4**, which is available in the online version of this Design Idea at www.edn.com/091215dia).

The FPGA-based circuit facilitates writing and reading functions from PC to FPGA logic, and it promotes the JTAG interface to a general communication port attached to the FPGA. FPGA manufacturers, including Actel (www.actel.com), Altera (www.altera.com), Lattice Semiconductor (www.latticesemi.com), and Xilinx (www.xilinx.com), respectively, call this circuit UJTAG (user JTAG), Virtual JTAG, ORCAstra, and BScan (**references 1** through **4**).

The GUI for this circuit uses Tcl/Tk (tool-command-language tool kit). FPGA manufacturers provide vendor-specific APIs (application-programming interfaces) in Tcl for the PC side of the JTAG-communication circuit. The APIs include basic functions, such as JTAG-chain initialization, selection, and data reading and writing. With the data-read function, you can check the capturing status and get the transaction data from the FIFO buffer. With the data-writing function, you can send the filter and trigger configuration data to the capturing circuit in the FPGA (**Listing 4**). The JTAG-based debugging method provides dynamic visibility and controllability into the microcontroller-to-FPGA interface and the FPGA's internal logic without the need to recompile and download FPGA code. EDN

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