1. INSTANTIATING LPM IN EDIF

The LPM standard is designed to take advantage of the existing, widespread support of the EDIF standard. This section describes the syntax for instantiating LPM modules within EDIF netlists.

1.1 EDIF VERSIONS

The LPM 2 2 0 standard netlist can support both EDIF 2 0 0 and EDIF 3 0 0. The LPM standard adheres to the syntax described in the EIA EDIF Standard and refers all details concerning netlist syntax to that document. Note that all names in LPM are case insensitive. LPM_FF and lpm_ff are equivalent, as are data0 and daTA0.

1.2 MODULE DECLARATION

1.2.1 CELL

EDIF netlists follow a strict "declaration before use" rule. Every component must be defined in a library before the component can be used. This means that an EDIF netlist of LPM modules will have a number of cell definitions before the netlist itself appears. These cell definitions can be thought of as "fully described modules" of the (LPM) parameterized modules. Once defined, any number of these "fully described modules" can be instantiated within the netlist. The declaration serves two purposes: it indicates that the module is to be used and it also fixes the values of the parameters to be used (e.g., the AND gate is 4 bits wide). However a design may need both 4-input and 2-input AND gates. Both of these have to be declared and clearly they need to have names that distinguish between them. In addition there may be several instances of use of the same type of gate (e.g., the 2-input AND gate may be used 5 times). Thus LPM has three types of names for each module. These are:

1. **LPM TYPE Name**
   This is a name specified by property LPM_TYPE. These cell names are listed in chapter four and prefixed with “LPM_”. For example, LPM_COUNTER is the LPM_TYPE name in the following example.

   (property LPM_TYPE (string "**LPM_COUNTER**"))

2. **EDIF Cell Name**
   This is a name when the module, a "cell" in EDIF terminology, is declared. For example, addsub_4 is the EDIF cell name in the following example.

   EDIF 2 0 0 example:

   (cell **addsub_4** (cellType generic)
   (view view1 (viewType netlist)
   (interface
   . . . .

EDIF 3 0 0 example:

```
(cell addsub_4 (cellHeader …)
    (cluster . . .
        (interface
      . . . .
```

3. Instance Name

This is the name used by the instance construct when the cell is instantiated. Instance name refers to a unique use of a EDIF Cell name that has already been declared. For example, addsub_4 is the EDIF cell name in the following example.

EDIF 2 0 0 example:

```
(instance addsub1
    (viewRef view1
        (cellRef addsub_4)))
```

EDIF 3 0 0 example:

```
(instance addsub1
     (clusterRef C1
        (cellRef addsub_4)))
```

1.2.2 PORTS

All the used port names are defined in module declaration. Ports include all the required ports and optional ports if they are used. Some port names are not explicit in the standard and depend on associated property. One example is the decode output ports. They are of the form Eqn, where the n is the integer value of LPM_Decodes property.

1.2.2.1 Single Ports

Single port declartion is straight forward in EDIF 2 0 0 and EDIF 3 0 0. For example the clock pin of LPM_FF is declared as follow:

```
(port clock (direction INPUT))
```

1.2.2.2 Bus Port Names

In EDIF 2 0 0, all the bus ports in LPM were flatten as single port due to lack of bus support in EDIF specification. But in EDIF 3 0 0, the bus construct is well defined therefore all the bus ports in LPM cell are maintain as bus in its' cell declaration. . For example with a two-bit output bus in LPM_FF (ie. LPM_Width = 2), the port name for the Q output pin is declared as:

EDIF 3 0 0 example:

```
(port Q0 (outputPort)
```

```
            (nameInformation
               (primaryName "Q0"
                  (nameStructure
                     (complexName "Q"
                           (nameDimension
                              (nameDimensionStructure 0)))))))
      (port Q1 (outputPort)
            (nameInformation
               (primaryName "Q1"
                  (nameStructure
                     (complexName "Q"
                           (nameDimension
                              (nameDimensionStructure 1)))))))
      (portBundle Q
            (portList
               (portRef Q1)
               (portRef Q0))
            (nameInformation
               (primaryName "Q[1:0]"
                     (nameStructure
                     (complexName "Q"
                           (nameDimension
                              (nameDimensionStructure
                                 (sequence 1 0)))))))))
```

Both input numbers and bus numbers start with zero as the least significant bit. And the *rename* construct that used to hold original name in EDIF 2 0 0 is replaced by the *primaryName* in the *nameInformation* construct.

1.2.3 PROPERTIES

All the properties are well defined in their respective LPM module of chapter four. The following properties are listed due to their universal nature among all LPM modules.

1.2.3.1 LPM_TYPE Property

LPM_TYPE property is required to identify the LPM cell type in cell defination. It appears as the string property called LPM_TYPE in the cell defination. For example, LPM_AND is the value of string property LPM_TYPE.

EDIF 2 0 0 example:

```
      (cell and_4 (cellType generic)
            (view view1 (viewType netlist)
                  (interface
                        (port . . .)
```

```
(property LPM_TYPE (string "LPM_AND"))
```

EDIF 3 0 0 example:

```
(cell and_4
    (cellHeader . . .
        (cluster C1
        (interface (interfaceUnits)
            (port . . .)
        (clusterHeader
            (property LPM_TYPE (string "LPM_AND"))
```

1.2.3.2 LPM_Polarity Property

The LPM_Polarity property can be attached to any port in the cell definition of an LPM module. It is a mechanism for inverting the polarity of the port. With this property control, inputs and output ports can be of either polarity (active high or active low. The default value of LPM_Polarity is positive active (no inversion done) and hence the only accepted value for this property is "INVERT" as shown in the following LPM fragment:

```
(port clock
  (property LPM_Polarity (string "INVERT")))
```

LPM_Polarity property declartion is identical between EDIF 2 0 0 and EDIF 3 0 0.

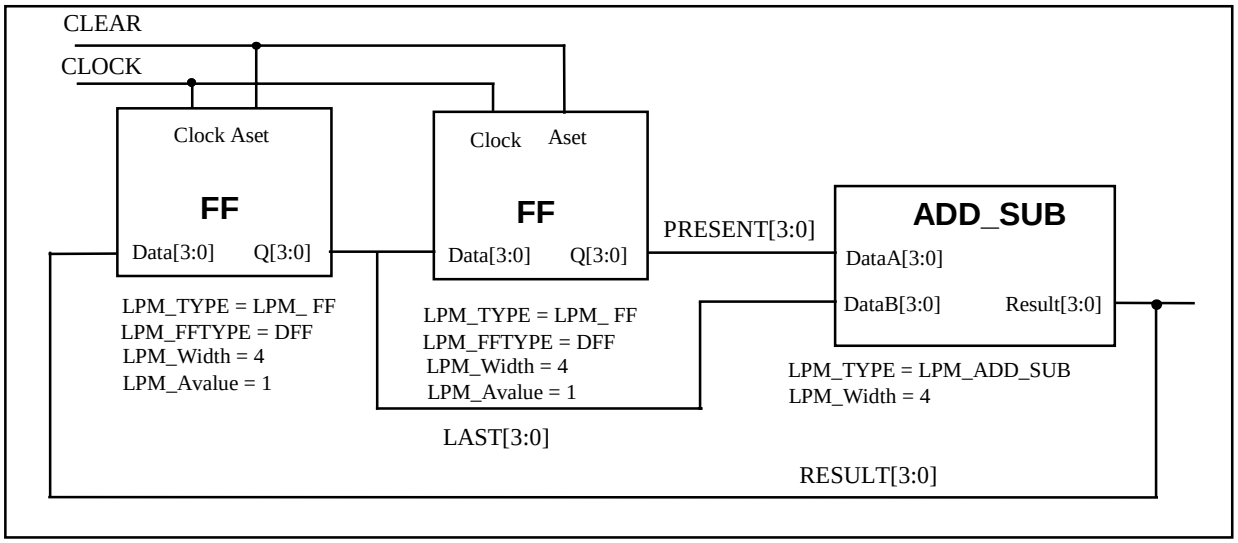
1.2.3.3 LPM_Hint Property

This is an optional property that contains additional technology-specific information for use by the silicon vendor tools. There are no standard values for this field and it is up to the design tool vendors and the silicon tool vendors to utilize it as needed. The LPM_HINT property can always be ignored and the correct logic will be constructed, although it may not be constructed efficiently.

1.3 EXAMPLE

1.3.1 Schematic Description

The schematic example is shown in the following figure.



1.3.2 EDIF 2 0 0 Description

```
(edif fibex  (edifVersion 2 0 0)
    (edifLevel 0)
    (keywordMap (keywordLevel 0))
    (status
        (written
            (timeStamp 1995 11 22 23 2 53)
            (program "EDIFWRITER" (version "v8.4_2.1"))
        )
    )
    (library FIBEX
        (edifLevel 0)
        (technology
            (numberDefinition
                (scale 1 (e 1 -6) (unit distance)))
        )
        (cell dff_4 (cellType generic)
            (view view1 (viewType netlist)
                (interface
                    (port aset (direction INPUT))
                    (port clock (direction INPUT))
                    (port data0 (direction INPUT))
                    (port data1 (direction INPUT))
                    (port data2 (direction INPUT))
                    (port data3 (direction INPUT))
                    (port q0 (direction OUTPUT))
```

```
            (port q1 (direction OUTPUT))
            (port q2 (direction OUTPUT))
            (port q3 (direction OUTPUT))
            (property LPM_Avalue (integer 1))
            (property LPM_TYPE (string "LPM_FF"))
            (property LPM_FFTYPE (string “DFF”))
            (property LPM_Width (integer 4))
        )
    )
)
(cell addsub_4 (cellType generic)
    (view view1 (viewType netlist)
        (interface
            (port dataA0 (direction INPUT))
            (port dataA1 (direction INPUT))
            (port dataA2 (direction INPUT))
            (port dataA3 (direction INPUT))
            (port dataB0 (direction INPUT))
            (port dataB1 (direction INPUT))
            (port dataB2 (direction INPUT))
            (port dataB3 (direction INPUT))
            (port result0 (direction OUTPUT))
            (port result1 (direction OUTPUT))
            (port result2 (direction OUTPUT))
            (port result3 (direction OUTPUT))
            (property LPM_TYPE (string "LPM_ADD_SUB"))
            (property LPM_Width (integer 4))
        )
    )
)
(cell FIBEX (cellType generic)
    (view schematic (viewType netlist)
        (interface
            (port CLEAR (direction INPUT))
            (port CLOCK (direction INPUT))
            (port (rename RESULT_91_0_93_ "RESULT[0]") (direction INOUT))
            (port (rename RESULT_91_1_93_ "RESULT[1]") (direction INOUT))
            (port (rename RESULT_91_2_93_ "RESULT[2]") (direction INOUT))
            (port (rename RESULT_91_3_93_ "RESULT[3]") (direction INOUT))
        )
        (contents
            (instance (rename I_36_1 "I$1")
                (viewRef view1 (cellRef dff_4))
            )
            (instance (rename I_36_3 "I$3")
                (viewRef view1 (cellRef addsub_4))
            )
            (instance (rename I_36_5 "I$5")
                (viewRef view1 (cellRef dff_4))
            )
            (net CLEAR
                (joined
                    (portRef CLEAR)
                    (portRef aset (instanceRef I_36_1))
```

```
            (portRef aset (instanceRef I_36_5))
        )
    )
    (net CLOCK
        (joined
            (portRef CLOCK)
            (portRef clock (instanceRef I_36_1))
            (portRef clock (instanceRef I_36_5))
        )
    )
    (net (rename LAST_91_0_93_ "LAST[0]")
        (joined
            (portRef data0 (instanceRef I_36_5))
            (portRef dataB0 (instanceRef I_36_3))
            (portRef q0 (instanceRef I_36_1))
        )
    )
    (net (rename LAST_91_1_93_ "LAST[1]")
        (joined
            (portRef data1 (instanceRef I_36_5))
            (portRef dataB1 (instanceRef I_36_3))
            (portRef q1 (instanceRef I_36_1))
        )
    )
    (net (rename LAST_91_2_93_ "LAST[2]")
        (joined
            (portRef data2 (instanceRef I_36_5))
            (portRef dataB2 (instanceRef I_36_3))
            (portRef q2 (instanceRef I_36_1))
        )
    )
    (net (rename LAST_91_3_93_ "LAST[3]")
        (joined
            (portRef data3 (instanceRef I_36_5))
            (portRef dataB3 (instanceRef I_36_3))
            (portRef q3 (instanceRef I_36_1))
        )
    )
    (net (rename PRESENT_91_0_93_ "PRESENT[0]")
        (joined
            (portRef dataA0 (instanceRef I_36_3))
            (portRef q0 (instanceRef I_36_5))
        )
    )
    (net (rename PRESENT_91_1_93_ "PRESENT[1]")
        (joined
            (portRef dataA1 (instanceRef I_36_3))
            (portRef q1 (instanceRef I_36_5))
        )
    )
    (net (rename PRESENT_91_2_93_ "PRESENT[2]")
        (joined
            (portRef dataA2 (instanceRef I_36_3))
            (portRef q2 (instanceRef I_36_5))
```

```
                    )
                )
                (net (rename PRESENT_91_3_93_ "PRESENT[3]")
                    (joined
                        (portRef dataA3 (instanceRef I_36_3))
                        (portRef q3 (instanceRef I_36_5))
                    )
                )
                (net (rename RESULT_91_0_93_ "RESULT[0]")
                    (joined
                        (portRef RESULT_91_0_93_)
                        (portRef data0 (instanceRef I_36_1))
                        (portRef result0 (instanceRef I_36_3))
                    )
                )
                (net (rename RESULT_91_1_93_ "RESULT[1]")
                    (joined
                        (portRef RESULT_91_1_93_)
                        (portRef data1 (instanceRef I_36_1))
                        (portRef result1 (instanceRef I_36_3))
                    )
                )
                (net (rename RESULT_91_2_93_ "RESULT[2]")
                    (joined
                        (portRef RESULT_91_2_93_)
                        (portRef data2 (instanceRef I_36_1))
                        (portRef result2 (instanceRef I_36_3))
                    )
                )
                (net (rename RESULT_91_3_93_ "RESULT[3]")
                    (joined
                        (portRef RESULT_91_3_93_)
                        (portRef data3 (instanceRef I_36_1))
                        (portRef result3 (instanceRef I_36_3))
                    )
                )
            )
        )
    )
)
(design FIBEX
    (cellRef FIBEX (libraryRef FIBEX))
)
```

1.3.3 EDIF 3 0 0 Description

```
(edif fibex
    (edifVersion 3 0 0)
     (edifHeader
        (edifLevel 0)
        (keywordMap
            (k0KeywordLevel))
        (fontDefinitions)
        (physicalDefaults)
        (status
            (copyright (year 1998) "Altera Corporation")
            (comment "LPM Version 3 0 0 Example")
             (written
            (dataOrigin "Altera Corporation")
                (program "MAX+plus II 9.0")))
        (nameInformation
            (primaryName "fibex"))
        (physicalScaling
            (connectivityUnits
                (setTime (unitRef ns)))))
    (library fibex
        (libraryHeader
            (edifLevel 0)
            (nameCaseSensitivity)
            (technology
                (physicalScaling
                    (connectivityUnits
                        (setTime (unitRef ns))))
                (logicDefinitions
                    (setVoltage (unitRef mv))
                    (setCurrent (unitRef ua))
                    (logicValue L)
                    (logicValue H)
                    (logicValue X)
                    (logicValue Z))))
        (cell dff4
            (cellHeader
                 (nameInformation
                    (primaryName "dff4")))
            (cluster C1
                (interface (interfaceUnits)
                    (port CLOCK (inputPort)
                        (nameInformation
                            (primaryName "CLOCK")))
                    (port ASET (inputPort)
                        (nameInformation
                            (primaryName "ASET")))
                    (port DATA0 (inputPort)
                        (nameInformation
                            (pimaryName "DATA0"
                                (nameStructure
                                    (complexName "DATA"
```

```
                    (nameDimension
                        (nameDimensionStructure 0)))))))
    (port DATA1 (inputPort)
        (nameInformation
            (primaryName "DATA1"
                (nameStructure
                    (complexName "DATA"
                        (nameDimension
                            (nameDimensionStructure 1)))))))
    (port DATA2 (inputPort)
        (nameInformation
            (primaryName "DATA2"
                (nameStructure
                    (complexName "DATA"
                        (nameDimension
                            (nameDimensionStructure 2)))))))
    (port DATA3 (inputPort)
        (nameInformation
            (primaryName "DATA3"
                (nameStructure
                    (complexName "DATA"
                        (nameDimension
                            (nameDimensionStructure 3)))))))
    (portBundle DATA
        (portList
            (portRef DATA3)
            (portRef DATA2)
            (portRef DATA1)
            (portRef DATA0))
        (nameInformation
            (primaryName "DATA[3:0]"
                (nameStructure
                    (complexName "DATA"
                        (nameDimension
                            (nameDimensionStructure
                                (sequence 3 0))))))))
    (port Q0 (outputPort)
        (nameInformation
            (primaryName "Q0"
                (nameStructure
                    (complexName "Q"
                        (nameDimension
                            (nameDimensionStructure 0)))))))
    (port Q1 (outputPort)
        (nameInformation
            (primaryName "Q1"
                (nameStructure
                    (complexName "Q"
                        (nameDimension
                            (nameDimensionStructure 1)))))))
    (port Q2 (outputPort)
        (nameInformation
            (primaryName "Q2"
                (nameStructure
```

```
                        (complexName "Q"
                            (nameDimension
                                (nameDimensionStructure 2)))))))
                (port Q3 (outputPort)
                    (nameInformation
                        (primaryName "Q3"
                            (nameStructure
                                (complexName "Q"
                                    (nameDimension
                                        (nameDimensionStructure 3)))))))
                (portBundle Q
                    (portList
                        (portRef Q3)
                        (portRef Q2)
                        (portRef Q1)
                        (portRef Q0))
                    (nameInformation
                        (primaryName "Q[3:0]"
                            (nameStructure
                                (complexName "Q"
                                    (nameDimension
                                        (nameDimensionStructure
                                            (sequence 3 0)))))))))
                (clusterHeader
                    (property LPM_TYPE (string "LPM_FF"))
                    (property LPM_FFTYPE (string "DFF"))
                    (property LPM_Width (integer 4))
                    (property LPM_Avalue (integer 1)))))
        (cell addsub_4
            (cellHeader
                (nameInformation
                    (primaryName "addsub_4")))
            (cluster C1
                (interface (interfaceUnits)
                    (port DATAA0 (inputPort)
                        (nameInformation
                            (primaryName "DATAA0"
                                (nameStructure
                                    (complexName "DATAA"
                                        (nameDimension
                                            (nameDimensionStructure 0)))))))
                    (port DATAA1 (inputPort)
                        (nameInformation
                            (primaryName "DATAA1"
                                (nameStructure
                                    (complexName "DATAA"
                                        (nameDimension
                                            (nameDimensionStructure 1)))))))
                    (port DATAA2 (inputPort)
                        (nameInformation
                            (primaryName "DATAA2"
                                (nameStructure
                                    (complexName "DATAA"
                                        (nameDimension
```

```
                    (nameDimensionStructure 2)))))))
(port DATAA3 (inputPort)
    (nameInformation
        (primaryName "DATAA3"
            (nameStructure
                (complexName "DATAA"
                    (nameDimension
                        (nameDimensionStructure 3)))))))
(portBundle DATAA
    (portList
    (portRef DATAA3)
    (portRef DATAA2)
    (portRef DATAA1)
    (portRef DATAA0))
(nameInformation
    (primaryName "DATAA[3:0]"
        (nameStructure
            (complexName "DATAA"
                (nameDimension
                    (nameDimensionStructure
                        (sequence 3 0))))))))
(port DATAB0 (inputPort)
    (nameInformation
        (primaryName "DATAB0"
            (nameStructure
                (complexName "DATAB"
                    (nameDimension
                        (nameDimensionStructure 0)))))))
(port DATAB1 (inputPort)
    (nameInformation
        (primaryName "DATAB1"
            (nameStructure
                (complexName "DATAB"
                    (nameDimension
                        (nameDimensionStructure 1)))))))
(port DATAB2 (inputPort)
    (nameInformation
        (primaryName "DATAB2"
            (nameStructure
                (complexName "DATAB"
                    (nameDimension
                        (nameDimensionStructure 2)))))))
(port DATAB3 (inputPort)
    (nameInformation
        (primaryName "DATAB3"
            (nameStructure
                (complexName "DATAB"
                    (nameDimension
                        (nameDimensionStructure 3)))))))
(portBundle DATAB
    (portList
        (portRef DATAB3)
        (portRef DATAB2)
        (portRef DATAB1)
```

```
                (portRef DATAB0))
            (nameInformation
                (primaryName "DATAB[3:0]"
                    (nameStructure
                        (complexName "DATAB"
                            (nameDimension
                                (nameDimensionStructure
                                    (sequence 3 0))))))))
        (port RESULT0 (outputPort)
            (nameInformation
                (primaryName "RESULT0"
                    (nameStructure
                        (complexName "RESULT"
                            (nameDimension
                                (nameDimensionStructure 0)))))))
        (port RESULT1 (outputPort)
            (nameInformation
                (primaryName "RESULT1"
                    (nameStructure
                        (complexName "RESULT"
                            (nameDimension
                                (nameDimensionStructure 1)))))))
        (port RESULT2 (outputPort)
            (nameInformation
                (primaryName "RESULT2"
                    (nameStructure
                        (complexName "RESULT"
                            (nameDimension
                                (nameDimensionStructure 2)))))))
        (port RESULT3 (outputPort)
            (nameInformation
                (primaryName "RESULT3"
                    (nameStructure
                        (complexName "RESULT"
                            (nameDimension
                                (nameDimensionStructure 3)))))))
        (portBundle RESULT
            (portList
                (portRef RESULT3)
                (portRef RESULT2)
                (portRef RESULT1)
                (portRef RESULT0))
            (nameInformation
                (primaryName "RESULT[3:0]"
                    (nameStructure
                        (complexName "RESULT"
                            (nameDimension
                                (nameDimensionStructure
                                    (sequence 3 0)))))))))
        (clusterHeader
                (property LPM_TYPE (string "LPM_ADD_SUB"))
                (property LPM_Width (integer 4)))))
(cell fibex
    (cellHeader
```

```
        (nameInformation
            (primaryName "fibex")))
    (cluster C1
        (interface (interfaceUnits)
            (port CLOCK (inputPort)
                (nameInformation
                    (primaryName "CLOCK")))
            (port CLEAR (inputPort)
                (nameInformation
                    (primaryName "CLEAR")))
            (port RESULT0 (bidirectionalPort)
                (nameInformation
                    (primaryName "RESULT0"
                        (nameStructure
                            (complexName "RESULT"
                                (nameDimension
                                    (nameDimensionStructure 0)))))))
            (port RESULT1 (bidirectionalPort)
                (nameInformation
                    (primaryName "RESULT1"
                        (nameStructure
                            (complexName "RESULT"
                                (nameDimension
                                    (nameDimensionStructure 1)))))))
            (port RESULT2 (bidirectionalPort)
                (nameInformation
                    (primaryName "RESULT2"
                        (nameStructure
                            (complexName "RESULT"
                                (nameDimension
                                    (nameDimensionStructure 2)))))))
            (port RESULT3 (bidirectionalPort)
                (nameInformation
                    (primaryName "RESULT3"
                        (nameStructure
                            (complexName "RESULT"
                                (nameDimension
                                    (nameDimensionStructure 3)))))))
            (portBundle RESULT
                (portList
                    (portRef RESULT3)
                    (portRef RESULT2)
                    (portRef RESULT1)
                    (portRef RESULT0))
                (nameInformation
                    (primaryName "RESULT[3:0]"
                        (nameStructure
                        (complexName "RESULT"
                            (nameDimension
                                (nameDimensionStructure
                                    (sequence 3 0)))))))))
            (clusterHeader)
                (connectivityView VIEW1
                    (connectivityViewHeader (connectivityUnits))
```

```
(logicalConnectivity
    (instance I1
        (clusterRef C1 (cellRef dff4))
        (nameInformation
            (primaryName "I1")))
    (instance I2
        (clusterRef C1 (cellRef dff4))
        (nameInformation
            (primaryName "I2")))
    (instance I3
        (clusterRef C1 (cellRef addsub_4))
        (nameInformation
            (primaryName "I3")))
    (signal CLOCK
        (signalJoined
            (portInstanceRef CLOCK (instanceRef I1))
            (portInstanceRef CLOCK (instanceRef I2))
            (portRef CLOCK)))
    (signal CLEAR
        (signalJoined
            (portInstanceRef ASET (instanceRef I1))
            (portInstanceRef ASET (instanceRef I2))
            (portRef CLEAR)))
    (signal LAST0
        (signalJoined
            (portInstanceRef Q0 (instanceRef I1))
            (portInstanceRef DATA0 (instanceRef I2))
            (portInstanceRef DATAB0 (instanceRef I3))))
    (signal LAST1
        (signalJoined
            (portInstanceRef Q1 (instanceRef I1))
            (portInstanceRef DATA1 (instanceRef I2))
            (portInstanceRef DATAB1 (instanceRef I3))))
    (signal LAST2
        (signalJoined
            (portInstanceRef Q2 (instanceRef I1))
            (portInstanceRef DATA2 (instanceRef I2))
            (portInstanceRef DATAB2 (instanceRef I3))))
    (signal LAST3
        (signalJoined
            (portInstanceRef Q3 (instanceRef I1))
            (portInstanceRef DATA3 (instanceRef I2))
            (portInstanceRef DATAB3 (instanceRef I3))))
    (signalGroup LAST
        (signalList
            (signalRef LAST0)
            (signalRef LAST1)
            (sinalRef LAST2)
            (signalRef LAST3)))
    (signal PRESENT0
        (signalJoined
            (portInstanceRef Q0 (instanceRef I2))
            (portInstanceRef DATAA0 (instanceRef I3))))
    (signal PRESENT1
```

```
                    (signalJoined
                        (portInstanceRef Q1 (instanceRef I2))
                        (portInstanceRef DATAA1 (instanceRef I3))))
                (signal PRESENT2
                    (signalJoined
                        (portInstanceRef Q2 (instanceRef I2))
                        (portInstanceRef DATAA2 (instanceRef I3))))
                (signal PRESENT3
                    (signalJoined
                        (portInstanceRef Q3 (instanceRef I2))
                        (portInstanceRef DATAA3 (instanceRef I3))))
                (signalGroup PRESENT
                    (signalList
                        (signalRef PRESENT0)
                        (signalRef PRESENT1)
                        (signalRef PRESENT2)
                        (signalRef PRESENT3)))
                (signal RESULT0
                    (signalJoined
                        (portInstanceRef DATA0 (instanceRef I1))
                        (portInstanceRef RESULT0 (instanceRef I3))
                        (portRef RESULT0)))
                (signal RESULT1
                    (signalJoined
                        (portInstanceRef DATA1 (instanceRef I1))
                        (portInstanceRef RESULT1 (instanceRef I3))
                        (portRef RESULT1)))
                (signal RESULT2
                    (signalJoined
                        (portInstanceRef DATA2 (instanceRef I1))
                        (portInstanceRef RESULT2 (instanceRef I3))
                        (portRef RESULT2)))
                (signal RESULT3
                    (signalJoined
                        (portInstanceRef DATA3 (instanceRef I1))
                        (portInstanceRef RESULT3 (instanceRef I3))
                        (portRef RESULT3)))
                (signalGroup RESULT
                    (signalList
                        (signalRef RESULT0)
                        (signalRef RESULT1)
                        (signalRef RESULT2)
                        (signalRef RESULT3))))
            (connectivitystructure)))))

    (design fibex
        (cellRef fibex
            (libraryRef fibex))
        (designHeader
            (designUnits))))
```