1. INSTANTIATING LPM in VHDL

To promote LPM usage in VHDL design community, this section describes the syntax for instantiating LPM in VHDL design file.

1.1 COMPONENT DECLARATION

To instantiate component in VHDL design file, the component has to be declared before use. The component declaration of LPM modules is defined in the LPM package file in Support Files section later in this document. In declaring the LPM module, the component should be "fully described". Which includes all the optional ports, parameters. Once defined, any number of these "fully described components" can be instantiated within the VHDL design. For example, LPM_MULT is declared as the follow:

```
component LPM_MULT
    generic (LPM_WIDTHA : positive;
            LPM_WIDTHB : positive;
            LPM_WIDTHS : positive;
            LPM_WIDTHP : positive;
            LPM_REPRESENTATION : string := "UNSIGNED";
            LPM_PIPELINE : integer := 0;
            LPM_TYPE: string := L_MULT;
            LPM_HINT : string := UNUSED);
    port    (DATAA : in std_logic_vector(LPM_WIDTHA-1 downto 0);
            DATAB : in std_logic_vector(LPM_WIDTHB-1 downto 0);
            ACLR : in std_logic := '0';
            CLOCK : in std_logic := '0';
            CLKEN : in std_logic := '0';
            SUM: in std_logic_vector(LPM_WIDTHS-1 downto 0) := (OTHERS => '0');
            RESULT : out std_logic_vector(LPM_WIDTHP-1 downto 0));
end component;
```

1.2 COMPONENT INSTANTIATION

1.2.1 Port

All the used port connections are defined in port map construct of VHDL. The unused optional ports were left out from the port map and its' default value from the component declaration will be used. For example, the u1 instance in this example only use aset optional port of LPM_FF so other unused optional ports were left our from the port map statement.

```
u1: lpm_ff
    PORT MAP (data => result, clock =>clock, aset => clear, q => last);
```

1.2.2 Property

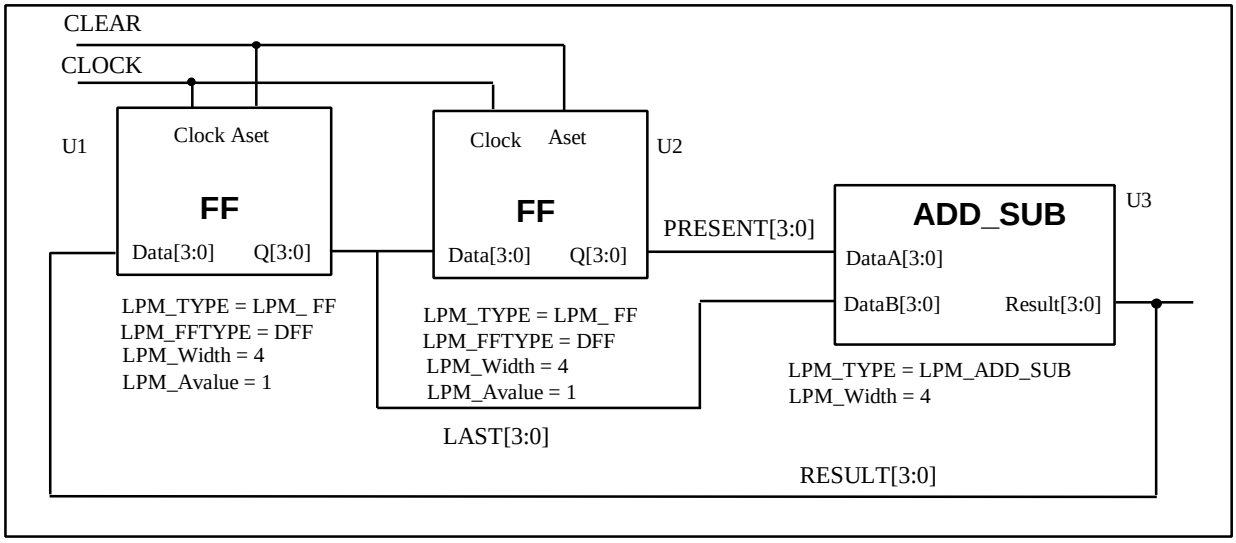
All the used LPM properties values are defined in generic map construct of VHDL. The unused optional properties were left out and its' default value from the component declaration will be used. For example, the u1 instance in this example is a 4-bits DFF with no synchronous set value (ie. LPM_SVALUE) so the LPM_SVALUE is left out from the generic map statement.

```
u1: lpm_ff
   GENERIC MAP (LPM_WIDTH => 4, LPM_AVALUE =>"0001")
```

1.3 EXAMPLE

1.3.1 Schematic description

The schematic example is shown in the following figure.



1.3.2 VHDL description

```
-- Description: LPM instantiation
 --

LIBRARY ieee;
 USE ieee.std_logic_1164.all;
 LIBRARY lpm;
 USE lpm.lpm_components.all;

 ENTITY fibex is
    PORT ( clock : in std_logic;
```

```
                clear : in std_logic;
                result :   buffer std_logic_vector (3 downto 0));
END fibex;

ARCHITECTURE lpm OF fibex IS
   SIGNAL last  : std_logic_vector (3 downto 0);
   SIGNAL present : std_logic_vector (3 downto 0);

BEGIN

  u1: lpm_ff
     GENERIC MAP (lpm_width => 4, lpm_avalue => "0001")
     PORT MAP (data => result, clock =>clock, aset => clear, q => last);

  u2: lpm_ff
     GENERIC MAP (lpm_width => 4, lpm_avalue => "0001")
     PORT MAP (data => last, clock =>clock, aset => clear, q => present);

  u3: lpm_add_sub
     GENERIC MAP (lpm_width  => 4)
     PORT MAP (dataa => present, datab => last, result => result);

END lpm
```