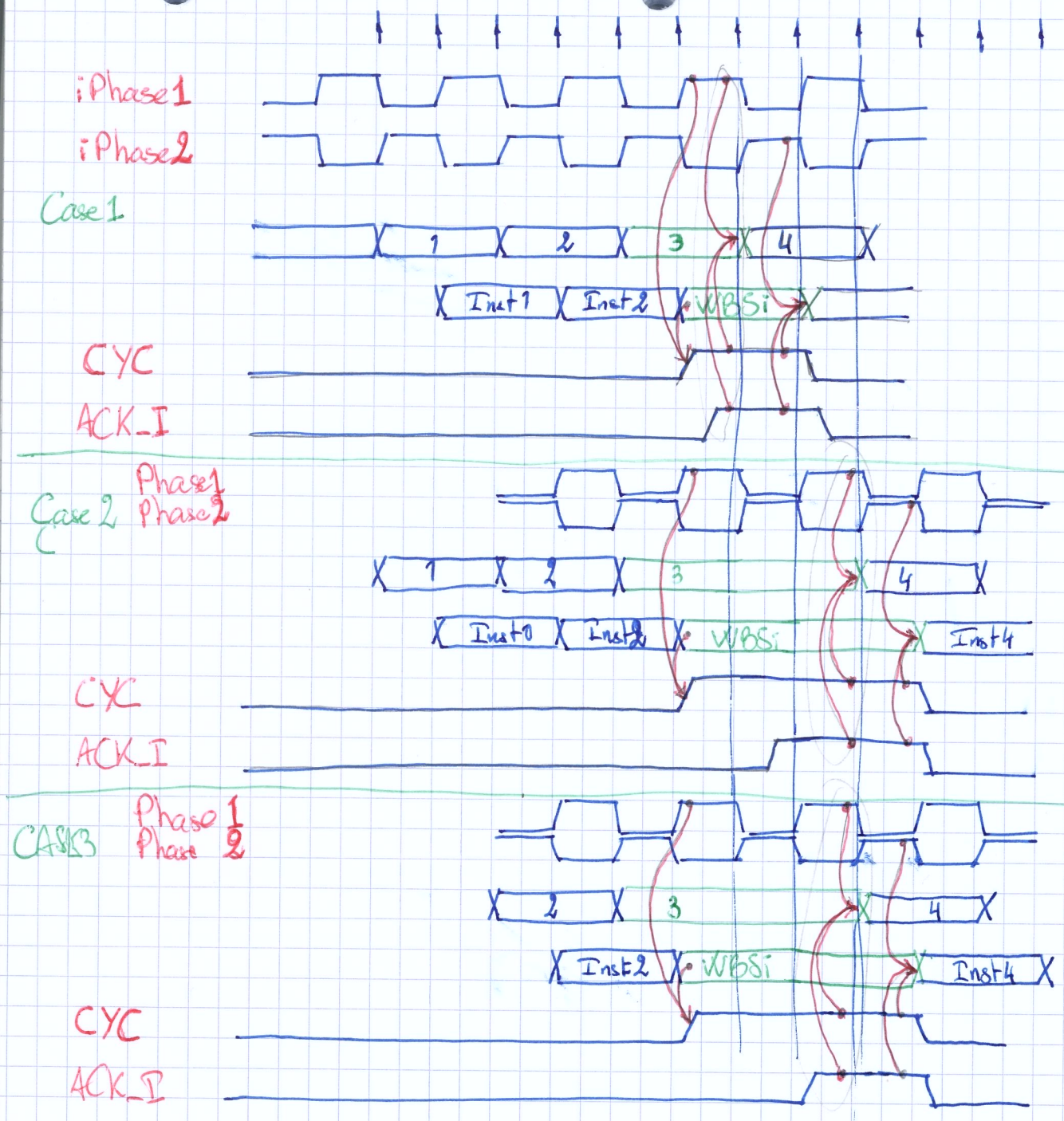
Wishbone Mode Asychrone



WB_vHs ⇐ CYC & ACK_I

- CYC : set (asynchrone) iPhase1 & WBSi
  : reset iPhase2 & WB_vHs
- PC : if (CYC) ⇐ iPhase1 & WBSi
  else ⇐ iPhase1

WB_validHandshake ⇐ CYC & ACK_I
(WB_vHs)

WB_valid PC ⇐ WB_vHs & iPhase1
(WB_vPC)

WB_valid Operation ⇐ (WB_vPC)$_{-1}$

- CYC (asynchrone)
  - set: iPhase1 & WBSi
  - reset: iPhase2 & WB_vOp
- PC if (CYC) ⇐ iPhase1 & WB_vHs
  else ⇐ iPhase1