DATA SHEET

Development Interface

Introduction

The Development Interface is used for development purposes (Boundary Scan testing, debugging, program flow tracking, etc.). It is an interface between the OpenRISC, peripheral cores, and any free (GDB) or commercial debugger/emulator or BS testing device. The external debugger or BS tester connects to the core via a JTAG port that is fully IEEE 1149.1 compatible. The Development Interface also contains a trace buffer and support for tracing the program flow, execution coverage, and profiling the code.

Features

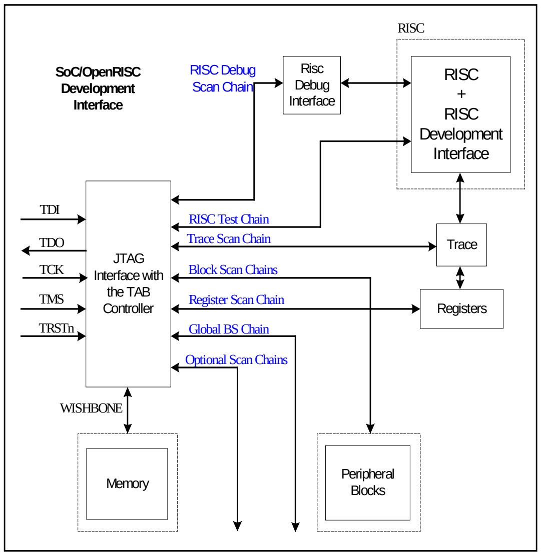

Figure 1: Soc/OpenRISC Development Interface

The Development Interface provides the following features:

- Direct internal signal monitoring (no need for additional software)
- IEEE 1149.1 compatible TAP controller that supports all IEEE 1149.1 basic functions and more
- Boundary Scan Testing (additional BS equipment that connects to the JTAG pins is needed)
- Program Trace incorporated for program flow monitoring
- OpenRISC debug interface
- WISHBONE interface

General Description

Architecture

Figure 1 above shows the general architecture of the Ethernet IP core. It consists of several building blocks:

- JTAG interface with the TAP controller
- RISC debug interface
- Trace
- Trace registers
- WISHBONE interface
- Several scan chains
- Boundary Scan (BS) cells (not in the figure)

JTAG Interface with TAP Controller

The JTAG interface with TAP controller is a fully IEEE 1149.1 std. compliant interface that supports all by standard requested commands plus some additional ones. The controller with the interface is one of the basic components of the development system. A device running the BS, trace, or debugging software connects to the development interface through the five JTAG pins. The controller is connected to several scan chains that are selectable through one of the additional commands.

RISC Debug Interface

The SoC development interface connects to the RISC development interface (which is part of the RISC) through the RISC debug scan chain. The complete control of the RISC is achieved by using this scan chain (setting watchpoints, breakpoints, registers, etc.).

Trace

The trace is used for tracking the program flow. This is especially useful when the RISC uses caches and the program is not necessarily executed serially. The trace has a large number of different modes to meet all needs a user might have:

- Option to change sample structure on-the-fly
- Normal mode (RISC is stopped when the buffer is full)
- Continuous mode (old samples are overwritten)
- Post event recording (recording starts after a certain event)
- Prior event recording (recording stops after a certain event)
- Post-prior event recording (recording occurs between two events)

If required, the RISC stalls automatically. When running resumes, no action needs to be taken as the RISC recommences exactly from where it stopped.

Boundary Scan (BS) Testing

Except for the BS scan chain, the Development Interface contains everything needed for BS testing. To complete this chain, the ASIC needs to be finished and the pin number determined. One of the commercial BS testers might be connected to the Development Interface for the purpose of BS testing.

WISHBONE Interface

The WISHBONE interface connects the Development Interface to external memory. The core is WISHBONE SoC Interconnection specification Rev. B compliant. The implementation realizes a 32-bit bus width and does not support other bus widths. Other cores linked to the WISHBONE can also be connected to the Development Interface by using the same interface.

Utilization

The following table lists the core’s intended applications.

Core	FPGA Size	Silicon Area	Speed	Power Consumption
	TBD	TBD	TBD	TBD

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