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DMT Transceiver
Free Core
Specification

Part 1: Modem

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Revision History

Rev.	Date	Author	Description
0.1	16.05.04	Günter Dannoritzer	First Draft

Contents

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Introduction

The ITU-T recommendation G.992.1 describes the requirements for Asymmetric Digital Subscriber Line (ADSL) transceivers. The used channel coding method for ADSL is Discrete Multi Tone Modulation (DMT).

The DMT transceiver is a free core implementation of the building blocks as described in ITU-T recommendation G.992.1. The core is subdivided into the modules error correction, modulation, demodulation, and handshake controller.

This document is part 1 of the design and specifies the modulator and demodulator building blocks.

On the transmitter side this includes the functional blocks:

· Constellation encoder

· Gain

· IDFT

· Add cyclic prefix

On the receiver side:

· TDQ

· Remove cyclic prefix

· DFT

· Constellation decoder

Recommendation G.992.1 allows an optional trellis coding to be included in the constellation encoder. This version **does not** included this feature.

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Architecture

This section describes the architecture of the DMT modem.

Modulator

The following figure provides a view of the modulator in the transmitter. It consists out of the constellation encoder, the gain, the IDFT, and the cyclic prefix.
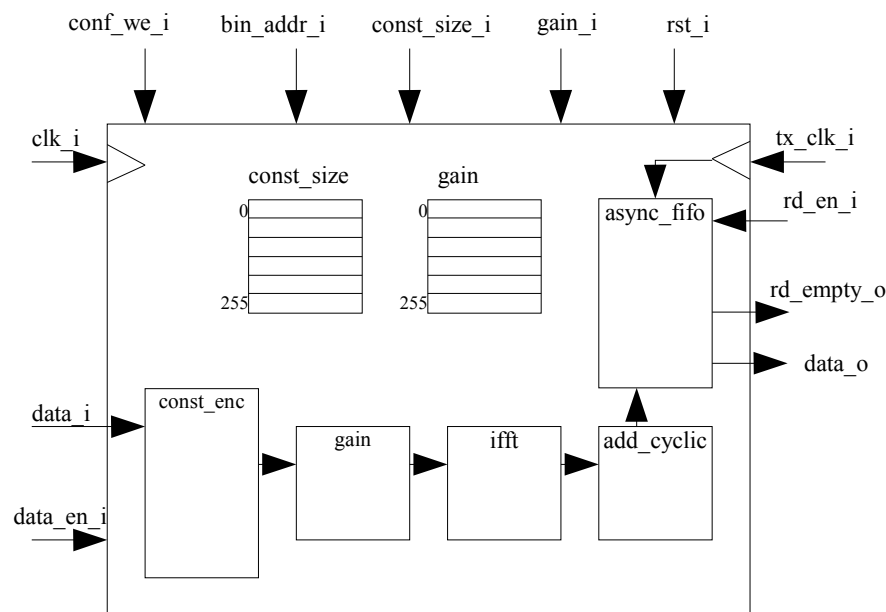

Figure 1: DMT Modulator, dmt_mod

The following figure provides a view of the demodulator in the receiver, containing the TDQ, the cyclic prefix, the DFT, and the constellation decoder.

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Operation

This section describes the operation of the DMT modem.

Modulator

Reset

Setting rst_i to '1' results in reset of the internal logic. This includes setting the 256 gain registers and 256 constellation size registers (const_size) to zero.

Configuration

The configuration process includes the setting of the constellation size registers and the gain registers for the 256 bins. This configure mode is achieved by setting config_we_i = '1' and data_en_i = '0'.

On the rising edge of the clk_i signal the system samples the bin_addr_i, const_size_i, and gain_i values. The bin_addr_i specifies for which bin the const_size_i and gain_i values should be stored. Note that the values are always stored as a pair. The configuration process overwrites old values.

Data processing

The data processing mode is the normal operation mode. This mode is achieved my setting data_en_i = '1' and config_we_i = '0'.

Data from data_i is sampled at the rising edge of the clock, processed and put into the asynchronous output FIFO. The availability of data in the FIFO is signaled through the rd_empty_o signal going low.

Output data are clocked out with rising edge of the tx_clk_i signal when the rd_en_i signal is high.

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Registers

This section specifies all internal registers.

List of Modulator Registers

Name	Address	Width	Access	Description
const_size	0..255	4	W	Stores the constellation size for each bin as unsigned integer.
gain	0..255	12	W	Stores the gain value for each bin. Value is a 12-bit unsigned fixed-point fractional number with bits 11:9 the integer part and bits 8:0 the fractional part.

Table 1: List of modulator registers

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Clocks

Modulator

This section specifies all the clocks. All clocks, clock domain passes and the clock relations should be described.

Name	Source	Rates (MHz)			Remarks	Description
		Max	Min	Resolution		
clk_i	Input					For external interface.
tx_clk_i	Input					Clock signal for the output data.

Table 2: List of Modulator clocks

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IO Ports

Modulator

This section specifies the modulator core IO ports.

Port	Width	Direction	Description
clk_i	1	Input	Clock input
rst_i	1	Input	Reset input
data_en_i	1	Input	Enables the data processing mode.
data_i	15	Input	Input data to the modulator core.
conf_we_i	1	Input	Enables the configuration mode.
bin_addr_i	8	Input	Addresses the bin configuration.
const_size_i	4	Input	Constellation size for the addressed bin.
gain_i	12	Input	Gain value for the addressed bin.
tx_clk_i	1	Input	Clock signal for the output data
rd_en_i	1	Input	Enables reading out data
rd_empty_o	1	Output	Signals empty output FIFO
data_o	16	Output	Output data from the modulator core.

Table 3: List of Modulator IO ports

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Device utilization

Modulator

The following table shows device utilization results.

Device	Slices	Slices Flip-Flop	4-input LUT	$f_{(MAX)}$[MHz]
TBD	TBD	TBD	TBD	TBD

Table 4: Modulator device utilization

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This section contains an alphabetical list of helpful document entries with their corresponding page numbers.