Tone Ordering and Constellation Encoder Specification

Günter Dannoritzer
dannoritzer@opencores.org

July 9, 2007

1 Introduction

The Tone Ordering and Constellation Encoder core implements the tone ordering and constellation encoding as described in ADSL recommendation ITU G.992.1.

2 Architecture

The core consists out of the tone ordering block, the constellation encoder block, and the controller block.

Figure 1 on page 3 shows the architecture of the Tone Ordering and Constellation Encoder core. Data entering the tone ordering block one byte at a time are stored in FIFOs. There is a FIFO for the fast path and one for the interleaved path. Data can be written to the two FIFOs simultaneously.

Each carrier can be loaded with 2-15 bits, with the data from the fast path being assigned first to carriers followed by the data from the interleaved path.

The amount of bits in the fast path does not necessarly match on a carrier boundary, so there might be one carrier that holds bits from the fast path and the interleaved path. Here comes the information about the number of bits from the fast path in. After this amount of bits has been assigned, the bit extraction switches from the fast path FIFO to the interleaved path FIFO and bits are now assigned from the interleaved path shift register until the bit loading table is processed to the end.

Now the processing starts again by switching back to the fast path shift register and processing the bit loading table from beginning.

The processing can only start if enough bytes are in the FIFO to fill the first carrier. The controller block watches over this and if enough bytes are in the FIFO one or two bytes are copied to the shift register. After that the shift register will shift out the amount of bits for the first carrier. Now it depends on the amount of bits needed for the next carrier how many bytes need to get copied out of the FIFO into the shift register. After shifting out the fast path bits, data from the interleaved path are used to fill the register for the constellation encoder input.

From the shift registers the bits are shifted into a 15 bits wide register. After all bits for a carrier are shifted into that register, the data are loaded into the constellation encoder block.

The constellation encoder puts out the result of the constellation encoding, which is the result of the top core.

3 Operation

3.1 Reset

Performing a reset will reset all internal state machines and set all registers to 0. After a reset the core needs to be configured for proper operation.

3.2 Configuration

The configuration requires the setting of bit loading per carrier and how many bits are assigned to the fast path.

The core has two register sets for the bit loading. The first register set holds the number of bits per carrier and the second register set the carrier number. Tone ordering is done by assigning the first data bits to carriers with the lower number of bits. The core handles this ordering by having a register set configured in the order the bits are to be assigned. After the configuration the core just processes the register list in ascending order. As not all carrier will be used, there is an additional register that specifies how many registers of the list should be processed.

Finally the number of bits in the fast path have to be configured. Now the core is ready to process data.

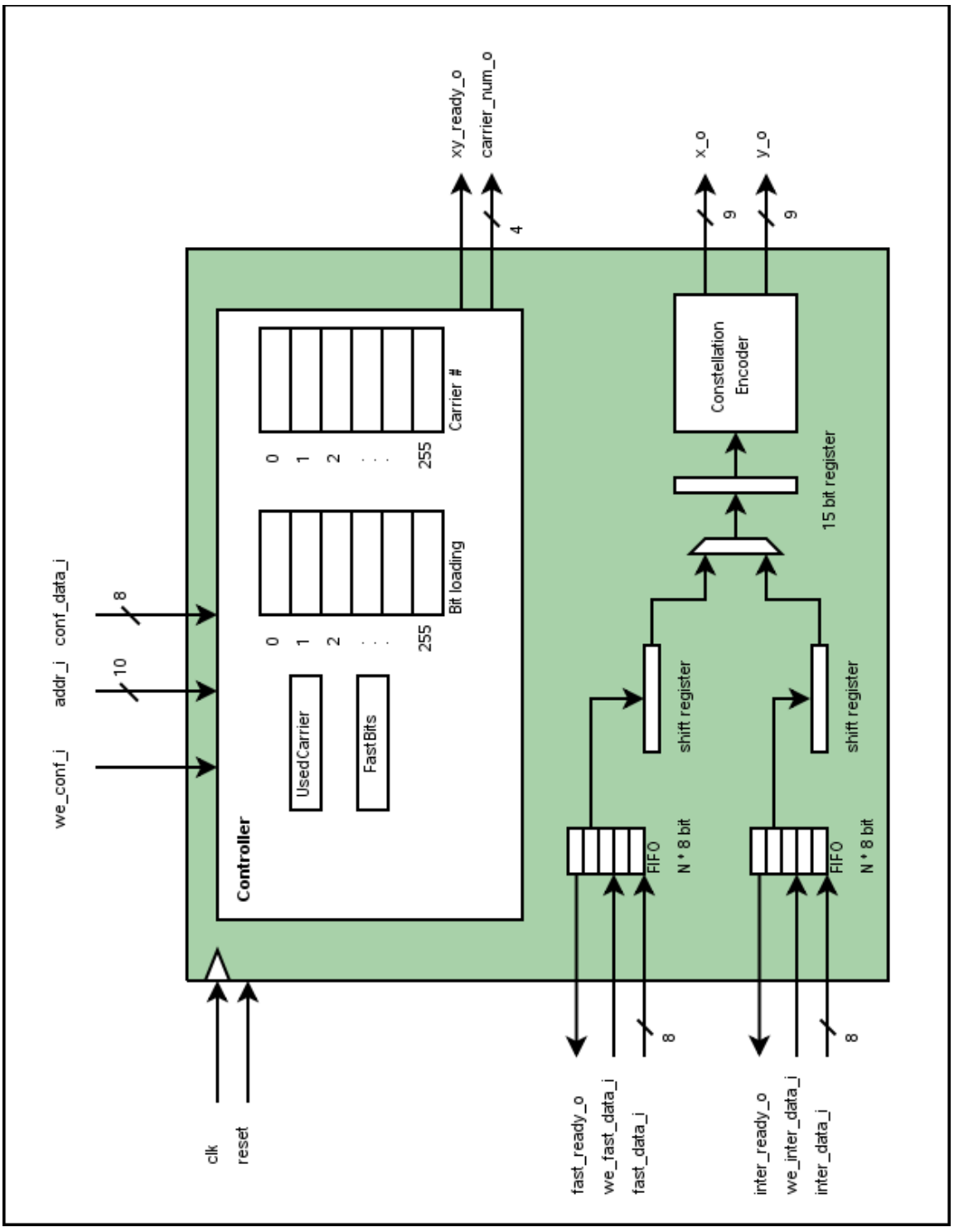

Figure 1: Architecture

3.3 Data Processing

There are two FIFO buffered data input interfaces. One for data of the fast path and one for data of the interleaved path.

If a data input interface is ready for accepting data, it is signalling that via the ready output. The core takes data in 1 byte groups and stores them in a FIFO. To write data to the data input the write enable signal needs to be asserted and the valid data are entered into the FIFO with the next raising edge of the clk signal.

Once enough data are entered to encode the first carrier, as specified in the bit loading table, data are extracted and passed to the constellation encoder. The output of the encoder is passed along with the carrier number as output of the core.

4 Registers

Table 1 lists the registers which are accessible over the address and configuration data bus.

Name	Address	Width	Access	Description
BitLoading	0x000 - 0x0FF	4	W	Specifies how many bits a carrier is loaded with
CarrierNumber	0x100 - 0x1FF	8	W	Specifies the carrier number
UsedCarrier	0x200	8	W	How many of the BitLoading and CarrierNumber registers are filled with information
FastBits	0x201	8	W	How many bits are used for the fast path

Table 1: List of registers

4.1 BitLoading

The BitLoading register is of size 256*4 bits and only writeable. It lists the amount of bits to be loaded on a carrier. The core will process the list in ascending order, so the registers need to be configured in the way the tone ordering should be performed. That means carriers with the least amount of non-zero bits have to be written first into the registers. The stored information is only meaningful in connection with the CarrierNumber registers.

4.2 CarrierNumber

The information of the CarrierNumber registers are tight to the BitLoading registers by the register number. For example, BitLoading register 0 at address 0x000 specifies the amount of bits loaded onto the carrier, specified in CarrierNumber register 0 at address 0x100.

4.3 UsedCarriers

Although ADSL supports 256 carriers, not all of them will be loaded with bits. As the BitLoading and the CarrierNumber registers are storing the information in ordered form, only the first n of 256 registers will be filled with information and need to be processed by the tone ordering and constellation encoder. The UsedCarriers register specified how many of those registers need to be processed.

4.4 FastBits

The FastBits register specifies how many bits from the fast path are shifted into the constellation encoder. After this amount of bits are shifted out, the multiplexer is switched and data are shifted from the interleaved path.

5 Interface Description

Table 2 on the following page shows the I/O port configuration of the Core.

6 Synthesis Results

Table 3 on the next page lists some synthesis results.

7 Revision History

Rev.	Date	Author	Description
0.1	09.07.2007	GAD	First draft

Port	Width	Direction	Description
clk	1	Input	Clock input
reset	1	Input	Reset the block
fast_ready_o	1	Output	Fast path FIFO is ready to receive data
we_fast_data_i	1	Input	Write enable for fast path data
fast_data_i	8	Input	Fast path data
inter_ready_o	1	Output	Interleaved path FIFO is ready to receive data
we_inter_data_i	1	Input	Write enable for interleaved path data
inter_data_i	8	Input	Interleaved path data
addr_i	10	Input	Address for configuration registers
we_conf_i	1	Input	Write enable for configuration data
conf_data_i	8	Input	Configuration data
xy_ready_o	1	Output	Signal that the X and Y output values are valid
carrier_num_o	4	Output	Specify the carrier number for which the X and Y output values are
x_o	9	Input	X output value of the constellation encoder
y_o	9	Input	Y output value of the constellation encoder

Table 2: List of I/O Ports for the Tone Ordering and Constellation Encoder Core

Vendor	Family	Device	Resource usage	Max. Clock speed
Xilinx				

Table 3: Synthesis results for Core