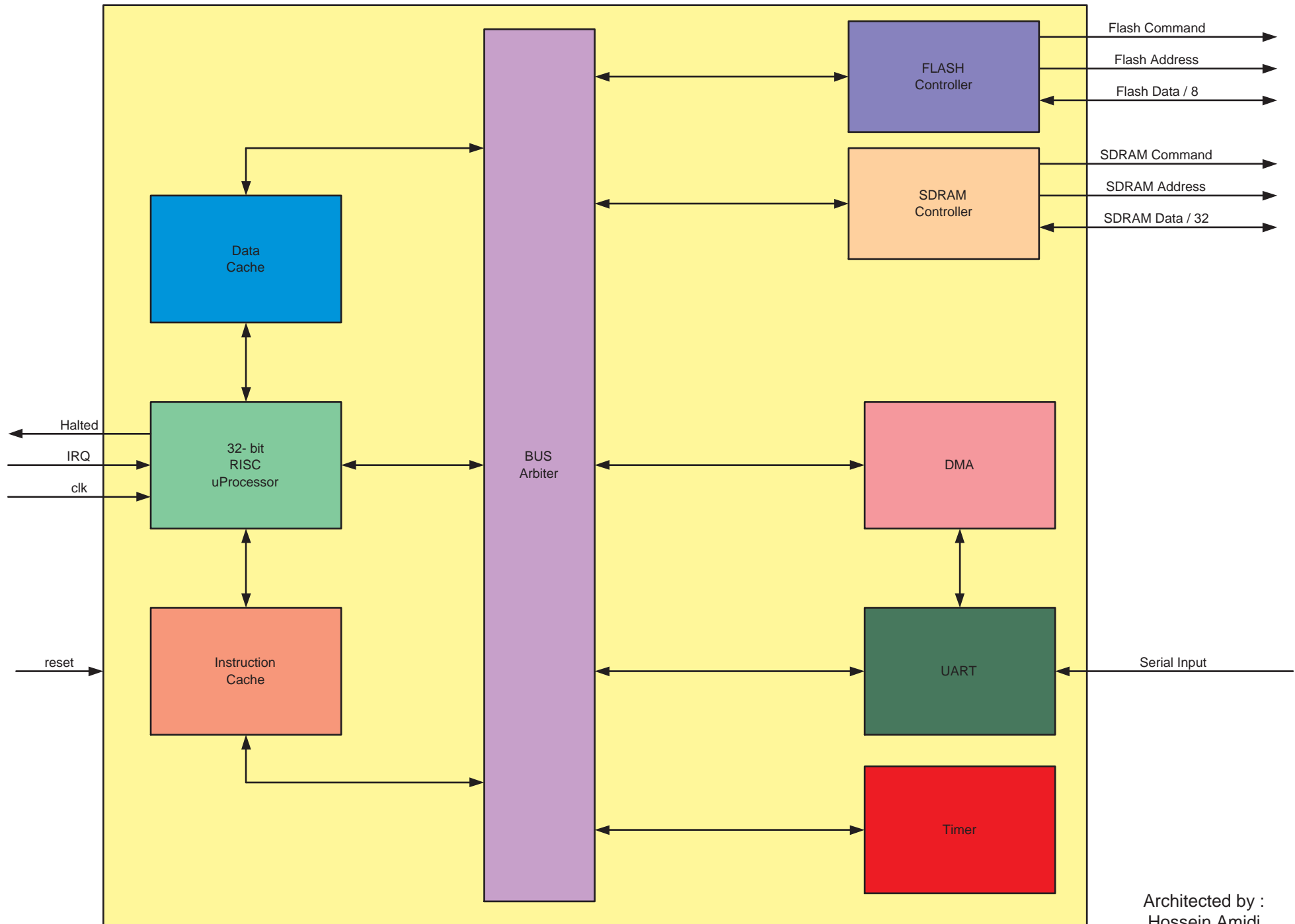
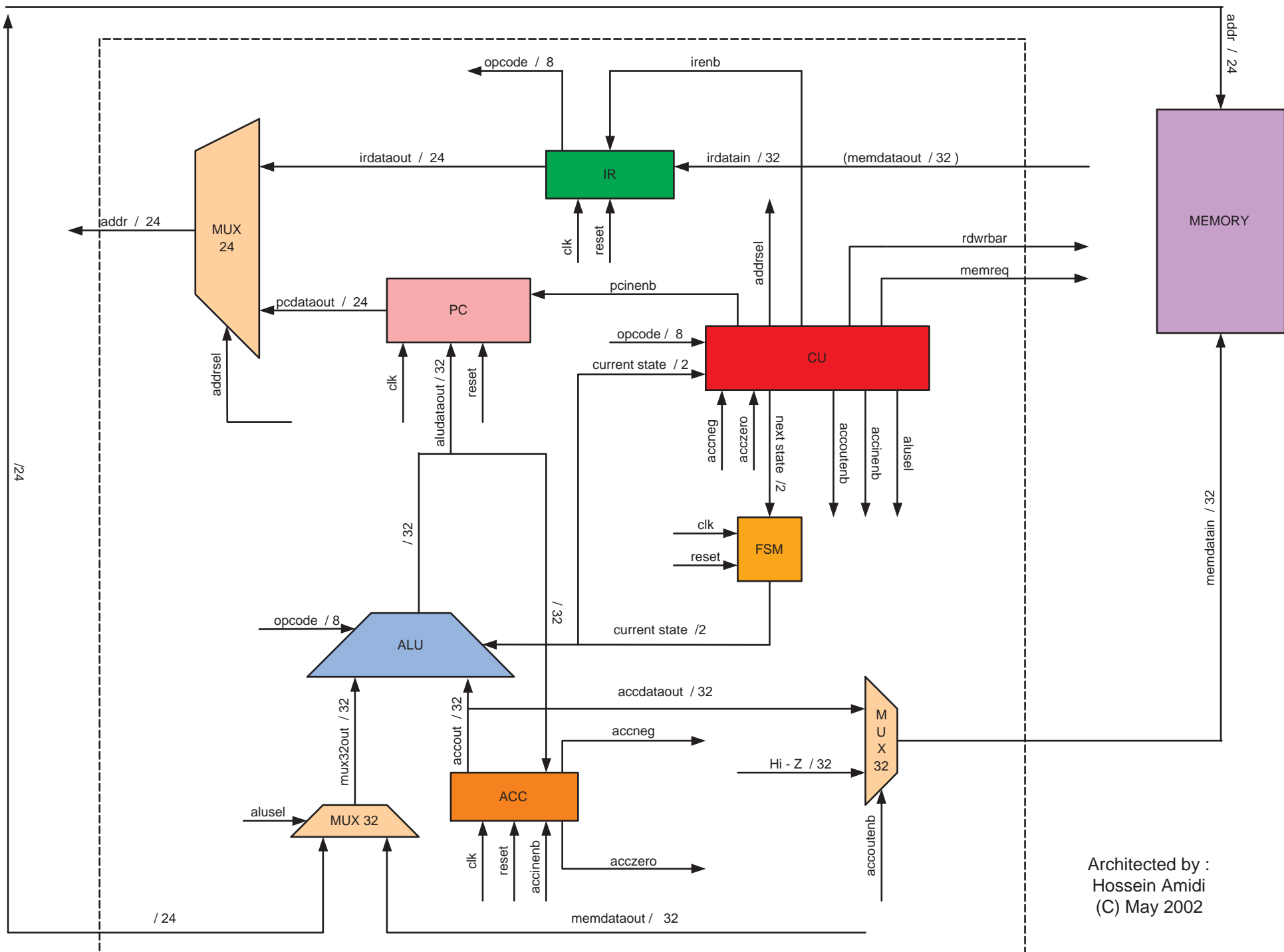


System On a Chip

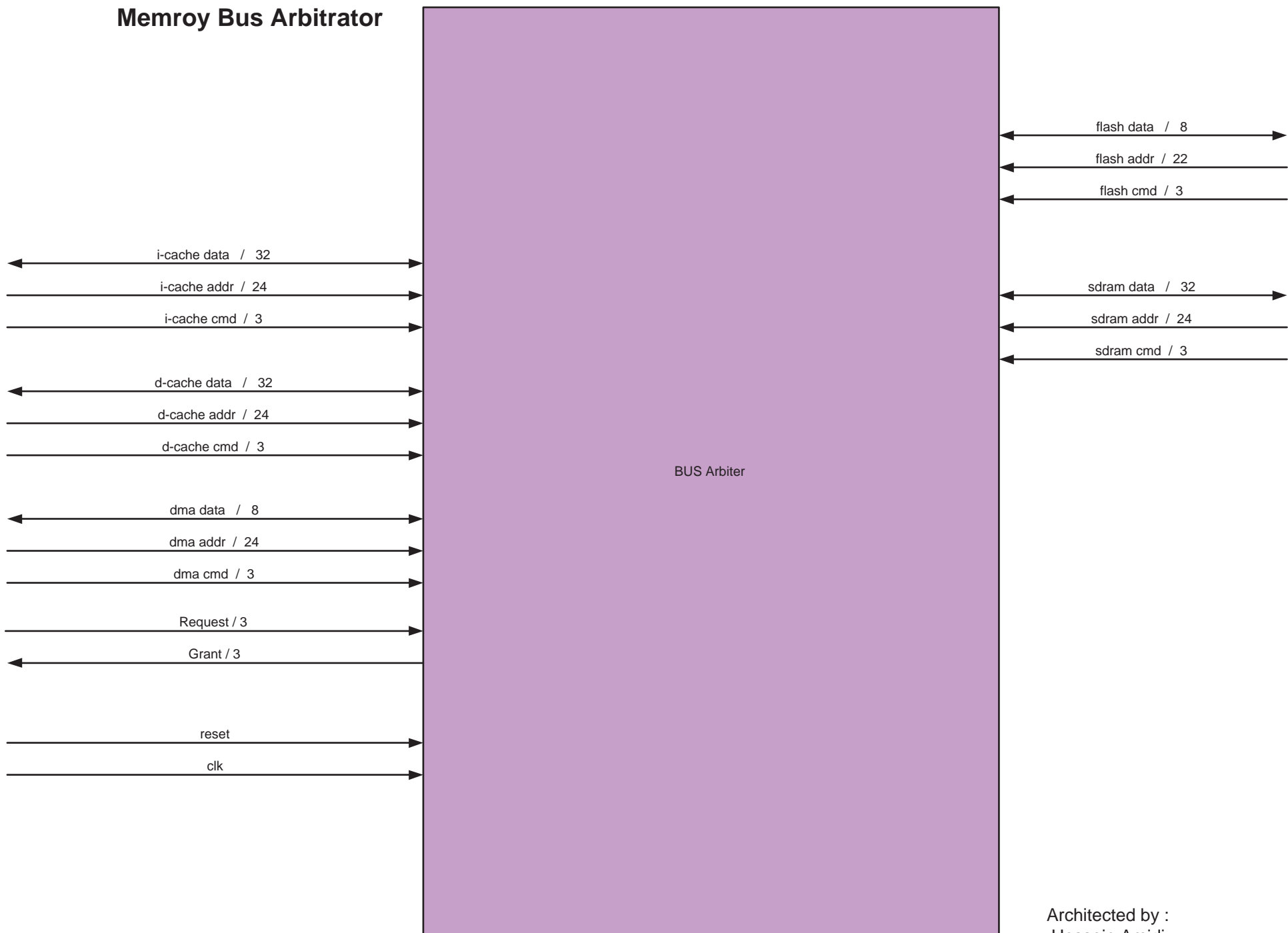


32-bit uRISC Processor



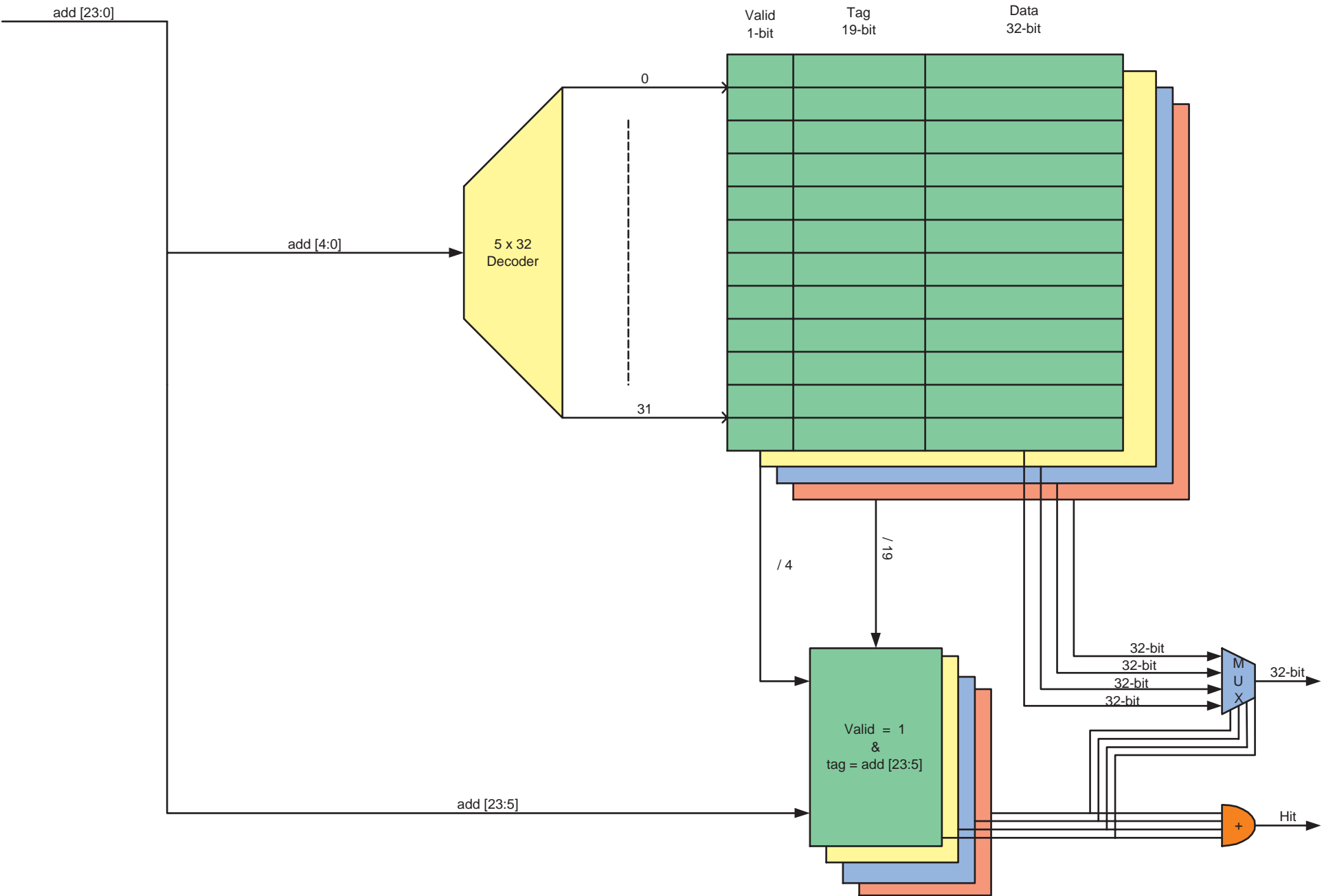
Architected by :
 Hossein Amidi
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Memroy Bus Arbitrator

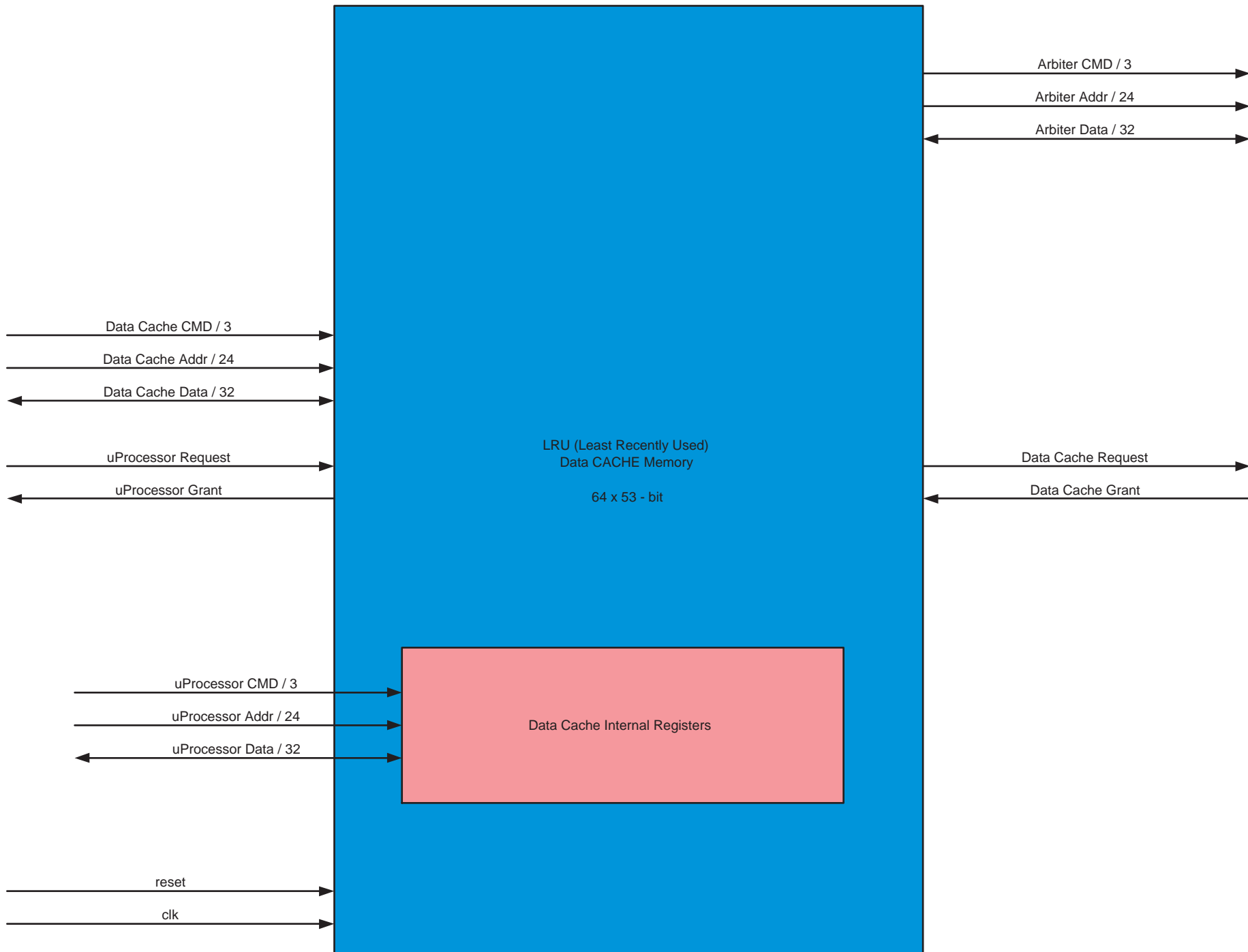


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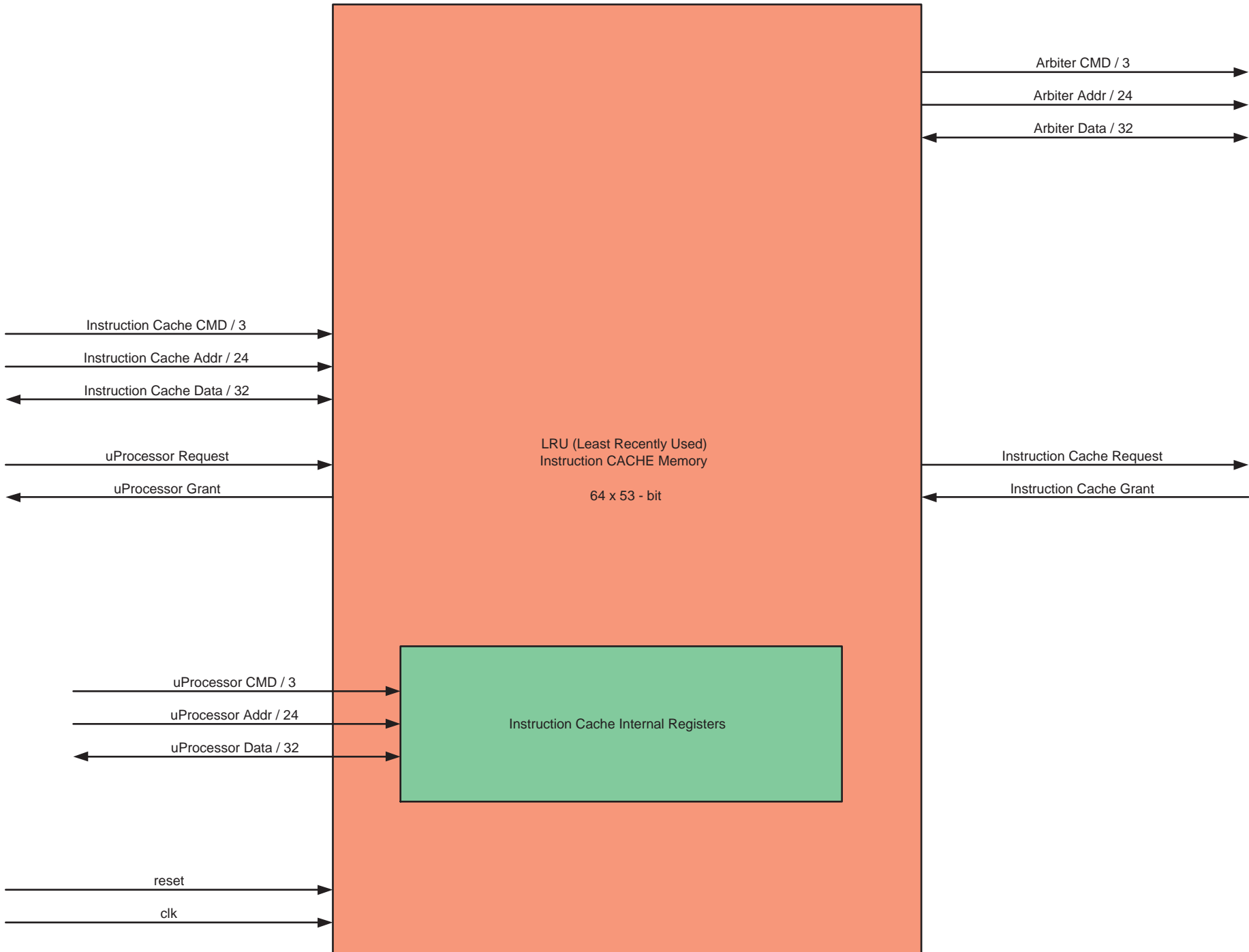
4-Way LRU Cache



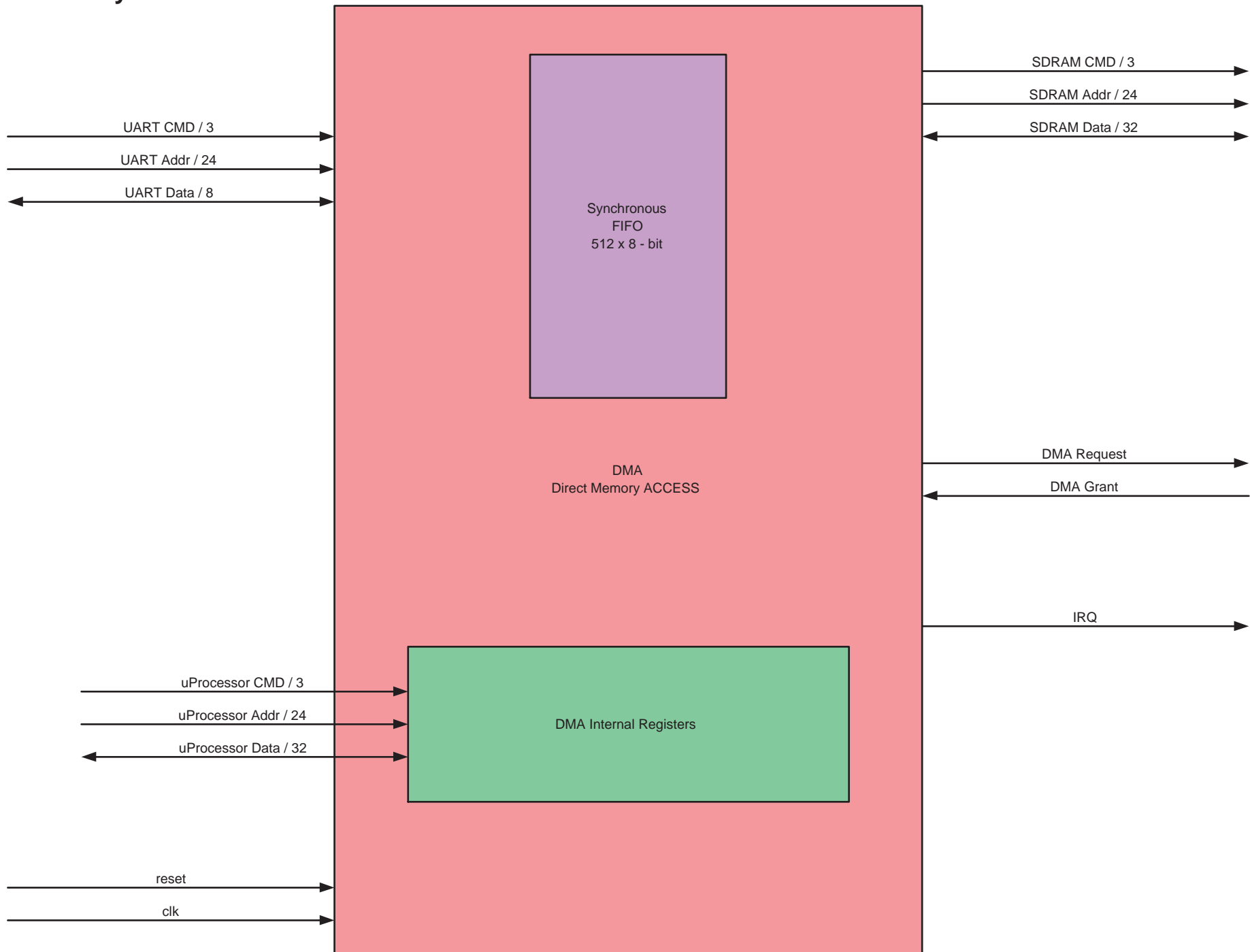
Data Cache



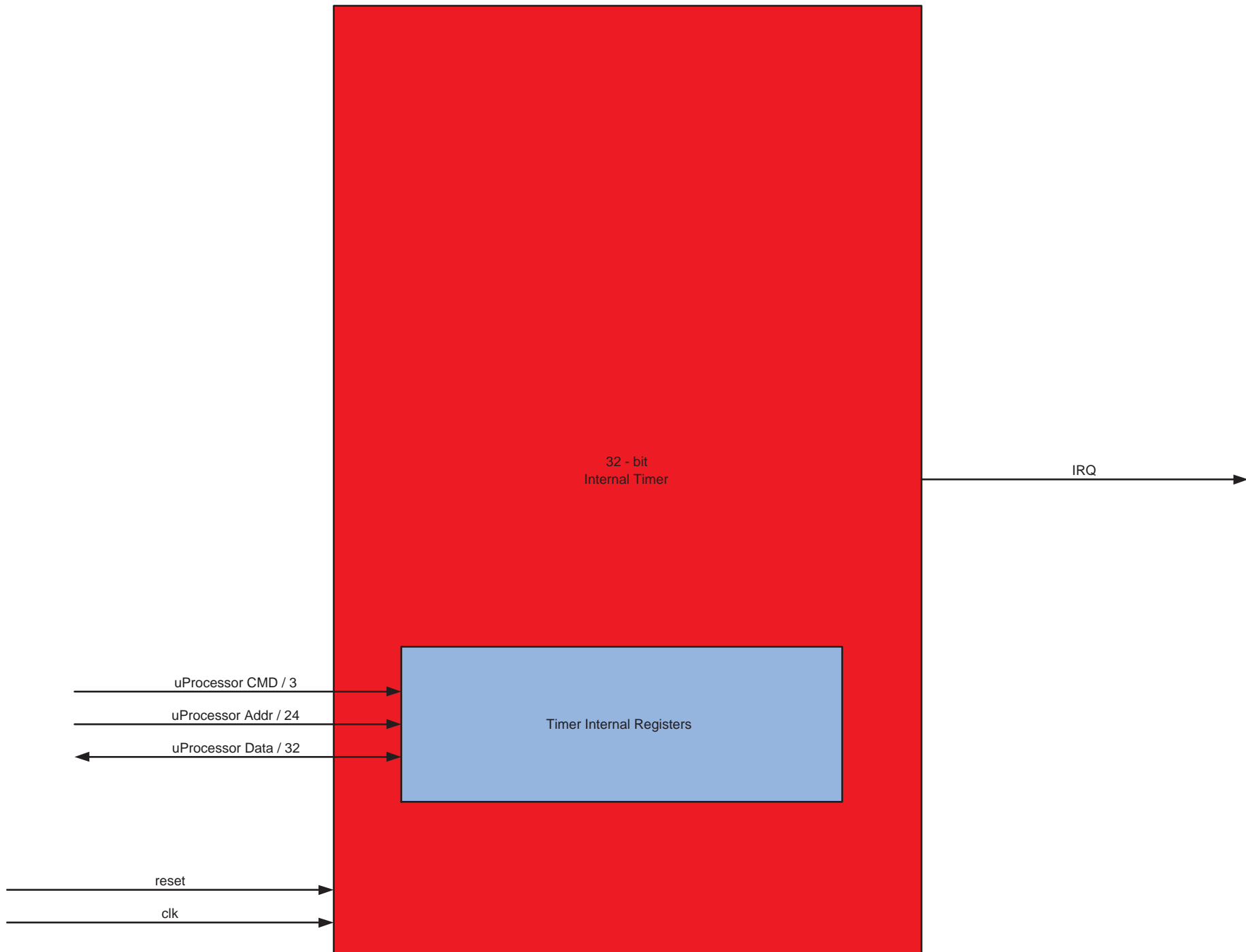
Instruction Cache



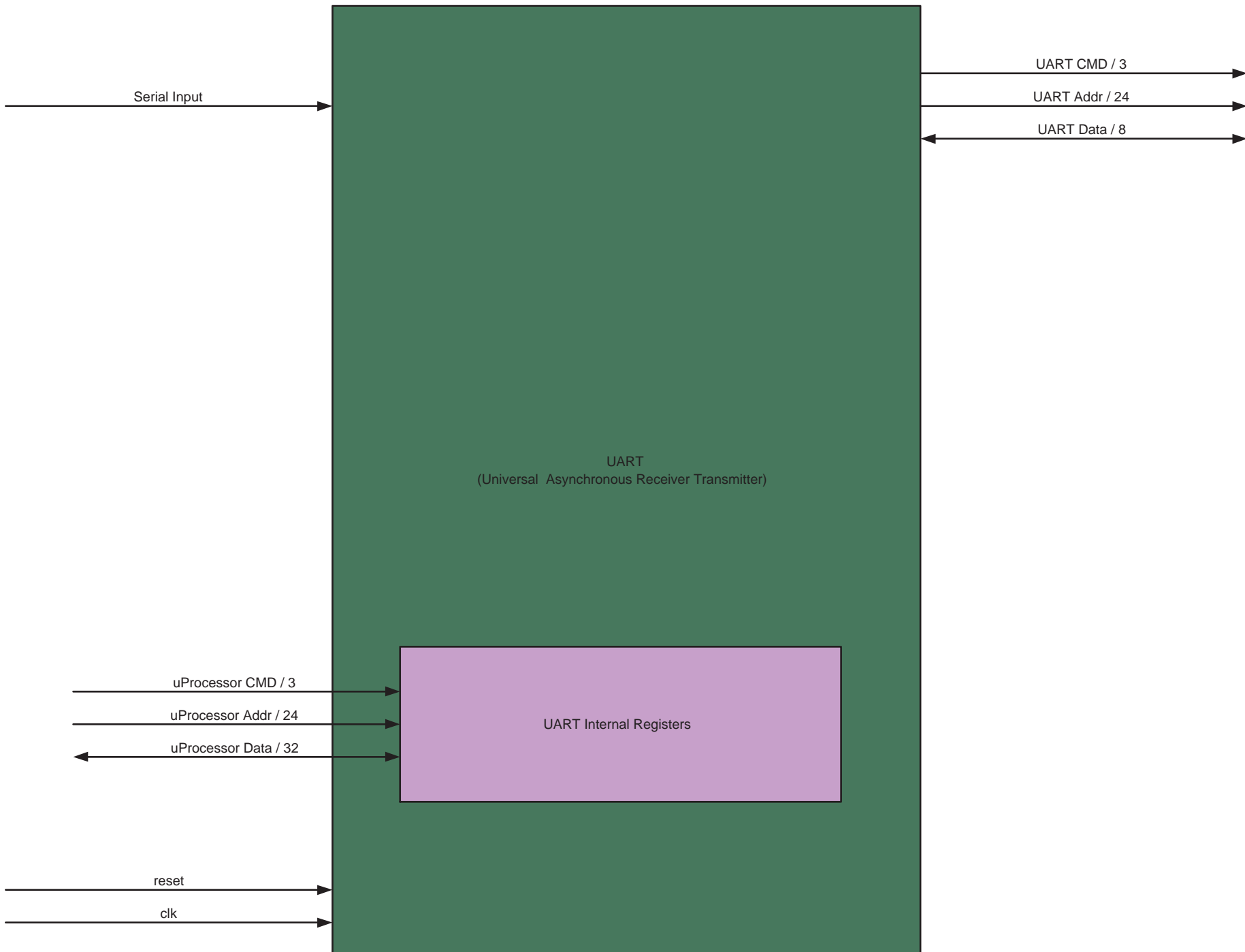
Direct Memory Access



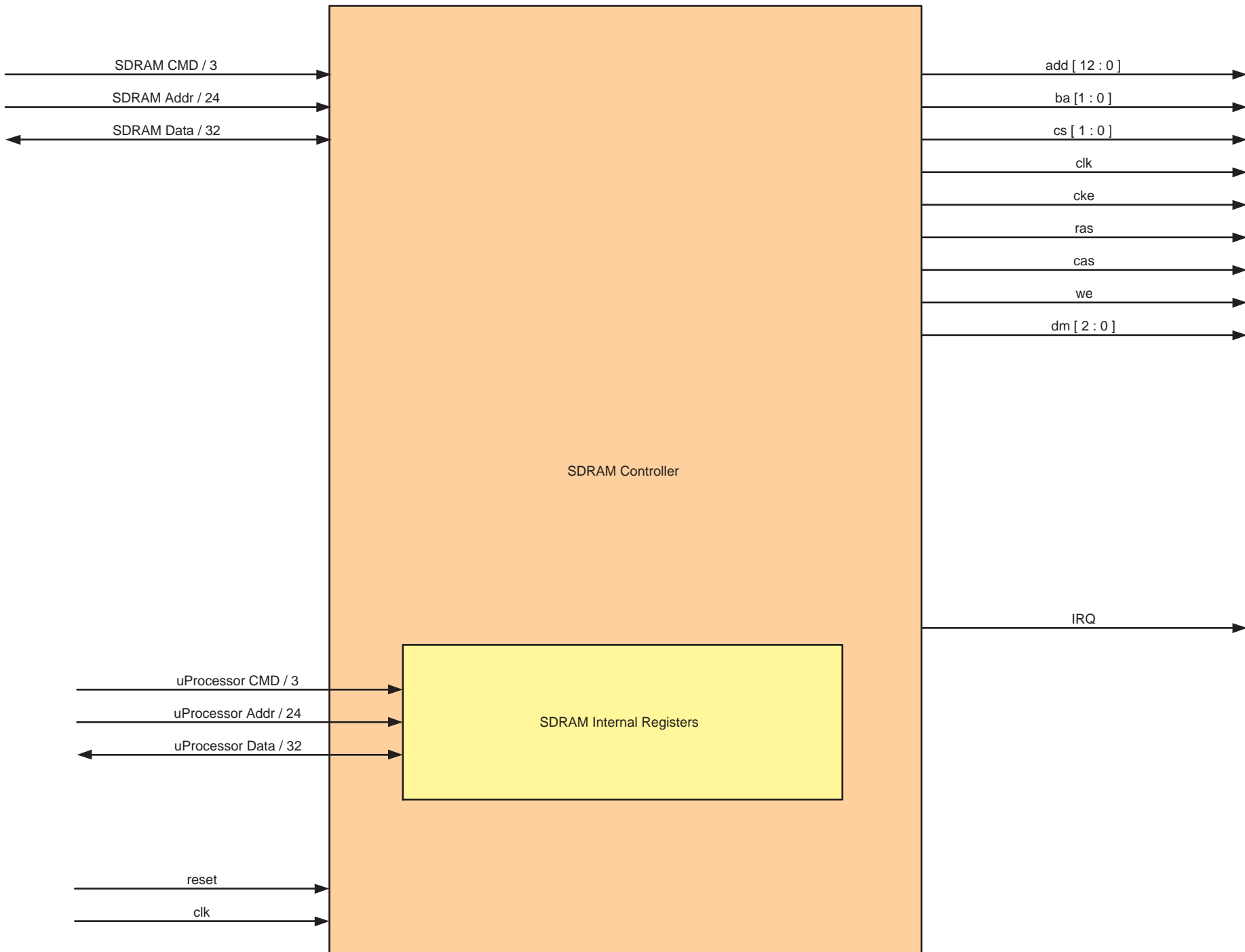
32 - bit Timer



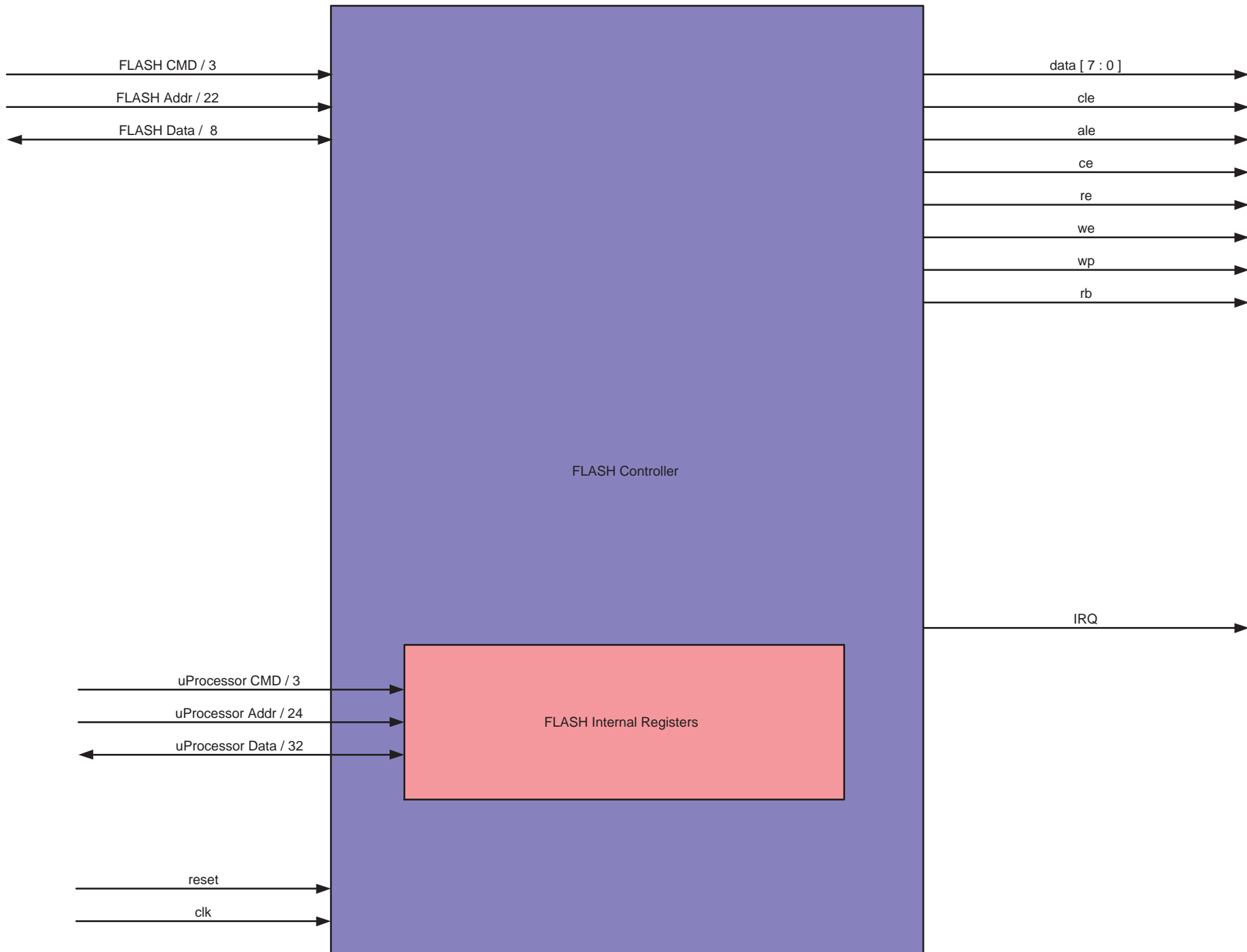
UART



SDRAM Controller



Flash Controller



Memory Map

