IEEE 1394
Link Layer Core
Specification

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Revision History

Rev	Date	Author	Description
Working	**11/03/01**	**Jim.W**	**First draft**

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2 Architecture

2.1 Block Diagram

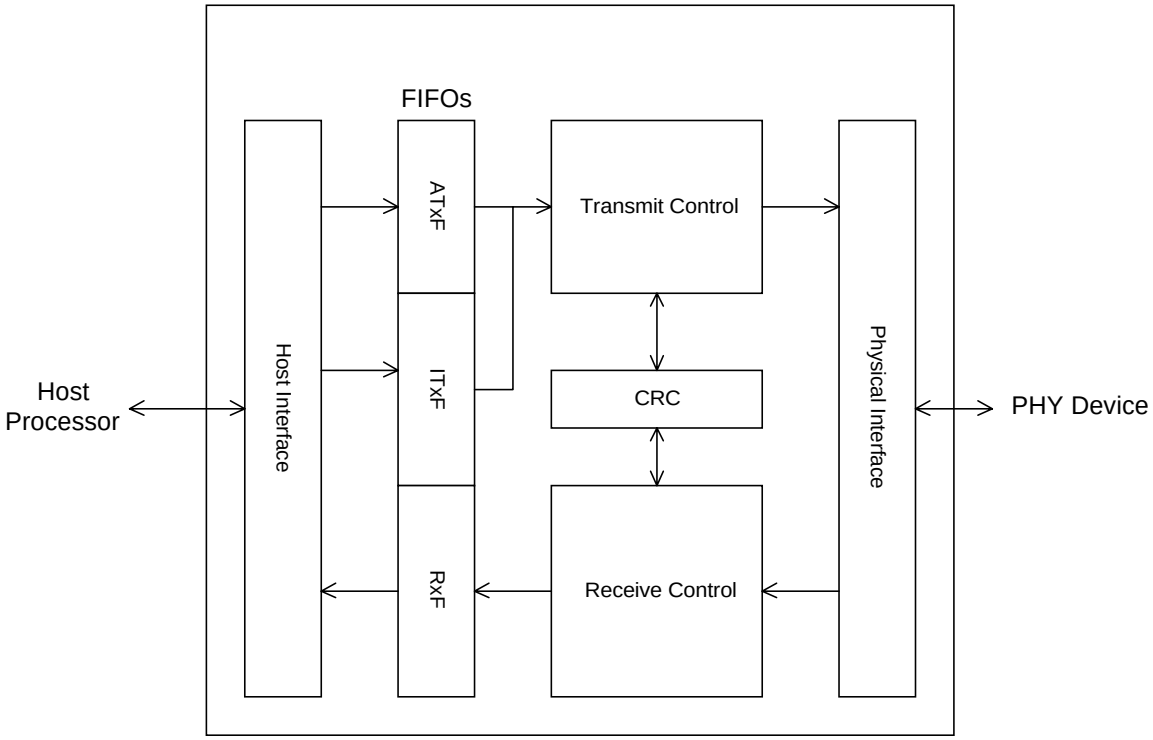

Figure 1 Link Layer Core Block Diagram

2.2 Physical Interface

The physical (PHY) interface is responsible for the following operations:

- Gain access to the serial bus.
- Send and receive packet.
- Send and receive acknowledge packets.
- Provide read and write access to PHY registers.

2.3 Transmit Control

The transmit control block is responsible for the following operations:

- Receive data from either the Asynchronous Transmit FIFO (ATxFIFO) or the Isochronous Transmit FIFO (ITxFIFO).
- Creates serial-bus packets to be transmitted through the PHY interface.
- Arbitrate for the serial bus to correctly send both asynchronous and isochronous packets
- Sends cycle-start packets in cycle master mode.

2.4 Receive Control

The receive control block is responsible for the following operations:

- Receive incoming packets from the PHY interface.
- Check the CRC of the incoming packets addressed to the node.
- Sends the header to Receiving FIFO (RxFIFO) if header CRC is good. Otherwise flush the header and ignore the rest of the packet.
- Check the rest data of the packet and sends the data to RxFIFO
- Send a status quadlet to RxFIFO.

2.5 CRC

The CRC block is responsible for a 32-bit CRC generation for error detection. It generates the header and data CRC for transmitting packets and checks the header and data CRC for received packets.

2.6 FIFOs

The FIFO block includes two transmit blocks, Asynchronous Transmit FIFO (ATxFIFO) and the Isochronous Transmit FIFO (ITxFIFO).

2.7 Host Interface

The host interface block is responsible for the communication between the link layer core and the host processor.

3 I/O Ports

3.1 Physical Interface

Name	I/O	Description
D[0:7]	I/O	PHY-link interface data bus. Data is expected on D0 – D1 for 100 Mbits/s packets, D0 – D3 for 200 Mbits/s, and D0 – D7 for 400 Mbits/s.
Ctl[0:1]	I/O	PHY-link interface control bus. CTL1 and CTL0 indicate the four operations that can occur on this interface.
Lreq	O	Link request to PHY. LReq makes bus requests and register access requests to the PHY.
SClk	I	System clock. SClk is a 49.152-MHz clock from the PHY and used to generate the 24.576-MHz clock.

3.2 Host Interface

3.2.1 Generic Host Interface

3.2.2 Wishbone Host Interface

3.2.3 PCI Host Interface

4 Operations

4.1 Asynchronous Transmit

4.2 Isochronous Transmit

4.3 Asynchronous Receive

4.4 Isochronous Receive

5 Registers