Open Floating Point Unit

The Free IP Cores Projects
www.opencores.org

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Summary:
This documents describes a free single precision floating point unit. This floating point unit can perform add, subtract, multiply, divide, integer to floating point and floating point to integer conversion.

Change Log

13/9/2000   RU
        Initial release of FPU

To Do

Things that still need to be done:

        - As of 9/13/200 int2float and float2int conversions are still missing
        - Improve performance by prediction leading zeros in post normalization unit

1. Introduction

This document describes a single precision floating point unit. The floating point unit is fully IEEE 754 compliant.

1.1. The FPU supports the following operations:

fpu_op	Operation
0	Add
1	Subtract
2	Multiply
3	Divide
4	Int to float conversion (Future function)
5	Float to int conversion (Future Function)
6	Remainder (Future Function)
7	RESERVED

1.2. The FPU supports the following Rounding Modes:

| rmode	Rounding Mode
0	Round to nearest even
1	Round to Zero
2	Round to +INF (UP)
3	Round to -INF (DOWN)

1.3. General Operation

The FPU can perform a floating point operation every cycle. It will latch the operation type, rounding mode and operands and deliver a result four cycles later.

2. FPU Architecture

This is a simple single precision floating point unit.

Below diagram illustrates the internal of this implementation (pipeline not shown).
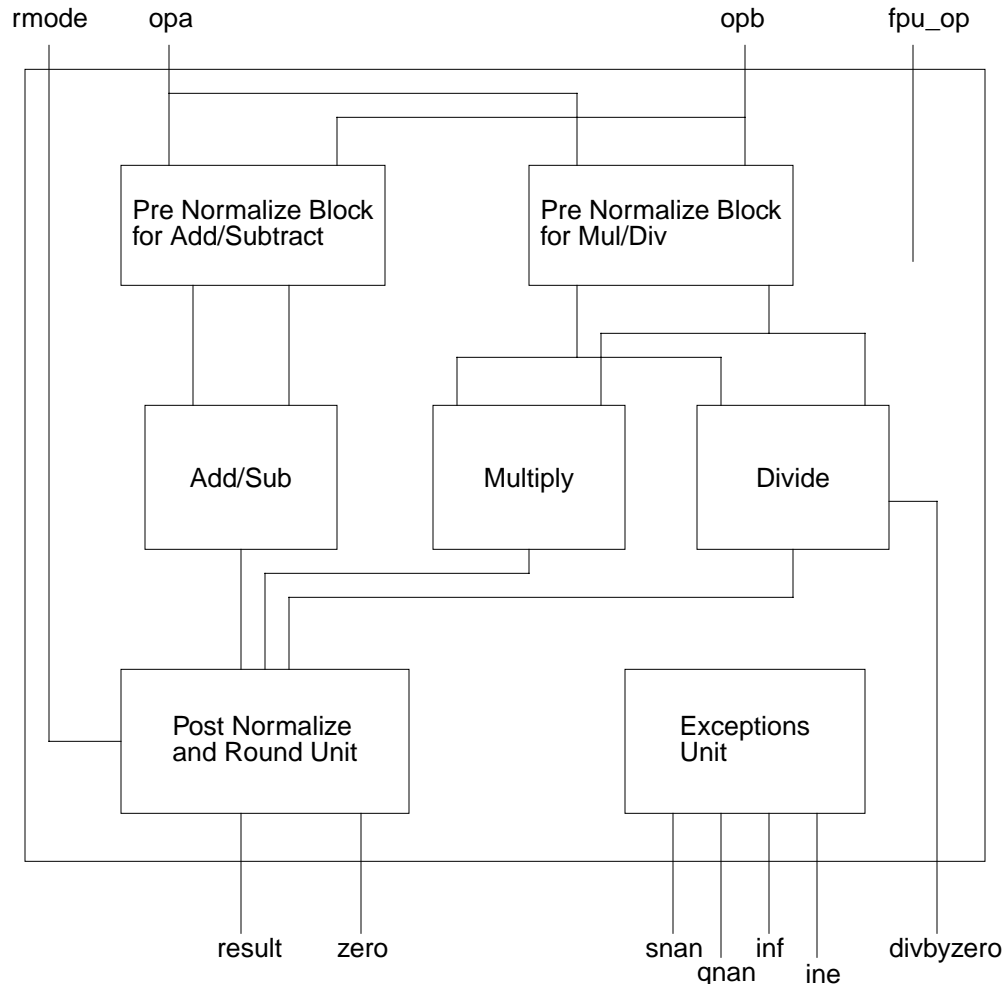
2.1. General Notes

1. The FPU will never generate a SNAN on the output
2. The SNAN output is asserted when one of the operands was a signaling NAN (output will be a quiet NAN).
3. The QNAN output is asserted whenever the OUTUT of the FPU is NAN (always a quiet NAN).

3. Interface

This table lists all inputs and outputs of the FPU and provides a general description of their functions.

Table 1:

Signal Name	With	Direction	Description
clk	1	Input	System Clock
rmode	4	Input	Rounding Mode
fpu_op	7	Input	Floating Point Operation Select
opa, opb	32	Input	Operand a and B
out	32	Output	Result Output
snan	1	Output	Asserted when either operand is a SNAN
qnan	1	Output	Asserted when output is a QNAN
inf	1	Output	Asserted when output is a INF
ine	1	Output	Asserted when the Result is Inexact
overflow	1	Output	Asserted when a overflow occurs
underflow	1	Output	Asserted when a Underflow occurs
div_by_zero	1	Output	Asserted when the fpu_op is set to divide and opb is zero
zero	1	Output	Asserted when the output is a numeric zero