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FH Crossbar
Reference Manual

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Contents

1 REVISION HISTORY

Table 1

Revision	Author	Date	Description
1.00	Lasse Lehtonen	22.8.2011	Initial documentation

2 DOCUMENT OVERVIEW

2.1 SCOPE

This documentation describes the basic operation and usage of FH Crossbar Network-on-Chip component.

2.2 AUDIENCE

For hardware integrators wanting to use this component.

2.3 RELATED DOCUMENTATION

Table 2

Document	Description

2.4 DOCUMENT CONVENTIONS

- Ports: `teletype` in text
- Generics: `teletype` in text

3 INTRODUCTION

3.1 BRIEF DESCRIPTION

FH Crossbar Network-on-Chip is a highly configurable network. Network can be configured to use either store-and-forward of wormhole switching and either packet or circuit switching. Fifo depths and bus widths can be freely set and the network supports different synchronous frequencies for agents than the network's operating frequency.

3.2 EXAMPLE SYSTEM

Example system in figure 1 presents a four agent FH Crossbar.

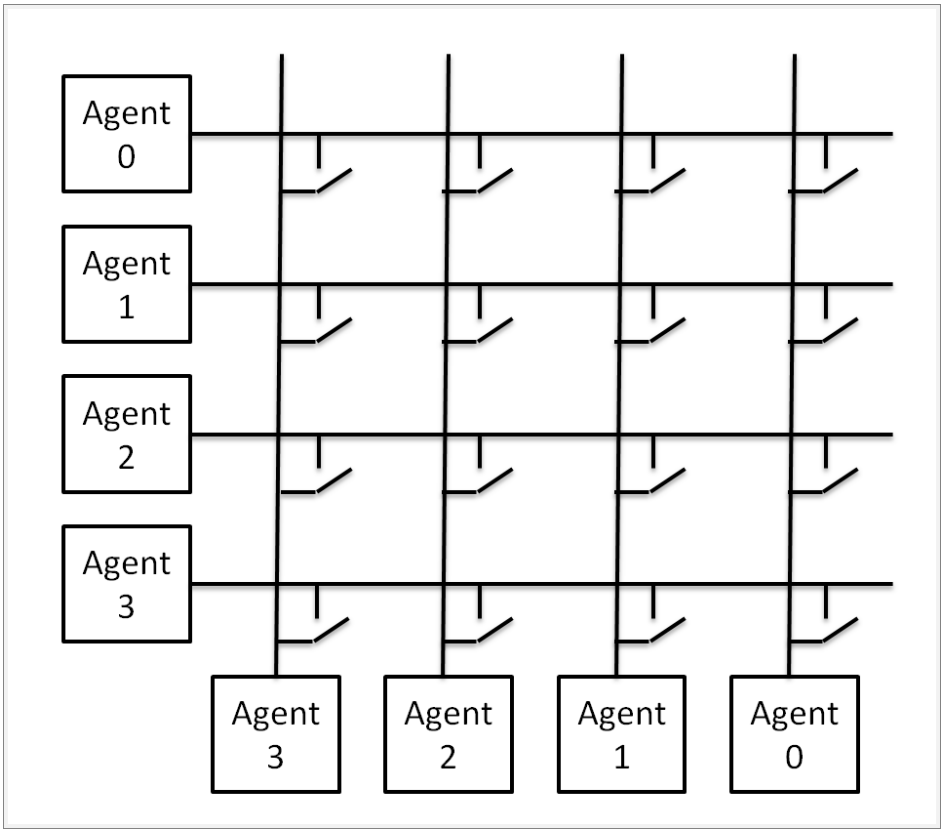

Figure 1

4 HARDWARE DESIGN

4.1 FH CROSSBAR

4.1.1 GENERICS

Table 3

Name	Description
pkt_switch_en_g	Packet (1) or circuit (0) switched
n_ag_g	Number of agents NoC connects
stfwd_en_g	Selects between store-and-forward (1) and wormhole (0) switching
data_width_g	Width of the data bus in bits
addr_width_g	Width of the address bus in bits. Must be less or equal than data_width_g
fifo_depth_g	Depth of FIFOs in words
packet_length_g	Maximum packet size in words
timeout_g	How long to wait for packet to fill
lut_en_g	Enable memory mapped address translation
len_flit_en_g	Enable packet to carry length information in its own flit
fill_packet_g	Only send full packets
oaddr_flit_en_g	Enable packet to carry the destination memory-mapped address
max_send_g	Max continuos send in the crossbar
net_freq_g	Network's frequency relative to IP frequecy
ip_freq_g	Agent's relative frequency to network frequecy

4.1.2 CLOCKING AND RESET

Table 4

Port	Width	Direction	Description
clk_net	1	in	Clock for the network, active on rising edge
clk_ip	1	in	Clock for the IP, active on rising edge
rst_n	1	in	Reset, asynchronous, active low

Clock frequencies must be at integer ratio (e.g. 1:3 but not 2:3) and they must have a synchronized rising edge.

4.1.3 DATA INTERFACE

Table 5

Port	Width	Direction	Description
tx_data_in	n_ag_g*data_width_g	in	All TX datas from IPs
tx_we_in	n_ag_g	in	Write enables from all IPs
tx_re_in	n_ag_g	in	Read enables from all IPs
rx_data_out	n_ag_g*data_width_g	out	All RX datas from the network
rx_empty_out	n_ag_g	out	RX FIFO empty signals
rx_full_out	n_ag_g	out	RX FIFO full signals
tx_empty_out	n_ag_g	out	TX FIFO empty signals
tx_full_out	n_ag_g	out	TX FIFO full signals

Routers are connected to vectors starting from 0 and continuing to $n\_ag\_g - 1$.

4.1.4 ARCHITECTURE

Packet Codec is instantiated between the FH Crossbar and agents to enable additional features such as clock domain crossing and address translation from memory mapped io addresses to the network address.

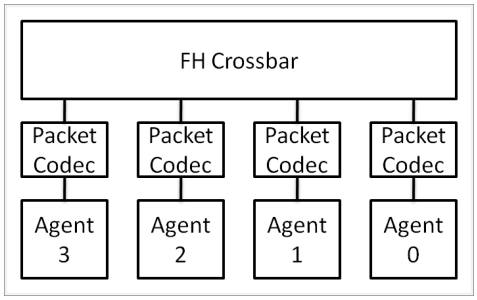

Figure 2

4.1.5 INTEGRATION

Related source files are listed in next table in the order of compilation (when applicable).

Table 6

Filename	Description
fifo.vhd	Simple synchronous FIFO
multiclk_fifo.vhd	FIFO with clock domain crossing
pkt_counter.vhd	Debug component counting packets
addr_lut_pkg.vhd	Package for pkt_codec
addr_lut.vhd	Address translation unit
pkt_enc.vhd	Packet encoder
pkt_dec.vhd	Pakcet decoder
pkt_enc_dec_1d	Top level for encoders and decoders
allocator.vhd	Allocates connections
arbiter.vhd	Arbiter
io_block.vhd	Contains FIFOSs
switch_matrix.vhd	Switching element
crossbar.vhd	Top level for FH Crossbar
crossbar_with_pkt_codec_top.vhd	Top level with Packet Codecs

4.1.6 SWITCHING

Depending on generic `stfwd_en_g` FH Crossbar uses either store-and-forward or wormhole switching. If store-and-forward switching is used the Packet Codec handles the creation of the network packet. If there's not enough data to fill the whole packet the unused flits will be sent empty. Packet Codec will wait few clock cycles before filling the packet to allow IP to stall a little while sending. For store-and-forward switching the FIFOs must be the same size as the packets. If circuit-switched mode is used Packet Codec is not instantiated.

For wormhole switched configuration there's no limitation to the size of the FIFOs.

5 TESTING

5.1 TEST CASE

FH Crossbar network model comes with a simple test case which instantiates a six agent crossbar with packet codec inteface. Test case sends one message from agent 0 to agent 5 and terminates after that.

5.2 SIMULATION

In order to simulate the test case one needs to compile files listed in table 6 in addition to files listed in table 7 found in basic_tester/vhd. Top level for the simulation (simple_test_crossbar.vhd) and the test case files are located in directory crossbar/sim. For the users of Modelsim also a do-file to compile needed files is supplied.

Table 7

Filename	Description
txt_util.vhd	Helper functions for printing
basic_tester_pkg.vhd	Package for Basic Tester
basic_tester_tx.vhd	Transfer generation
basic_tester_rx.vhd	Transfer validator