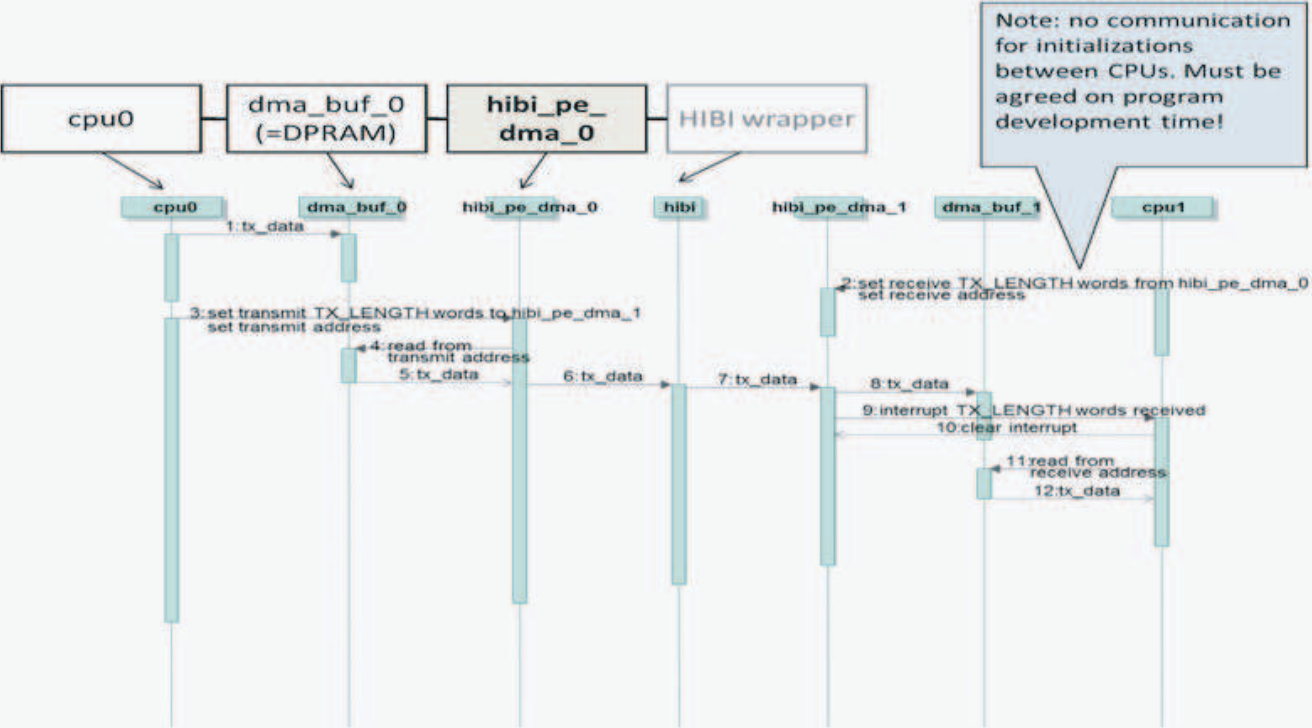
cpu0
dma_buf_0 (=DPRAM)
hibi_pe_ dma_0
HIBI wrapper
Note: no communication for initializations between CPUs. Must be agreed on program development time!
cpu0
dma_buf_0
hibi_pe_dma_0
hibi
hibi_pe_dma_1
dma_buf_1
cpu1
1:tx_data
2:set receive TX_LENGTH words from hibi_pe_dma_0
set receive address
3:set transmit TX_LENGTH words to hibi_pe_dma_1
set transmit address
4:read from transmit address
5:tx_data
6:tx_data
7:tx_data
8:tx_data
9:interrupt TX_LENGTH words received
10:clear interrupt
11:read from receive address
12:tx_data