#	Generic and VHDL default	Category	Subcategory	Type	Value range	Description
1	addr_width_g : integer := 32;	Structural	Bus widths	Bits	less than or equal data_width_g if muxed	address (bus) width
2	data_width_g : integer := 32;	Structural	Bus widths	Bits	positive integer	width of data bus (which can be multiplexed with address)
3	comm_width_g : integer := 5;	Structural	Bus widths	Bits	practically always 3	width of command bus
4	counter_width_g : integer := 8;	Structural	Bus widths	Bits	greater or equal than (log(max_send)	width if the internal counters in a wrapper
5	debug_width_g : integer := 0	Structural	Bus widths	Bits	positive integer	width of debug port (for special monitors)
6	rx_fifo_depth_g : integer := 5;	Structural	FIFO	Words	0,2,3...	Rx fifo depth
7	rx_msg_fifo_depth_g : integer := 5;	Structural	FIFO	Words	0,2,3...	Rx message (high-priority) fifo depth
8	tx_fifo_depth_g : integer := 5;	Structural	FIFO	Words	0,2,3...	Tx fifo depth
9	tx_msg_fifo_depth_g : integer := 5;	Structural	FIFO	Words	0,2,3...	Tx message (high-priority) fifo depth
10	fifo_sel_g : integer := 0;	Synchronization	Clock domains	Number	0-3: Synchronous multi-clock, GALS (globally asynchronous, locally synchronous), Gray FIFO, or Mixed clock pausible	Type of the synchronizing FIFO buffers between bus and agent
11	rel_agent_freq_g : integer := 1;	Synchronization	Clock domains	Number	positive integer	Relative frequencies of IP and bus, Needed at least for synchr. multiclk FIFOs
12	rel_bus_freq_g : integer := 1;	Synchronization	Clock domains	Number	positive integer	see above
13	addr_g : integer := 46;	Functional	Addressing	Number	positive integer	unique address for each wrapper
14	inv_addr_en_g : integer := 0;	Functional	Addressing	Number	0 or 1	only for bridges, other half uses 0 and the other 1
15	multicast_en_g : integer := 0	Functional	Addressing	Number	0 or 1	enable special addressing
16	n_agents_g : integer := 4;	Functional	Arbitration	Number	positive integer	total number of agents within one segment (distributed arbitration requires this)
17	prior_g : integer := 2;	Functional	Arbitration	Number	less than or equal n_agents	unique priority value for all wrappers within one segment
18	max_send_g : integer := 50;	Functional	Arbitration	Number	in words, 0 means unlimited	max words the wrapper can reserve bus
19	n_time_slots_g : integer := 0;	Functional	Arbitration	Number		Number of time slots in a TDMA frame. TDMA is enabled by setting n_time_slots > 0. Ensure that all wrappers in a segment agree on arb_type, n_agents, and n_slots. Max_send can be wrapper-specific.
20	arb_type_g : integer := 0;	Functional	Arbitration	Number	0 round-robin, 1 priority, 2 combined, 3 DAA	Arbitration type
21	keep_slot_g := 1	Functional	Arbitration	Number	For TDMA: 0 release unused time slots 1 keep unused	Keep reserved but unused slots in TDMA. **Not used in HIBI revision r3**
22	id_g : integer := 5;	Func/Struct	Reconfiguration	Number	positive integer	unique wrapper identification for reconfiguration
23	id_width_g : integer := 4;	Func/Struct	Reconfiguration	Number	greater than or equal(log2(id_g))	wrapper identification size = max number of wrappers
24	base_id_g : integer := 5;	Func/Struct	Reconfiguration	Number	positive integer	only for bridges, which cfg id are routed acrossa the bridge
25	cfg_re_g : integer := 0;	Func/Struct	Reconfigur	Number	0 or 1	enable reading configuration memory
26	cfg_we_g : integer := 0;	Func/Struct	Reconfigur	Number	0 or 1	enable writing configuration memory
27	n_extra_params_g : integer := 0;	Func/Struct	Reconfigur	Number	positive integer	Number of app-specific extra registers
28	n_cfg_pages_g : integer := 1;	Func/Struct	Reconfiguration	Number	1,2,3...	Number of configuration pages. Having multiple pages allows fast reconfig. Note that cfg memory initialization is done with separate package if you have many time slots or configuration pages