	Property	HIBI v.3
Basics	Description language	VHDL, SystemC
	Topology	Hier.bus
	Interface	HIBI-specific OCP (TLM1, TLM2)
	Clocking	Synchronous wrapper GALS network
	Switching type (within segment)	Circuit-switching
	Switching type (between segments)	Wormhole (packet)switching
Configuration	Configuration	Design-time, runtime
	Design-time configurable parameters	Data width, addr width, FIFO sizes, address mutliplexing, initial configuration, addresses, clocking style Number of config pages and their type (RAM/ROM)
	Run-time configurable parameters	TDMA cycle and slots, max send, own priority Current TDMA clk cycle Utilized arbitration algorithm Change configuration page, change configuration contents (of RAM)
Transfers	Burst transfers	All transfers are bursts
	Data priority	2-level: regular and high-prior
	Commands	17 idle write: data (lo/hi-prior), config, conditional (lo/hi), non-post data (lo/hi) read request: data (lo/hi-prior), config, linked (lo/hi) exclusive access: lock, write, read, release
Signals	System signals	Clk, rst_n
	Bus signals	Data [n-1:0] (*) may contain address as well Addr valid Command [4:0] Lock Full
	IP signals	Data, addr valid, cmd, we, full, re, empty, optionally one_p + one_d
	Address lines	Multiplexed or concatenated with data
	Signal type	Unidirectional, all shared
	Signal resolution	OR-based
Flow control	Arbitration algorithms	Round-robin, DAA, TDMA, priority, random, combination
	Arbitration implementation	Distributed Pipelined
	Handshaking	1 hadnshake signal, RX buffering reserved at application level
	Qos	TDMA, round-robin/prior with limited tx length Multiple priorities for data Fast runtime configuration TDMA synchronization
Usage	Verification	HW sim, HW/SW sim FPGA prototypes
	Articles	> 10 conference, >5 journals
	Test applications (simulation)	10-CPU H.263 video encoder Synthetic test cases WLAN baseband
	Test applications (FPGA)	H.263 H.263 + WLAN (FPGA) MPEG-4, up to 35 CPUs + accelerators