GPIO IP Core Specification

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Revision History

Rev.	Date	Author	Description
0.1	4/2/01	Damjan Lampret	First Draft
0.2	20/2/01	Damjan Lampret	Compliance with WISHBONE Rev.B1
0.3	29/10/01	Damjan Lampret	Updated names of ports and RGPIO_CTRL. Added additional parameters to Appendix A.

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Introduction

The GPIO IP core is user-programmable general-purpose I/O controller. Its use is to implement functions that are not implemented with the dedicated controllers in a system and require simple input and/or output software controlled signals.

Features

The following lists the main features of GPIO IP core:

- Number of general-purpose I/O signals is user selectable and can be in range from 1 to 32. For more I/Os several GPIO cores can be used in parallel.
- All general-purpose I/O signals can be bi-directional (external bi-directional I/O cells are required in this case).
- All general-purpose I/O signals can be three-stated or open-drain enabled (external three-state or open-drain I/O cells are required in this case).
- General-purpose I/O signals programmed as inputs can cause interrupt to the CPU.
- General-purpose I/O signals programmed as inputs can be registered at raising edge of system clock or at user programmed edge of external clock.
- All general-purpose I/O signals are programmed as inputs at hardware reset.
- Auxiliary inputs to GPIO core to bypass outputs from RGPIO_OUT register.
- Alternative input reference clock signal from external interface.
- WISHBONE SoC Interconnection Rev. B compliant interface

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Architecture

Figure 1 below shows general architecture of GPIO IP core. It consists of four main building blocks:

- WISHBONE host interface
- GPIO registers
- Auxiliary inputs
- Interface to external I/O cells and pads

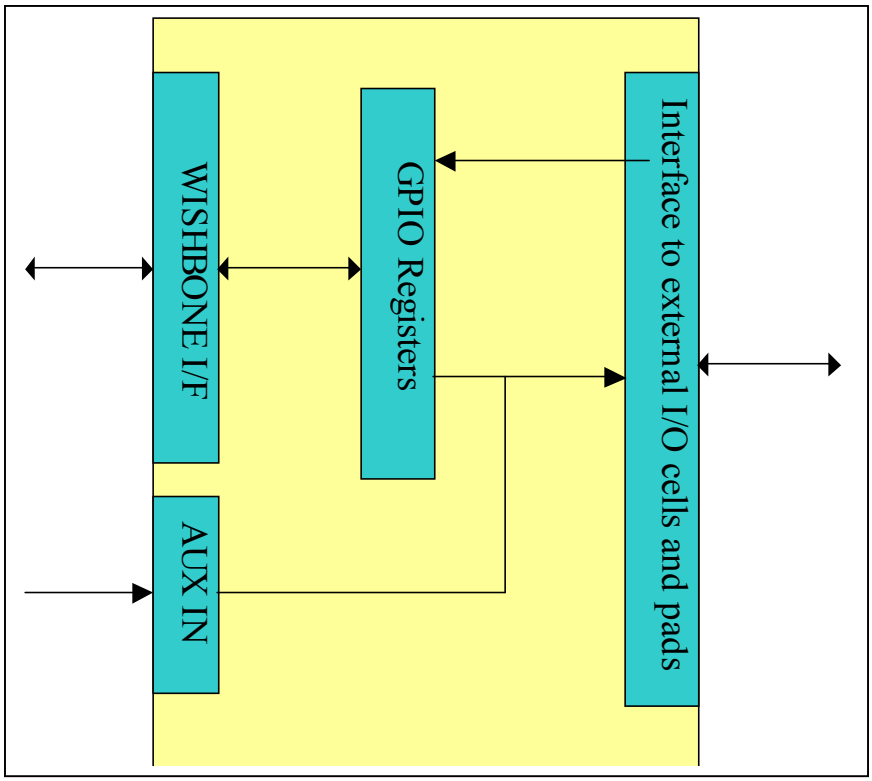

Figure 1. Core Architecture

Clocks

The GPIO core has two clock domains. All registers except RGPIO_IN are in system clock domain.
RGPIO_IN register can be clocked by system clock or by external clock reference.

WISHBONE Interface

WISHBONE interface connects GPIO core to the host system. It is WISHBONE SoC Interconnection specification Rev. B compliant. The implementation implements a 32-bit bus width and does not support other bus widths.

GPIO Registers

The GPIO IP Core has several software accessible registers. Most registers have the same width as number of general-purpose I/O signals and they can be from 1 – 32 bits. The host through these registers programs type and operation of each general-purpose I/O signal.

Auxiliary Inputs

The auxiliary inputs can bypass RGPIO_OUT outputs based on programming of RPGIO_AUX register. Auxiliary inputs are used to multiplex other on-chip peripherals on GPIO pins.

Interface to External I/O Cells and Pads

External interface connects GPIO core to external I/O ring cells and pads. To support open-drain or three-state outputs, appropriate open-drain or three-state I/O cells must be used.
Part of external interface is also ECLK signal. It can be used to register inputs based on external clock reference.

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Operation

This section describes the operation of the GPIO core. The GPIO core provides toggling of general-purpose outputs and sampling of general-purpose inputs under software control.

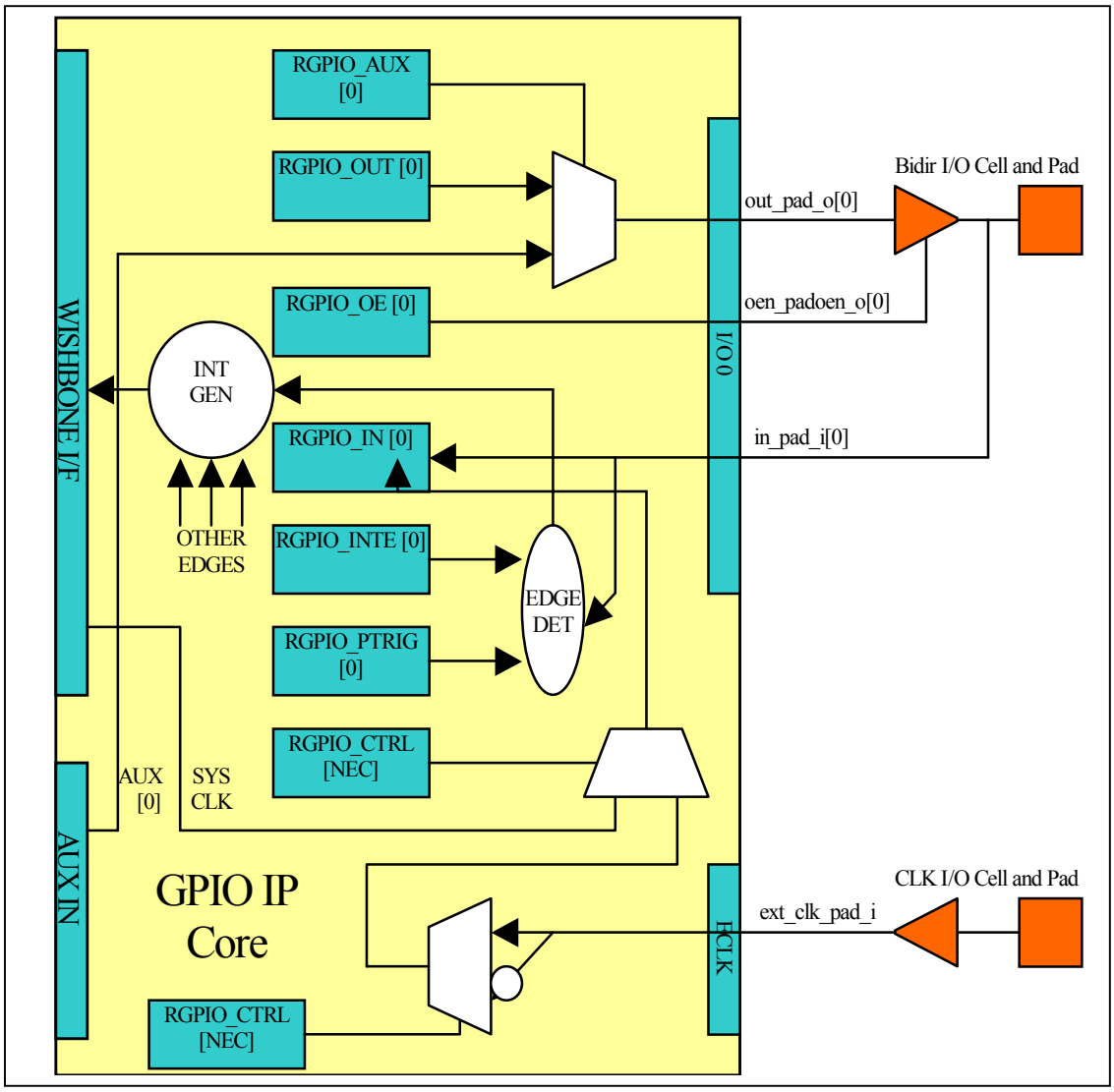

Figure 2. Block Diagram of GPIO Logic

General-purpose inputs can generate interrupts so that software does not have to be in poll mode all the time when sampling inputs.
General-purpose outputs can also be disabled by switching output drivers into open-drain or three-state mode.
To lower number of pins of the chip, other on-chip peripherals can be multiplexed together with the GPIO pins. For this purpose, auxiliary inputs can be multiplexed on general-purpose outputs.

Hardware Reset

Following hardware reset all general-purpose I/O signals are set into input mode. Meaning, all output drivers are disabled. All interrupts are masked, so that inputs would not generate any spurious interrupts. Gpio_eclk signal is not used to latch inputs into RGPIO_IN register; instead system clock is used.

General-Purpose I/O as Polled Input

To use general-purpose I/O as input only, bit in RGPIO_OE register must be cleared. Bit RGPIO_CTRL[INTE] and corresponding bit in RGPIO_INTE register must be cleared as well, to disabled generation of interrupts.
Bit RGPIO_IN register reflects registered value of general-purpose input signal. RGPIO_IN is updated on positive edge of system clock or if RGPIO_CTRL[ECLK] is set, on gpio_eclk edge. Which clock edge is selected, is defined by value of RGPIO_CTRL[NEC] bit.

General-Purpose I/O as Input in Interrupt Mode

To use general-purpose I/O as input with generation of interrupts, bit in RGPIO_OE register must be cleared. Bit in RGPIO_PTRIG register must be set to generate an interrupt on positive edge event on general-purpose input. To generate an interrupt on negative edge event, bit in RGPIO_PTRIG register must be cleared. Last, RGPIO_CTRL[INTE] bit and corresponding bit in RGPIO_INTE register must be set to enable generation of interrupts.
Bit RGPIO_IN register reflects registered value of general-purpose input signal. RGPIO_IN is updated on positive edge of system clock or if RGPIO_CTRL[ECLK] is set, on gpio_eclk edge. Which clock edge is selected, is defined by value of RGPIO_CTRL[NEC] bit.
Interrupt is de-asserted after read access to RGPIO_IN register.

General-Purpose I/O as Output

To enable general-purpose I/O output driver, bit in RGPIO_OE must be set. Bit in RGPIO_OUT register must be set to the value that is required to be driven on output

driver. Corresponding bit in RGPIO_INTE register must be cleared to disable generation of spurious interrupts.
Clearing bit in RGPIO_OE register will disable output driver and enable three-state or open-drain.

General-Purpose I/O as Bi-Directional I/O

To use general-purpose I/O as bi-directional signal, bit in RGPIO_OE must be toggled to enable or disable three-state or open-drain mode of bi-directional driver. Bit in RGPIO_OUT register must be set to the value that is required to be driven on output driver. Corresponding bit in RGPIO_INTE register must be cleared to disable generation of spurious interrupts. If input should generate interrupts, bit in RGPIO_INTE register must be set and bit in RGPIO_PTRIG should be set if required.
Bit RGPIO_IN register reflects registered value of general-purpose input signal. RGPIO_IN is updated on positive edge of system clock or if RGPIO_CTRL[ECLK] is set, on gpio_eclk edge. Which clock edge is selected, is defined by value of RGPIO_CTRL[NEC] bit.
If an interrupt is enabled and pending, it can be de-asserted by reading RGPIO_IN register.

General-Purpose I/O driven by Auxiliary Input

To drive general-purpose output with auxiliary input, bit in RGPIO_OE must be set to enable output driver. Bit in RGPIO_AUX must be set to enable multiplexing of auxiliary input onto general-purpose output.

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Registers

This section describes all control and status register inside the GPIO core. The *Address* field indicates address in hexadecimal. *Width* specifies the number of bits in the register, and *Access* specifies the valid access types for that register. R/W stands for read and write access and R stands for read only access.
Width of most registers is user selectable and is set by the user of the GPIO core at synthesis time.

Registers list

Name	Address	Width	Access	Description
RGPIO_IN	Base + 0x0	1 - 32	R	GPIO input data
RGPIO_OUT	Base + 0x4	1 - 32	R/W	GPIO output data
RGPIO_OE	Base + 0x8	1 - 32	R/W	GPIO output driver enable
RGPIO_INTE	Base + 0xC	1 - 32	R/W	Interrupt masking
RGPIO_PTRIG	Base + 0x10	1 - 32	R/W	Type of event that triggers an interrupt
RGPIO_AUX	Base + 0x14	1 - 32	R/W	Multiplex auxiliary inputs to GPIO outputs
RGPIO_CTRL	Base + 0x18	2	R/W	Control register

Table 1. List of All Software Accessible Registers

Register RGPIO_IN description

RGPIO_IN register latches general-purpose inputs. Reference clock is either system clock or ECLK input. Selection between both clocks is performed with RGPIO_CTRL[0].

Bit #	Access	Reset	Description
1 - 32	R	0x0	Latched value of general-purpose inputs

Table 2. Input Register

Register RGPIO_OUT description

RGPIO_OUT register drives general-purpose outputs. Additionally, external I/O cells can be operated open-drain or three-stated with RGPIO_OE register.

Bit #	Access	Reset	Description
1 - 32	R/W	0x0	General-purpose driven outputs

Table 3. Output Register

Register RGPIO_OE description

RGPIO_OE enables output/bi-directional mode of operation for each general-purpose I/O signal. When bit is set, corresponding general-purpose output driver is enabled. When bit is cleared, output/bi-directional driver is operating in open-drain or three-state mode.

Bit #	Access	Reset	Description
1 – 32	R/W	0x0	Output/bi-directional external I/O drivers enables

Table 4. Output Enable Register

Register RGPIO_INTE description

RGPIO_INTE register defines which general-purpose inputs generate interrupt to the host. When bit is set, corresponding general-purpose input generates interrupt.

Bit #	Access	Reset	Description
1 – 32	R/W	0x0	Enables for of interrupts generated by general-purpose input signals

Table 5. Interrupt Enable Register

Register RGPIO_PTRIG description

RGPIO_PTRIG register defines which edge of a general-purpose input generates an interrupt. Generation of an interrupt must be first enabled in RGPIO_INTE register. When bit is set, corresponding input generates an interrupt when positive edge is encountered. When bit is cleared, corresponding input generates an interrupt when negative edge is encountered.

Bit #	Access	Reset	Description
1 - 32	R/W	0x0	Triggering of an interrupt (positive edge when set, negative edge when cleared)

Table 6. Trigger Register

Register RGPIO_AUX description

RGPIO_AUX multiplexes auxiliary inputs to general-purpose outputs. When bit is set, corresponding auxiliary input drives corresponding general-purpose output instead of a bit in RGPIO_OUT register.

Bit #	Access	Reset	Description
1 - 32	R/W	0x0	When cleared, gpio_out signal is driven by a bit in RGPIO_OUT register. When set, gpio_out signal is driven by corresponding gpio_aux input.

Table 7. Auxiliary Inputs Register

Register RGPIO_CTRL description

Control bits in RGPIO_CTRL register control operation of entire GPIO core as opposed to bits in all other registers that control only individual general-purpose I/O signals.

Bit #	Access	Reset	Description
0	R/W	0	ECLK When set, gpio_eclk signal is used to latch general-purpose inputs into RGPIO_IN register. When cleared, system clock is used to latch input signals.
1	R/W	0	NEC When set, gpio_eclk is active on negative edge. When cleared, gpio_eclk is active on positive edge. This bit has no function when RGPIO_CTRL[ECLK] bit is cleared.
2	R/W	0	INTE When set, interrupt generation is enabled. When cleared, interrupts are masked.
3	R/W	0	INT When set, interrupt is pending. When cleared, no interrupt pending.

Table 8. Control Register

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IO ports

GPIO IP core has three interfaces. Figure 3 below shows all three interfaces:

- WISHBONE host interface
- Auxiliary inputs interface
- Interface to external I/O cells and pads

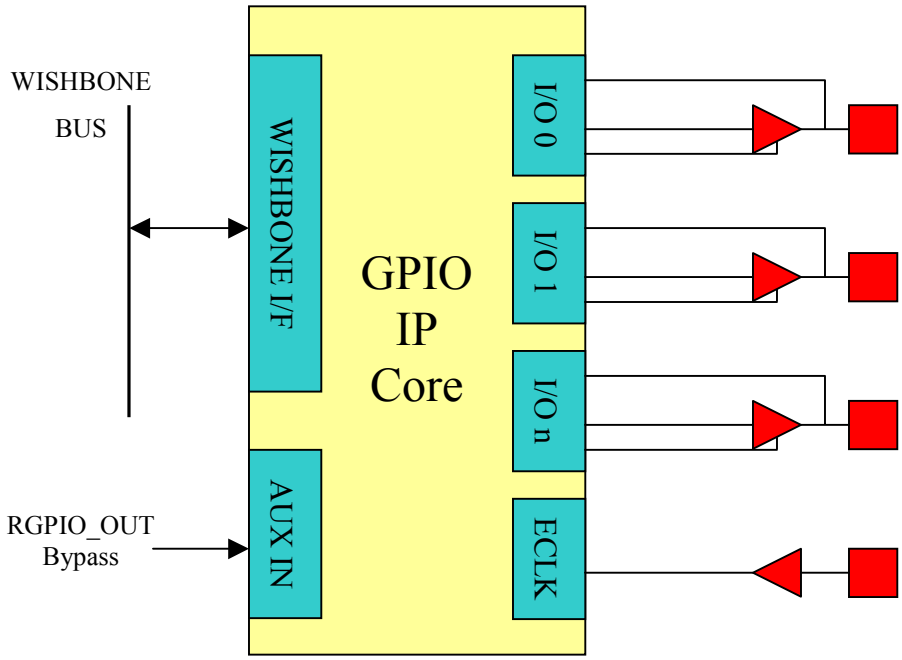

Figure 3. Core Interfaces

WISHBONE host interface

The host interface is a WISHBONE Rev B compliant interface. GPIO IP core works as a slave device only. When it needs the intervention of the local microcontroller, it will assert INTA_O.

Port	Width	Direction	Description
wb_clk_i	1	Input	Clock inputs
wb_rst_i	1	Input	Reset input

wb_cyc_i	1	Inputs	Indicates valid bus cycle (core select)
wb_adr_i	15	Inputs	Address inputs
wb_dat_i	32	Inputs	Data inputs
wb_dat_o	32	Outputs	Data outputs
wb_sel_i	4	Inputs	Indicates valid bytes on data bus (during valid cycle it must be 0xf)
wb_ack_o	1	Output	Acknowledgment output (indicates normal transaction termination)
wb_err_o	1	Output	Error acknowledgment output (indicates an abnormal transaction termination)
wb_rty_o	1	Output	Not used
wb_we_i	1	Input	Write transaction when asserted high
wb_stb_i	1	Input	Indicates valid data transfer cycle
wb_inta_o	1	Output	Interrupt output

Table 9. WISHBONE Interface' Signals

Auxiliary inputs

The auxiliary inputs can bypass RGPIO_OUT outputs based on programming of RPGIO_AUX register. Auxiliary inputs are used to multiplex other on-chip peripherals on GPIO pins.

Port	Width	Direction	Description
aux_i	1 - 32	Inputs	GPIO auxiliary inputs

Table 10. Auxiliary input signals

Interface to external I/O cells and pads

External interface connects GPIO core to external I/O ring cells and pads. To support open-drain or three-state outputs, I/O cells with open-drain or three-state support must be used.
Part of external interface is also ECLK signal. It can be used to register inputs based on external clock reference.

Port	Width	Direction	Description
in_pad_i	1 – 32	Inputs	GPIO inputs
out_pad_o	1 – 32	Outputs	GPIO outputs
oen_padoen_o	1 – 32	Outputs	GPIO output drivers enables (for three-state or open-drain drivers)
ext_clk_pad_i	1	Input	Alternative GPIO inputs' latch clock

Table 11. External interface

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Core HW Configuration

This section describes parameters that are set by the user of the core and define configuration of the core. Parameters must be set by the user before actual use of the core in simulation or synthesis.

Define	Range	Default	Description
GPIO_IOS	1 - 32	16	Number of general-purpose I/Os
GPIO_IMPLEMENTED		Defined	Define to implement the core
GPIO_READREGS		Defined	Define to allow reading of registers
GPIO_FULL_DECODE		Defined	Define to use full address decoding
GPIO_STRICT_32BIT_ACCESS		Defined	If not defined, wb_err_o will be asserted when WISHBONE access is not 32-bit.
GPIO_RGPIO_x	0 - 7	Defined 0 - 6	Address offsets for individual registers. Do not define an offset in order to prevent implementation of a register.
GPIO_DEF_RGPIO_x		0	Default values for unimplemented registers.

Table 12. List of All Core Parameters

There are additional parameters in the core but are considered only for development and should not be changed by the user.

Number of General-Purpose I/Os

Number of general-purpose I/O signals defines width of external interface and width of most of the software accessible registers. If more than 32 I/Os are required, several GPIO cores can be used in parallel.