Features

CAS Latency and Frequency

CAS Latency	Maximum Operating Frequency (MHz)			
	DDR200 -8	DDR266A -7	DDR266 -7F	DDR333 -6
2	100	133	133	133
2.5	125	143	143	166

- Double data rate architecture: two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK and $\overline{CK}$)
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Burst Lengths: 2, 4, or 8
- CAS Latency: (1.5), 2, 2.5, (3)
- Auto Precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- 7.8µs Maximum Average Periodic Refresh Interval (8K refresh)
- 2.5V (SSTL_2 compatible) I/O
- V_{DDQ} = 2.5V ± 0.2V / V_{DD} = 2.5V ± 0.2V
- TSOP66 package
- 60 balls BGA w/ 3 depop rows (“chipsize package”) 12 mm x 8 mm.

Description

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a *2n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM effectively consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 256Mb DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

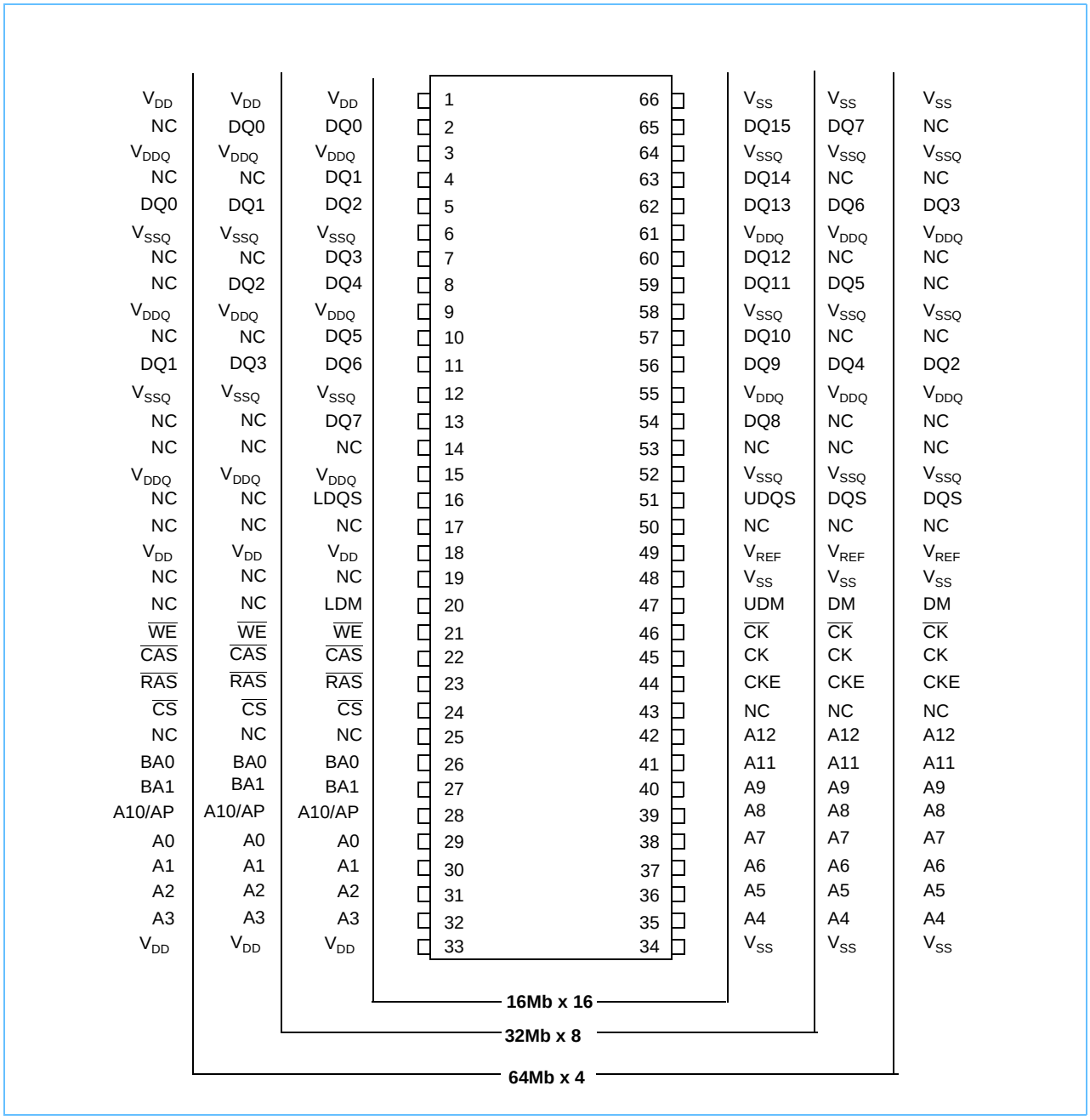
Note: The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Ordering Information

Part Number[a]	Org.	CAS-RCD-RP Latencies	Clock (MHz)	CAS-RCD-RP Latencies	Clock (MHz)	Speed	Package
HYB25D256400BT(L)-6	x4	2.5-3-3	166	2-3-3	133	DDR333	66 Pin P-TSOP-II
HYB25D256800BT(L)-6	x8						
HYB25D256160BT(L)-6	x16						
HYB25D256400BT(L)-7	x4		143			DDR266A	
HYB25D256800BT(L)-7	x8						
HYB25D256160BT(L)-7	x16						
HYB25D256400BT(L)-7F	x4			2-2-2		DDR266	
HYB25D256800BT(L)-7F	x8						
HYB25D256160BT(L)-7F	x16						
HYB25D256400BT(L)-8	x4		125		100	DDR200	
HYB25D256800BT(L)-8	x8						
HYB25D256160BT(L)-8	x16						
HYB25D256400BC(L)-6	x4	2.5-3-3	166	2-3-3	133	DDR333	60 Balls P-FBGA
HYB25D256800BC(L)-6	x8						
HYB25D256160BC(L)-6	x16						
HYB25D256400BC(L)-7	x4		143			DDR266A	
HYB25D256800BC(L)-7	x8						
HYB25D256160BC(L)-7	x16						
HYB25D256400BC(L)-7F	x4			2-2-2		DDR266	
HYB25D256800BC(L)-7F	x8						
HYB25D256160BC(L)-7F	x16						
HYB25D256400BC(L)-8	x4		125		100	DDR200	
HYB25D256800BC(L)-8	x8						
HYB25D256160BC(L)-8	x16						

a. HYB: designator for memory components
25D: DDR-I SDRAMs at Vddq=2.5V
256: 256Mb density
400/800/160: Product variations x4, x8 and x16
B: Die revision B
C/T: Package type FBGA and TSOP
L: Low power version (optional) - these components are specifically selected for low IDD6 Self Refresh currents
-5/6/7/7F/8: speed grade - see table

Pin Configuration (TSOP66)



16Mb x 16	32Mb x 8	64Mb x 4			16Mb x 16	32Mb x 8	64Mb x 4
V_{DD}	V_{DD}	V_{DD}	1	66	V_{SS}	V_{SS}	V_{SS}
NC	DQ0	DQ0	2	65	DQ15	DQ7	NC
V_{DDQ}	V_{DDQ}	V_{DDQ}	3	64	V_{SSQ}	V_{SSQ}	V_{SSQ}
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
V_{SSQ}	V_{SSQ}	V_{SSQ}	6	61	V_{DDQ}	V_{DDQ}	V_{DDQ}
NC	NC	DQ3	7	60	DQ12	NC	NC
NC	DQ2	DQ4	8	59	DQ11	DQ5	NC
V_{DDQ}	V_{DDQ}	V_{DDQ}	9	58	V_{SSQ}	V_{SSQ}	V_{SSQ}
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
V_{SSQ}	V_{SSQ}	V_{SSQ}	12	55	V_{DDQ}	V_{DDQ}	V_{DDQ}
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
V_{DDQ}	V_{DDQ}	V_{DDQ}	15	52	V_{SSQ}	V_{SSQ}	V_{SSQ}
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	NC	NC	NC
V_{DD}	V_{DD}	V_{DD}	18	49	V_{REF}	V_{REF}	V_{REF}
NC	NC	NC	19	48	V_{SS}	V_{SS}	V_{SS}
NC	NC	LDM	20	47	UDM	DM	DM
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	21	46	$\overline{CK}$	$\overline{CK}$	$\overline{CK}$
$\overline{CAS}$	$\overline{CAS}$	$\overline{CAS}$	22	45	CK	CK	CK
$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	23	44	CKE	CKE	CKE
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	24	43	NC	NC	NC
NC	NC	NC	25	42	A12	A12	A12
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
V_{DD}	V_{DD}	V_{DD}	33	34	V_{SS}	V_{SS}	V_{SS}

Pin Configuration (FBGA)

1	2	3		7	8	9
VSSQ	NC	VSS	A	VDD	NC	VDDQ
NC	VDDQ	DQ3	B	DQ0	VSSQ	NC
NC	VSSQ	NC	C	NC	VDDQ	NC
NC	VDDQ	DQ2	D	DQ1	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

(x 4)

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VDD	DQ0	VDDQ
NC	VDDQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VDDQ	NC
NC	VDDQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

(x8)

Top View (see the balls through the package)

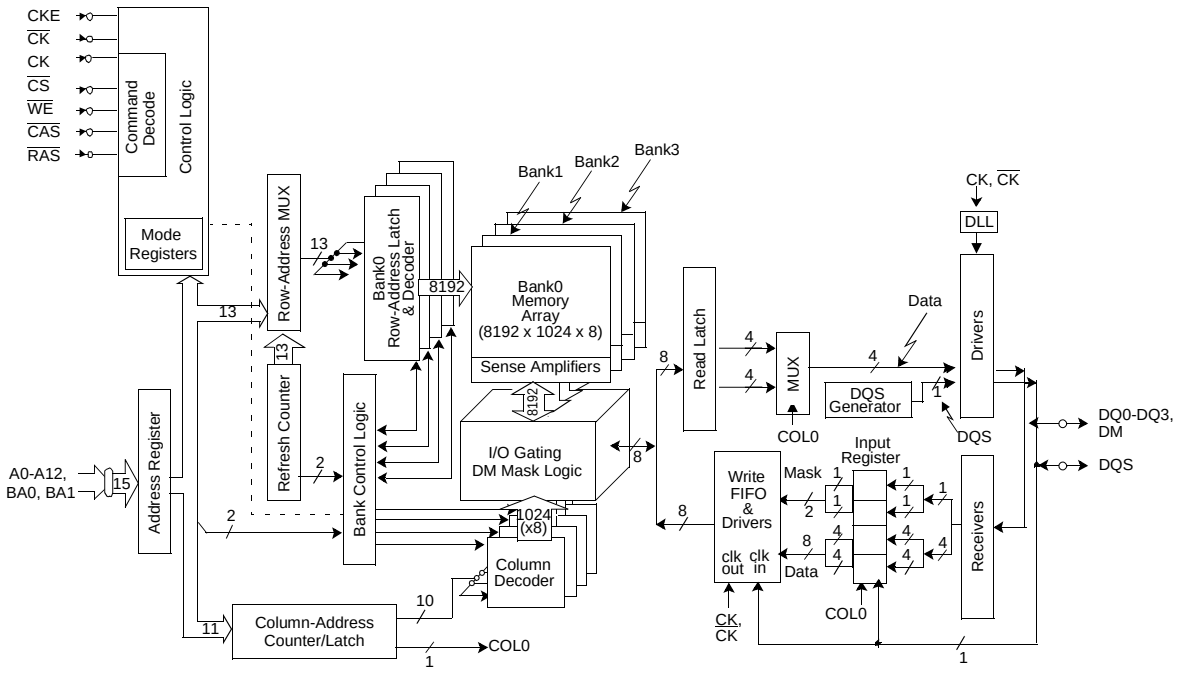
1	2	3		7	8	9
VSSQ	DQ15	VSS	A	VDD	DQ0	VDDQ
DQ14	VDDQ	DQ13	B	DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11	C	DQ4	VDDQ	DQ3
DQ10	VDDQ	DQ9	D	DQ6	VSSQ	DQ5
DQ8	VSSQ	UDQS	E	LDQS	VDDQ	DQ7
VREF	VSS	UDM	F	LDM	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

(x 16)

Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A12	Input	**Address Inputs:** Provide the row address for Active commands, and the column address and Auto Precharge bit for Read/Write commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a Mode Register Set command.
DQ	Input/Output	**Data Input/Output:** Data bus.
DQS	Input/Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 2.5V ± 0.2V.
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.5V ± 0.2V.
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**SSTL_2 reference voltage:** (V_{DDQ} / 2)

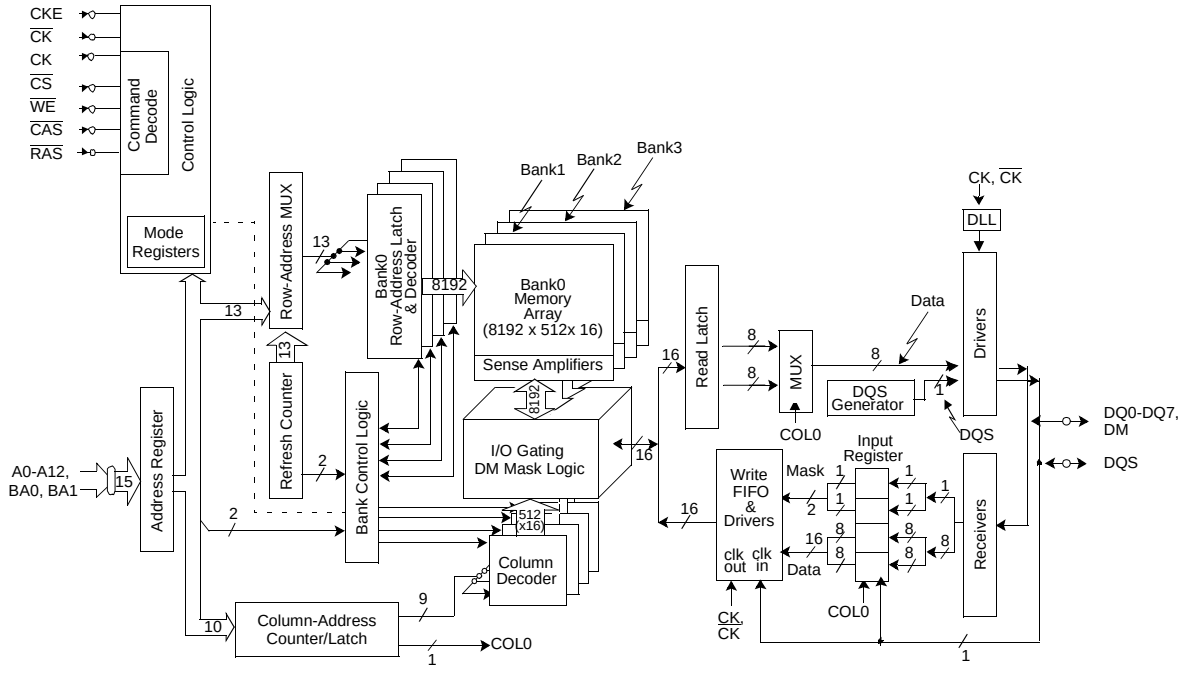
Block Diagram (64Mb x 4)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidi-rectional DQ and DQS signals.

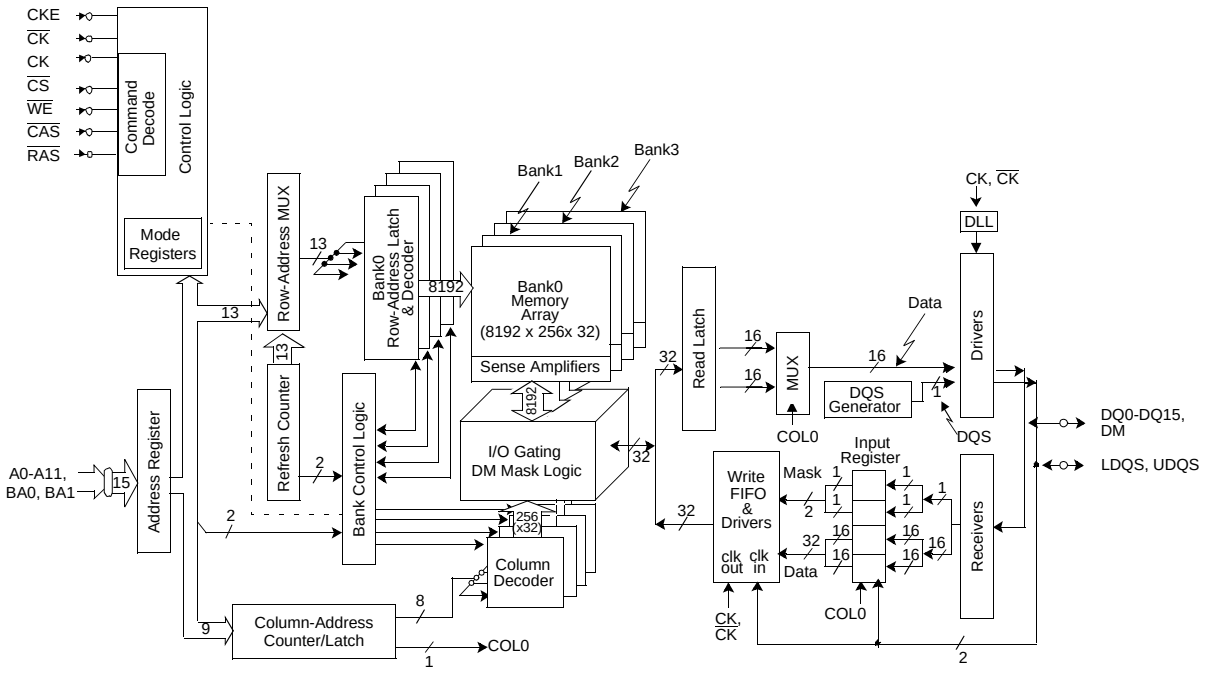
Block Diagram (32Mb x 8)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Block Diagram (16Mb x 16)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: UDM and LDM are unidirectional signals (input only), but is internally loaded to match the load of the bidirectional DQ , UDQS and LDQS signals.

Functional Description

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268, 435, 456 bits. The 256Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a *2n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following criteria must be met:

No power sequencing is specified during power up or power down given the following criteria:
V_{DD} and V_{DDQ} are driven from a single power converter output AND
V_{TT} meets the specification AND
V_{REF} tracks $V_{DDQ}/2$
or
The following relationship must be followed:
V_{DDQ} is driven after or with V_{DD} such that $V_{DDQ} < V_{DD} + 0.3$ V
V_{TT} is driven after or with V_{DDQ} such that $V_{TT} < V_{DDQ} + 0.3$V
V_{REF} is driven after or with V_{DDQ} such that $V_{REF} < V_{DDQ} + 0.3$V

The DQ and DQS outputs are in the High-Z state, where they remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200µs delay prior to applying an executable command.

Once the 200µs delay has been satisfied, a Deselect or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a Precharge ALL command should be applied. Next a Mode Register Set command should be issued for the Extended Mode Register, to enable the DLL, then a Mode Register Set command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any executable command. During the 200 cycles of clock for DLL locking, a Deselect or NOP command must be applied. After the 200 clock cycles, a Precharge ALL command should be applied, placing the device in the “all banks idle” state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

Register Definition

Mode Register

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode. The Mode Register is programmed via the Mode Register Set command (with BA0 = 0 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Mode Register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 specify the operating mode.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements results in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2-Ai when the burst length is set to four and by A3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

Mode Register Operation

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0*	0*	Operating Mode						CAS Latency			BT	Burst Length			Mode Register

A12 - A9	A8	A7	A6 - A0	Operating Mode
0	0	0	Valid	Normal operation Do not reset DLL
0	1	0	Valid	Normal operation in DLL Reset
0	0	1		Reserved
–	–	–		Reserved

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (optional)
1	0	0	Reserved
1	0	1	1.5 (optional)
1	1	0	2.5
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

***** BA0 and BA1 must be 0, 0 to select the Mode Register (vs. the Extended Mode Register).

Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:

1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in *Burst Definition* on page 12.

Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2, 2.5 or 3 clocks. CAS latency of 1.5 is an optional feature on this device.

If a Read command is registered at clock edge n, and the latency is *m* clocks, the data is available nominally coincident with clock edge *n* + m.

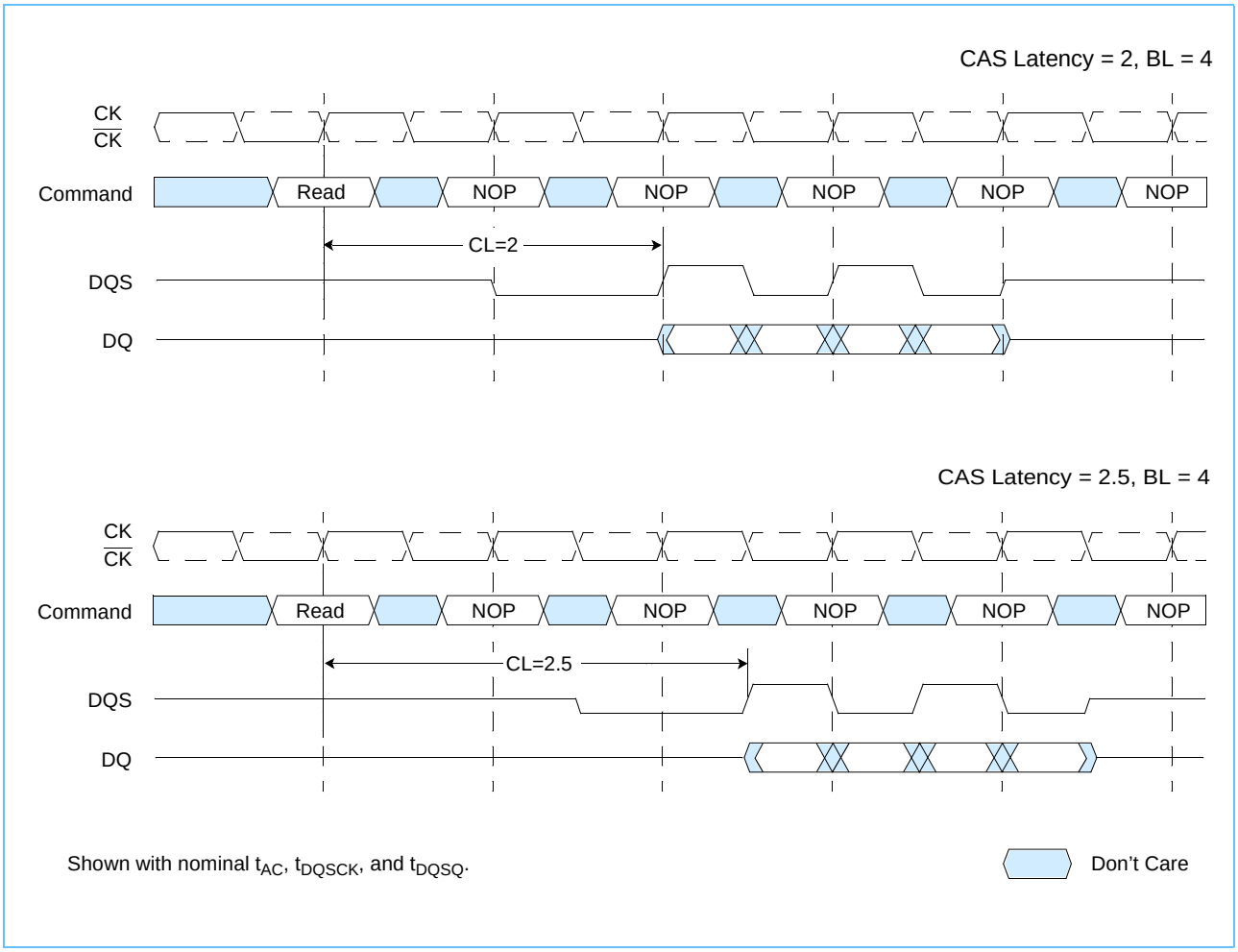
Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

Required CAS Latencies



Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, and output drive strength selection (optional). These functions are controlled via the bits shown in the Extended Mode Register Definition. The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 1 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation.

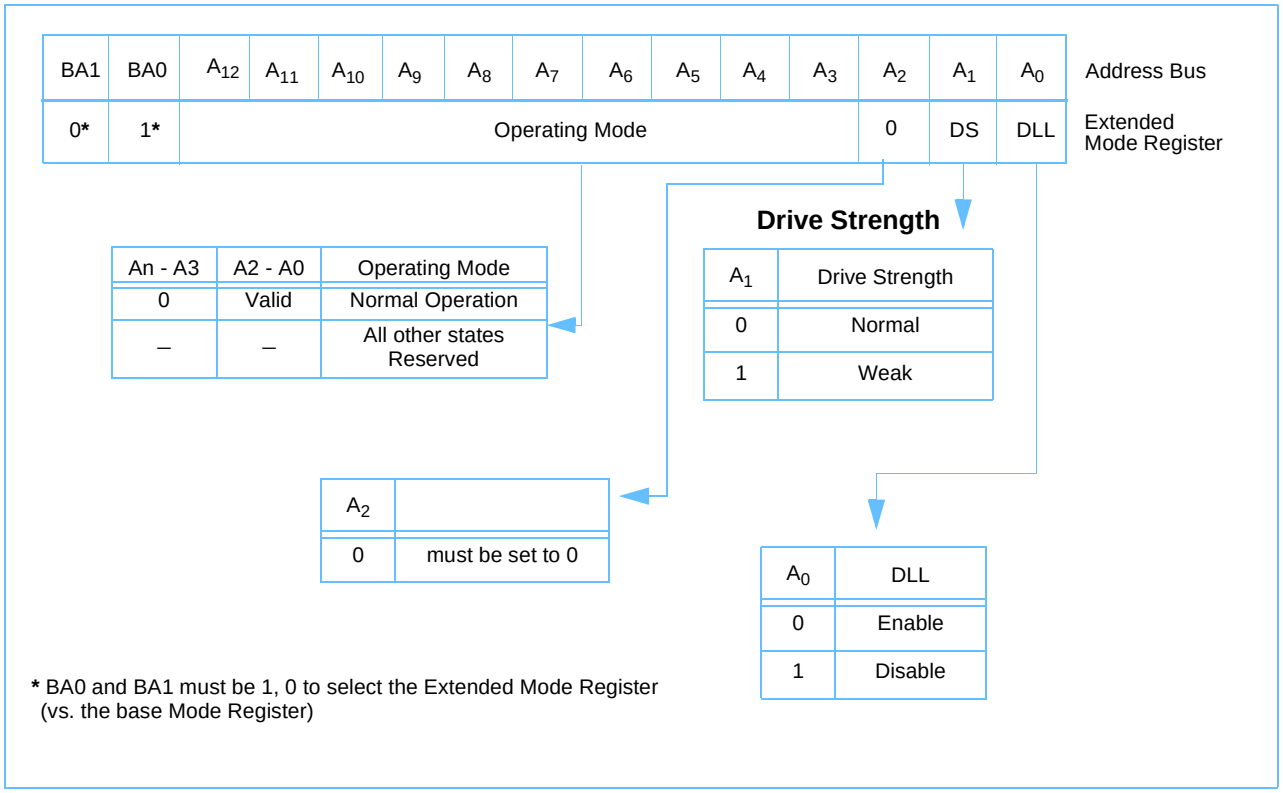
DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur before a Read command can be issued. This is the reason 200 clock cycles must occur before issuing a Read or Write command upon exit of self refresh operation.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. In addition this design version supports a weak driver mode for lighter load and/or point-to-point environments which can be activated during mode register set. I-V curves for the normal and weak drive strength are included in this document.

Extended Mode Register Definition



Commands

CommandsDeselect

The Deselect function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

No Operation (NOP)

The No Operation (NOP) command is used to perform a NOP to a DDR SDRAM. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Mode Register Set

The mode registers are loaded via inputs A0-A12, BA0 and BA1. See mode register descriptions in the Register Definition section. The Mode Register Set command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.

Active

The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a Precharge (or Read or Write with Auto Precharge) is issued to that bank. A Precharge (or Read or Write with Auto Precharge) command must be issued and completed before opening a different row in the same bank.

Read

The Read command is used to initiate a burst read access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 8, j = don't care] for x16, [i = 9, j = don't care] for x8 and [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Read burst; if Auto Precharge is not selected, the row remains open for subsequent accesses.

Write

The Write command is used to initiate a burst write access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 9, j = don't care] for x8; where [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Write burst; if Auto Precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data is written to memory; if the DM signal is registered high, the corresponding data inputs are ignored, and a Write is not executed to that byte/column location.

Precharge

The Precharge command is used to deactivate (close) the open row in a particular bank or the open row(s) in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any

Read or Write commands being issued to that bank. A precharge command is treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

Auto Precharge

Auto Precharge is a feature which performs the same individual-bank precharge functions described above, but without requiring an explicit command. This is accomplished by using A10 to enable Auto Precharge in conjunction with a specific Read or Write command. A precharge of the bank/row that is addressed with the Read or Write command is automatically performed upon completion of the Read or Write burst. Auto Precharge is nonpersistent in that it is either enabled or disabled for each individual Read or Write command. Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge (t_{RP}) is completed. This is determined as if an explicit Precharge command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

Burst Terminate

The Burst Terminate command is used to truncate read bursts (with Auto Precharge disabled). The most recently registered Read command prior to the Burst Terminate command is truncated, as shown in the Operation section of this data sheet.

Auto Refresh

Auto Refresh is used during normal operation of the DDR SDRAM and is analogous to CAS Before RAS (CBR) Refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an Auto Refresh command. The 256Mb DDR SDRAM requires Auto Refresh cycles at an average periodic interval of 7.8 µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto Refresh commands can be posted in the system, meaning that the maximum absolute interval between any Auto Refresh command and the next Auto Refresh command is 9 * 7.8 µs (70.2µs). This maximum absolute interval is short enough to allow for DLL updates internal to the DDR SDRAM to be restricted to Auto Refresh cycles, without allowing too much drift in t_{AC} between updates.

Self Refresh

The Self Refresh command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The Self Refresh command is initiated as an Auto Refresh command coincident with CKE transitioning low. The DLL is automatically disabled upon entering Self Refresh, and is automatically enabled upon exiting Self Refresh (200 clock cycles must then occur before a Read command can be issued). Input signals except CKE (low) are “Don’t Care” during Self Refresh operation.

The procedure for exiting self refresh requires a sequence of commands. CK (and $\overline{CK}$) must be stable prior to CKE returning high. Once CKE is high, the SDRAM must have NOP commands issued for t_{XSNR} because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

Truth Table 1a: Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	MNE	Notes
Deselect (Nop)	H	X	X	X	X	NOP	1, 9
No Operation (Nop)	L	H	H	H	X	NOP	1, 9
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	ACT	1, 3
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	Read	1, 4
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	Write	1, 4
Burst Terminate	L	H	H	L	X	BST	1, 8
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	PRE	1, 5
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR / SR	1, 6, 7
Mode Register Set	L	L	L	L	Op-Code	MRS	1, 2

1. CKE is HIGH for all commands shown except Self Refresh.
2. BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register.)
3. BA0-BA1 provide bank address and A0-A12 provide row address.
4. BA0, BA1 provide bank address; A0-A*i* provide column address (where *i* = 8for x16, *i* = 9 for x8 and 9, 11 for x4); A10 HIGH enables the Auto Precharge feature (nonpersistent), A10 LOW disables the Auto Precharge feature.
5. A10 LOW: BA0, BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH; Self Refresh if CKE is LOW.
7. Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts
9. Deselect and NOP are functionally interchangeable.

Truth Table 1b: DM Operation

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1
Write Inhibit	H	X	1

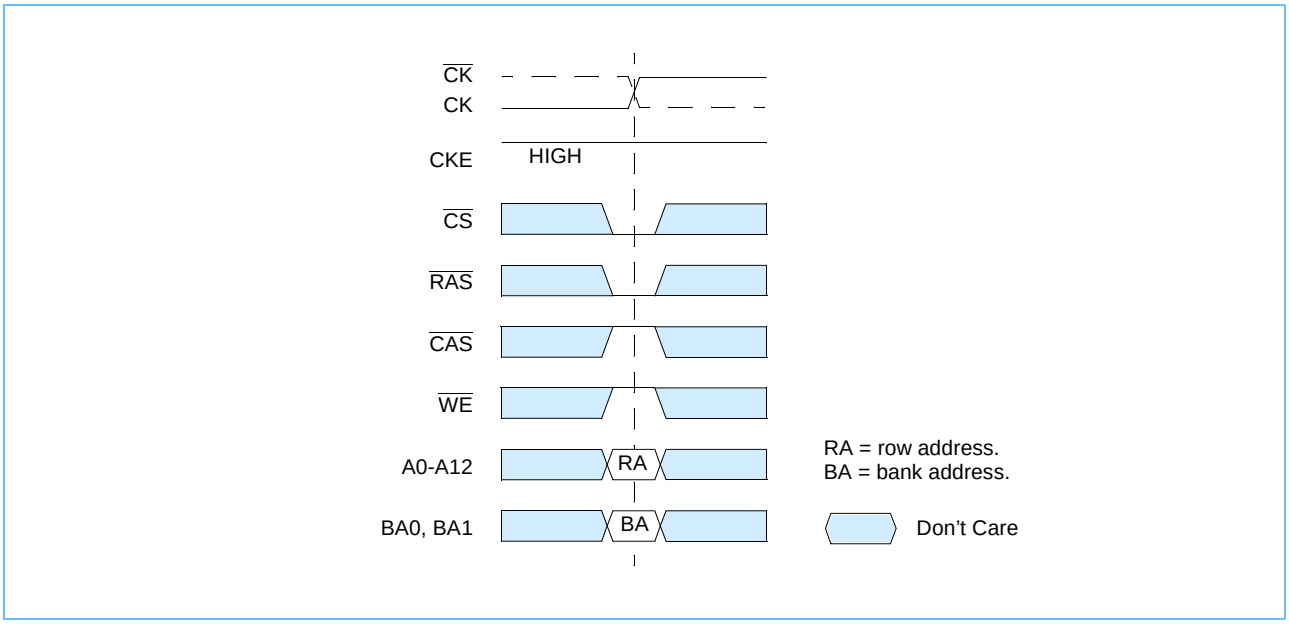
1. Used to mask write data; provided coincident with the corresponding data.

Operations

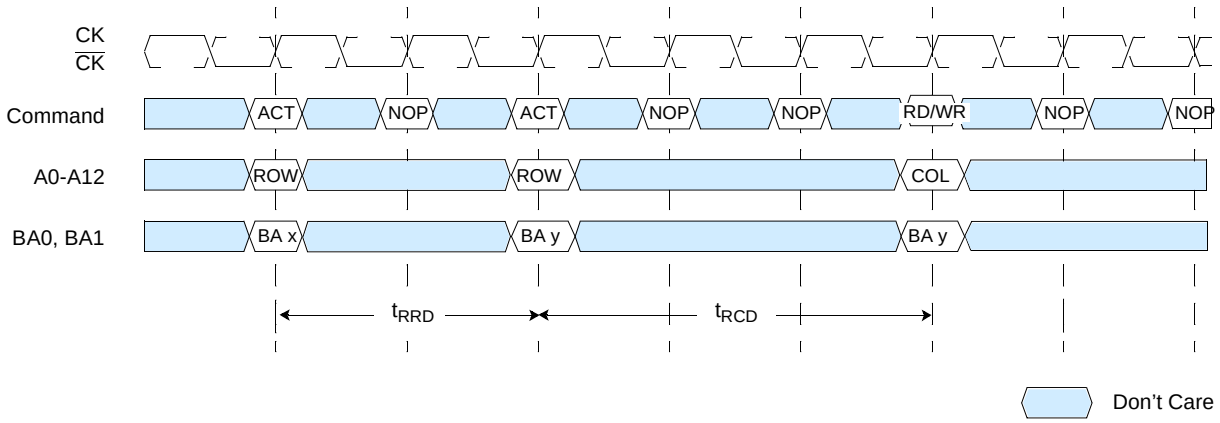
Bank/Row Activation

Before any Read or Write commands can be issued to a bank within the DDR SDRAM, a row in that bank must be “opened” (activated). This is accomplished via the Active command and addresses A0-A12, BA0 and BA1 (see Activating a Specific Row in a Specific Bank), which decode and select both the bank and the row to be activated. After opening a row (issuing an Active command), a Read or Write command may be issued to that row, subject to the t_{RCD} specification. A subsequent Active command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive Active commands to the same bank is defined by t_{RC}. A subsequent Active command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive Active commands to different banks is defined by t_{RRD}.

Activating a Specific Row in a Specific Bank



t_{RCD} and t_{RRD} Definition



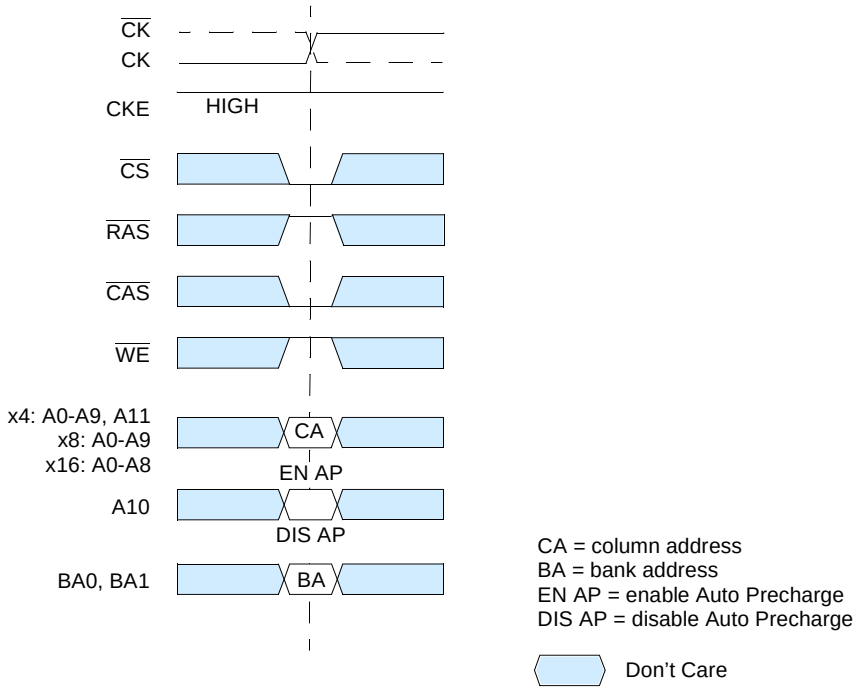
Reads

Subsequent to programming the mode register with CAS latency, burst type, and burst length, Read bursts are initiated with a Read command, as shown on *Read Command* on page 21.

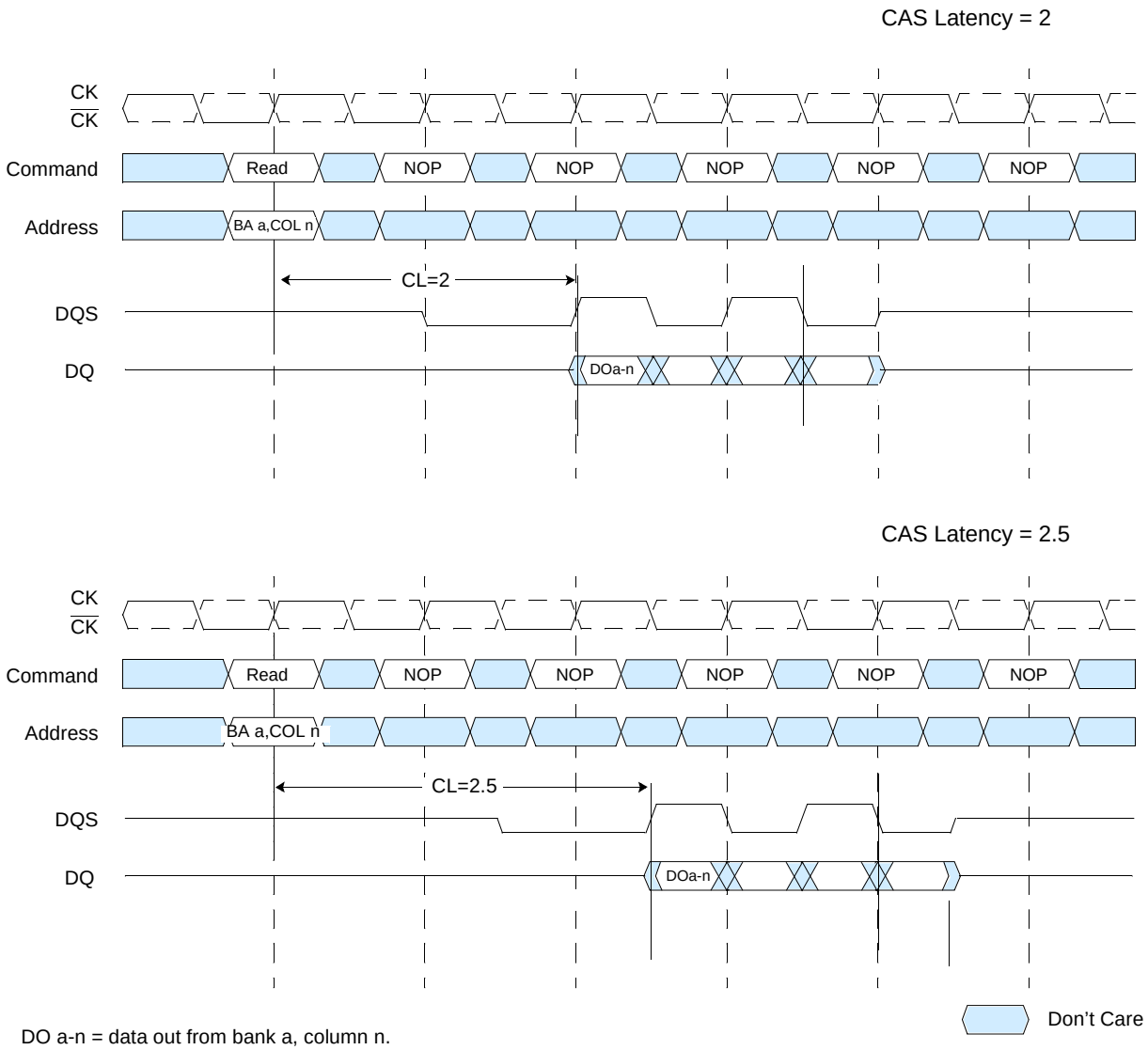
The starting column and bank addresses are provided with the Read command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row that is accessed starts precharge at the completion of the burst, provided t_{RAS} has been satisfied. For the generic Read commands used in the following illustrations, Auto Precharge is disabled.

During Read bursts, the valid data-out element from the starting column address is available following the CAS latency after the Read command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CK and $\overline{CK}$). *Read Burst: CAS Latencies (Burst Length = 4)* on page 22 shows general timing for each supported CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial low state on DQS is known as the read preamble; the low state coincident with the last data-out element is known as the read postamble. Upon completion of a burst, assuming no other commands have been initiated, the DQs goes High-Z. Data from any Read burst may be concatenated with or truncated with data from a subsequent Read command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Read command should be issued x cycles after the first Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown on *Consecutive Read Bursts: CAS Latencies (Burst Length = 4 or 8)* on page 23. A Read command can be initiated on any clock cycle following a previous Read command. Nonconsecutive Read data is illustrated on *Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)* on page 24. Full-speed Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8) within a page (or pages) can be performed as shown on page 25.

Read Command

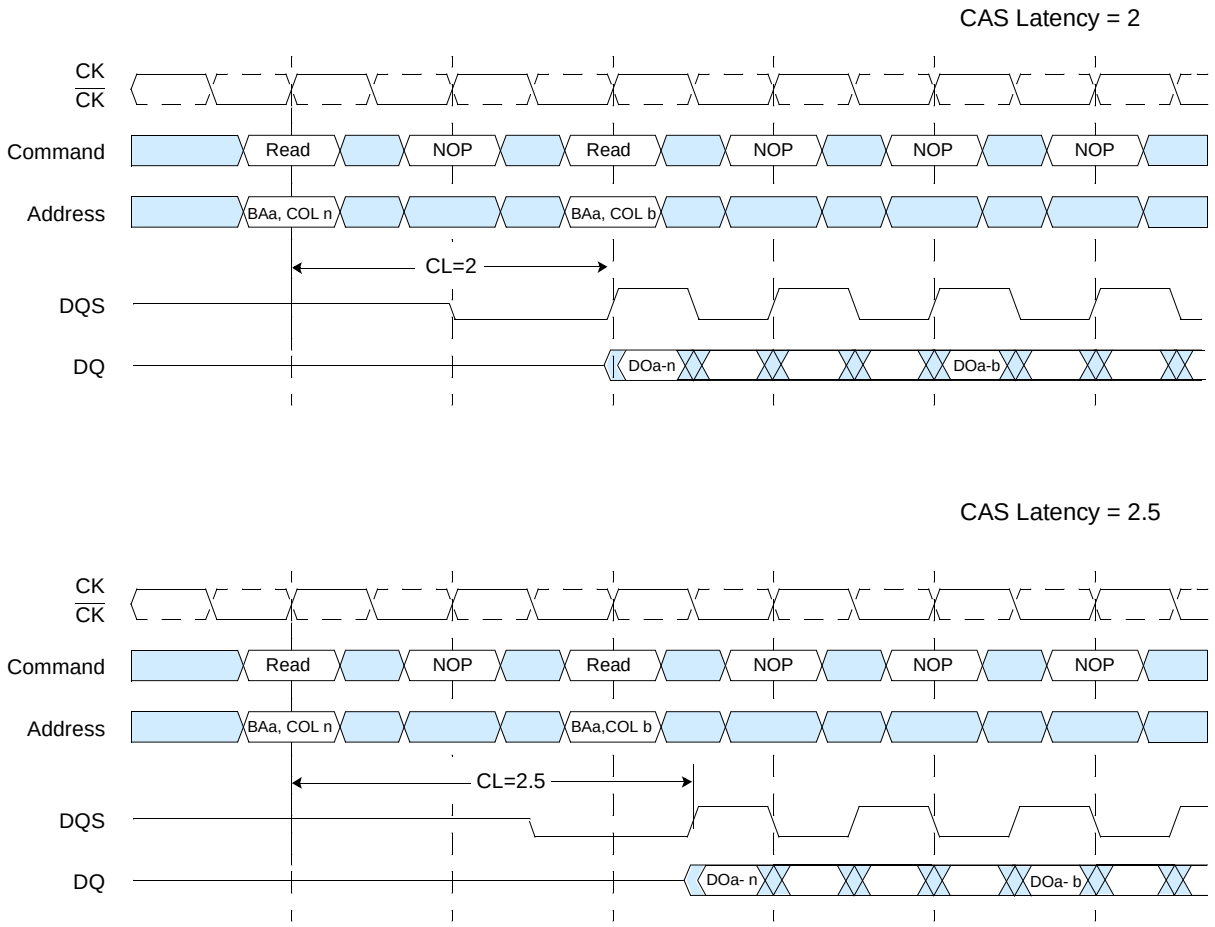


Read Burst: CAS Latencies (Burst Length = 4)



DO a-n = data out from bank a, column n.
3 subsequent elements of data out appear in the programmed order following DO a-n.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Consecutive Read Bursts: CAS Latencies (Burst Length = 4 or 8)

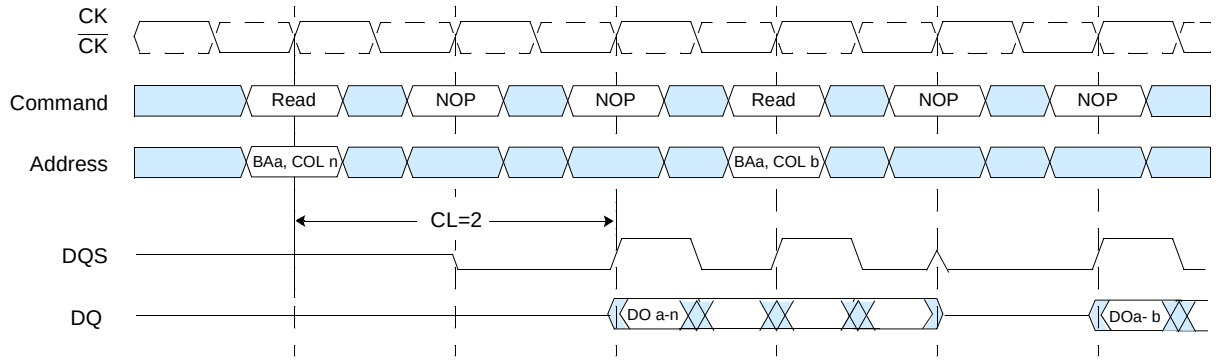


DO a-n (or a-b) = data out from bank a, column n (or bank a, column b).
When burst length = 4, the bursts are concatenated.
When burst length = 8, the second burst interrupts the first.
3 subsequent elements of data out appear in the programmed order following DO a-n.
3 (or 7) subsequent elements of data out appear in the programmed order following DO a-b.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

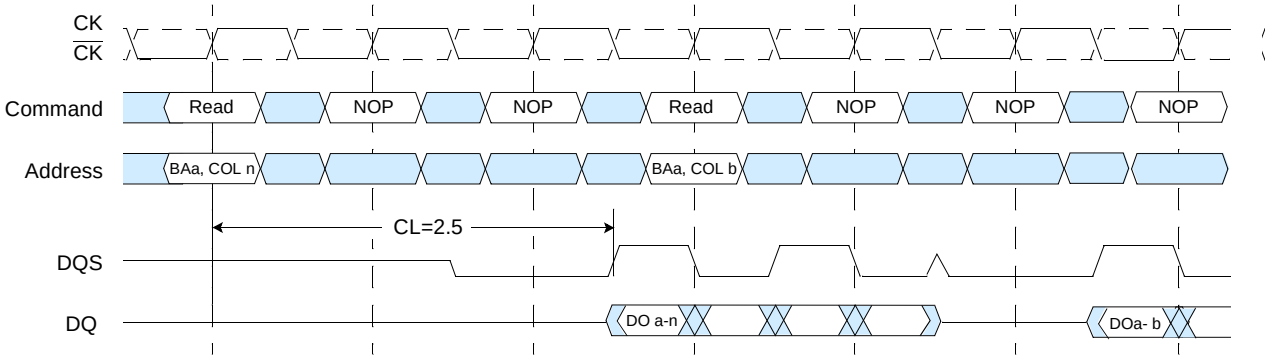
Don't Care

Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)

CAS Latency = 2



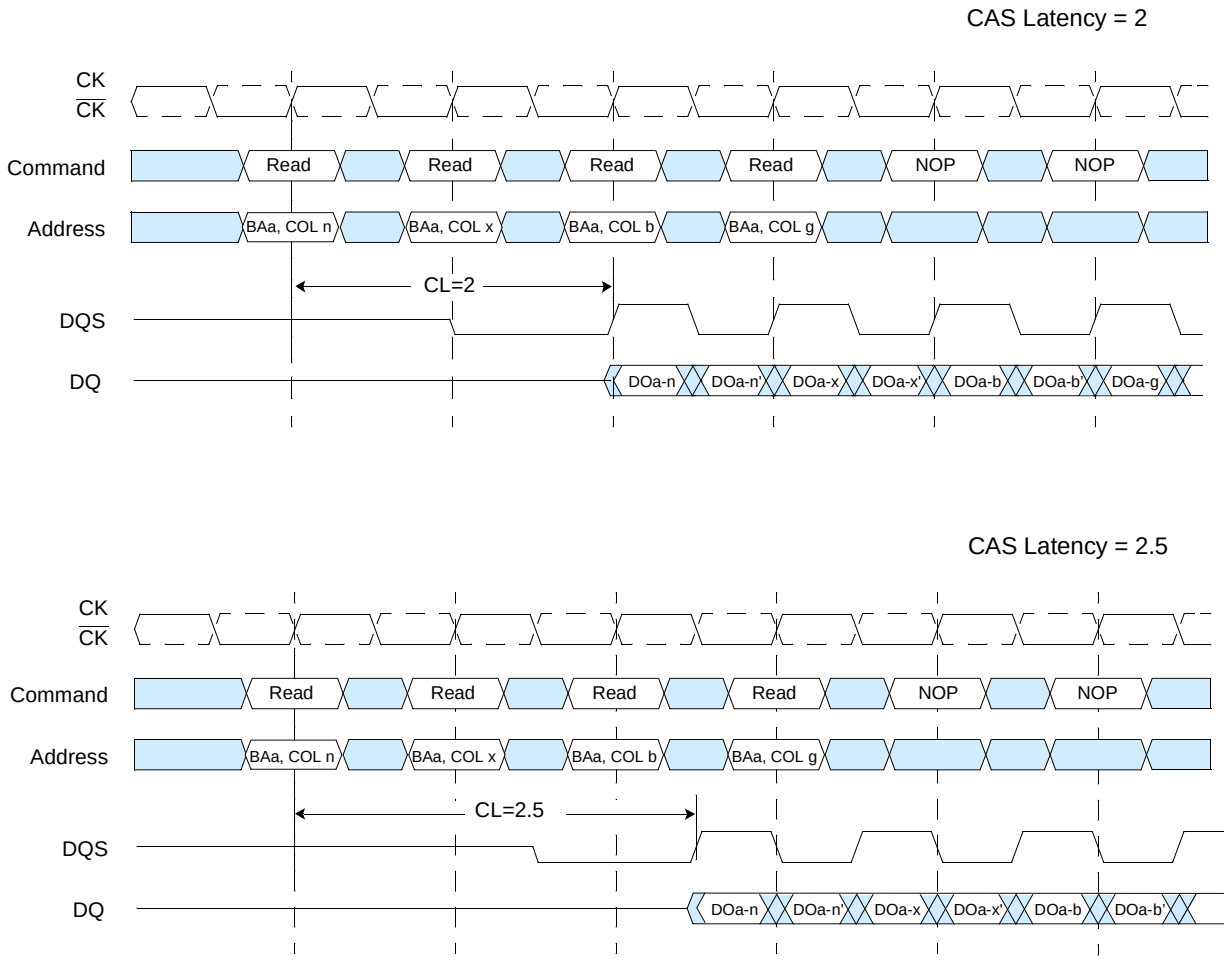
CAS Latency = 2.5



DO a-n (or a-b) = data out from bank a, column n (or bank a, column b).
3 subsequent elements of data out appear in the programmed order following DO a-n (and following DO a-b).
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8)



DO a-n, etc. = data out from bank a, column n etc.
n' etc. = odd or even complement of n, etc. (i.e., column address LSB inverted).
Reads are to active rows in any banks.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

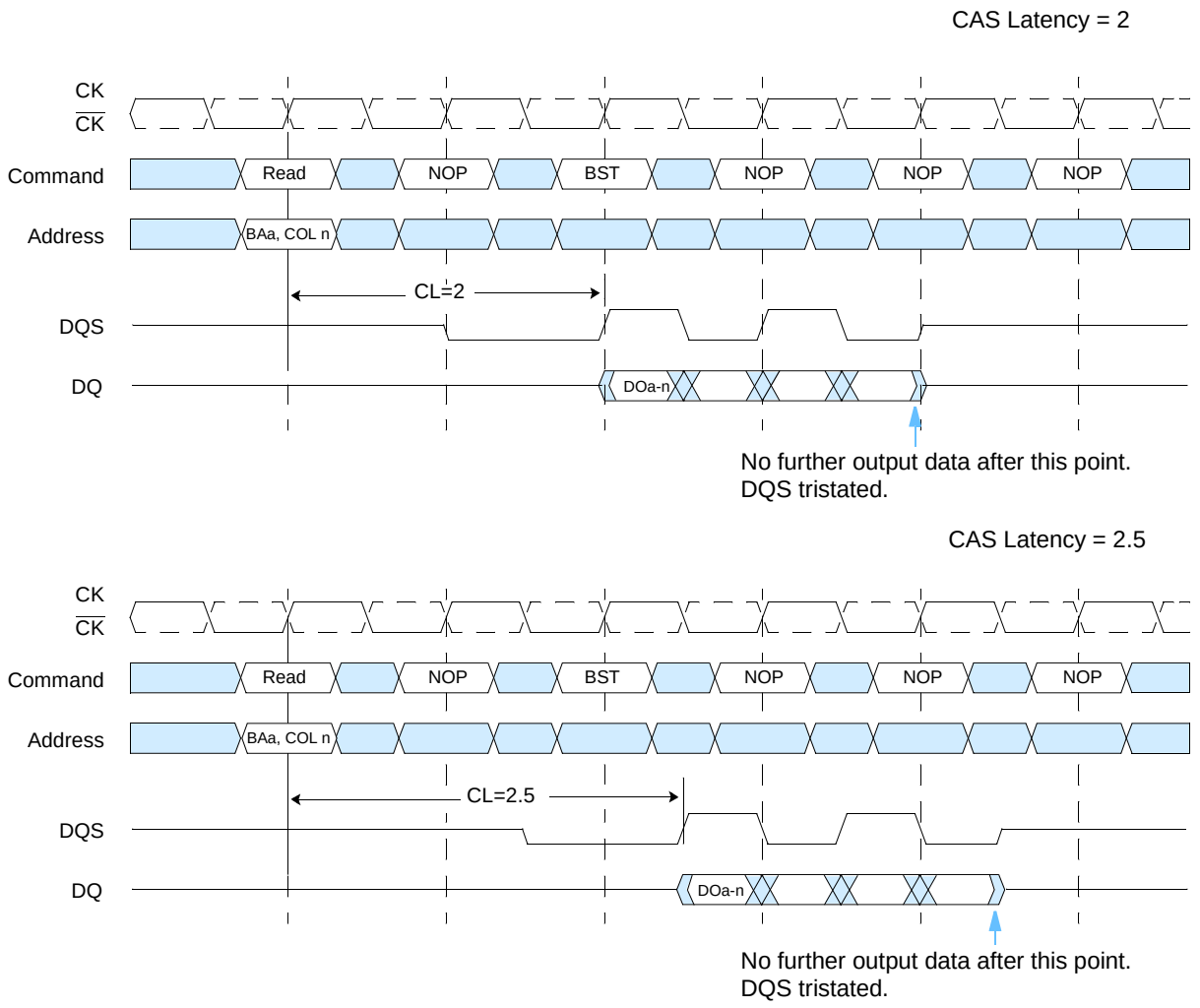
Data from any Read burst may be truncated with a Burst Terminate command, as shown on *Terminating a Read Burst: CAS Latencies (Burst Length = 8)* on page 27. The Burst Terminate latency is equal to the read (CAS) latency, i.e. the Burst Terminate command should be issued x cycles after the Read command, where x equals the number of desired data element pairs.

Data from any Read burst must be completed or truncated before a subsequent Write command can be issued. If truncation is necessary, the Burst Terminate command must be used, as shown on *Read to Write: CAS Latencies (Burst Length = 4 or 8)* on page 28. The example is shown for t_{DQSS}(min). The t_{DQSS}(max) case, not shown here, has a longer bus idle time. t_{DQSS}(min) and t_{DQSS}(max) are defined in the section on Writes.

A Read burst may be followed by, or truncated with, a Precharge command to the same bank (provided that Auto Precharge was not activated). The Precharge command should be issued x cycles after the Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown on *Read to Precharge: CAS Latencies (Burst Length = 4 or 8)* on page 29 for Read latencies of 2 and 2.5. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a Read being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same Read burst with Auto Precharge enabled. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

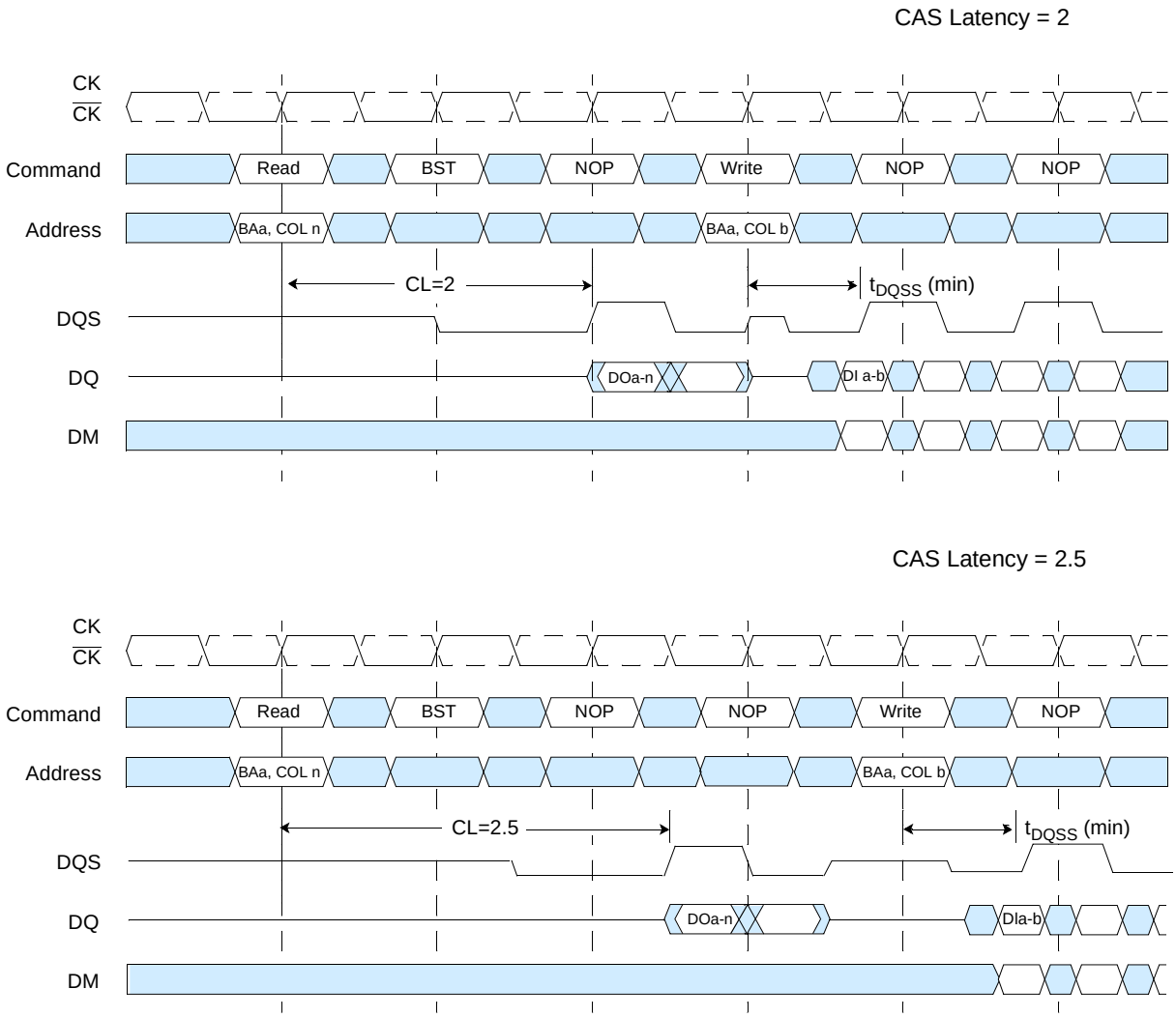
Terminating a Read Burst: CAS Latencies (Burst Length = 8)



DO a-n = data out from bank a, column n.
Cases shown are bursts of 8 terminated after 4 data elements.
3 subsequent elements of data out appear in the programmed order following DO a-n.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

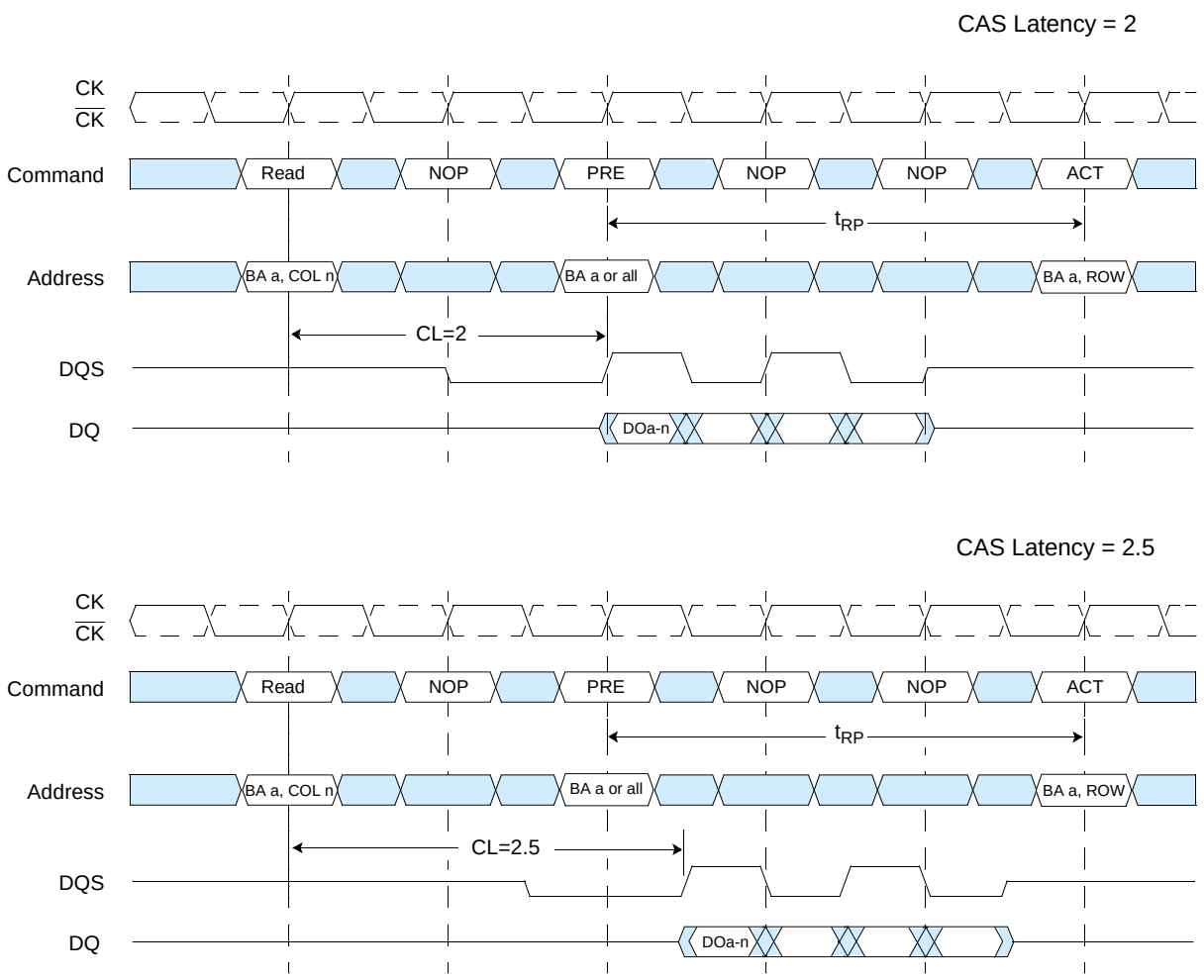
Read to Write: CAS Latencies (Burst Length = 4 or 8)



DO a-n = data out from bank a, column n
DI a-b = data in to bank a, column b
1 subsequent elements of data out appear in the programmed order following DO a-n.
Data In elements are applied following DI a-b in the programmed order, according to burst length.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

Read to Precharge: CAS Latencies (Burst Length = 4 or 8)



DO a-n = data out from bank a, column n.
Cases shown are either uninterrupted bursts of 4 or interrupted bursts of 8.
3 subsequent elements of data out appear in the programmed order following DO a-n.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

Writes

Write bursts are initiated with a Write command, as shown on *Write Command* on page 31.

The starting column and bank addresses are provided with the Write command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Write commands used in the following illustrations, Auto Precharge is disabled.

During Write bursts, the first valid data-in element is registered on the first rising edge of DQS following the write command, and subsequent data elements are registered on successive edges of DQS. The Low state on DQS between the Write command and the first rising edge is known as the write preamble; the Low state on DQS following the last data-in element is known as the write postamble. The time between the Write command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range (from 75% to 125% of one clock cycle), so most of the Write diagrams that follow are drawn for the two extreme cases (i.e. t_{DQSS}(min) and t_{DQSS}(max)). *Write Burst (Burst Length = 4)* on page 32 shows the two extremes of t_{DQSS} for a burst of four. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS enters High-Z and any additional input data is ignored.

Data for any Write burst may be concatenated with or truncated with a subsequent Write command. In either case, a continuous flow of input data can be maintained. The new Write command can be issued on any positive edge of clock following the previous Write command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Write command should be issued x cycles after the first Write command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). *Write to Write (Burst Length = 4)* on page 33 shows concatenated bursts of 4. An example of non-consecutive Writes is shown on *Write to Write: Max DQSS, Non-Consecutive (Burst Length = 4)* on page 34. Full-speed random write accesses within a page or pages can be performed as shown on *Random Write Cycles (Burst Length = 2, 4 or 8)* on page 35. Data for any Write burst may be followed by a subsequent Read command. To follow a Write without truncating the write burst, t_{WTR} (Write to Read) should be met as shown on *Write to Read: Non-Interrupting (CAS Latency = 2; Burst Length = 4)* on page 36.

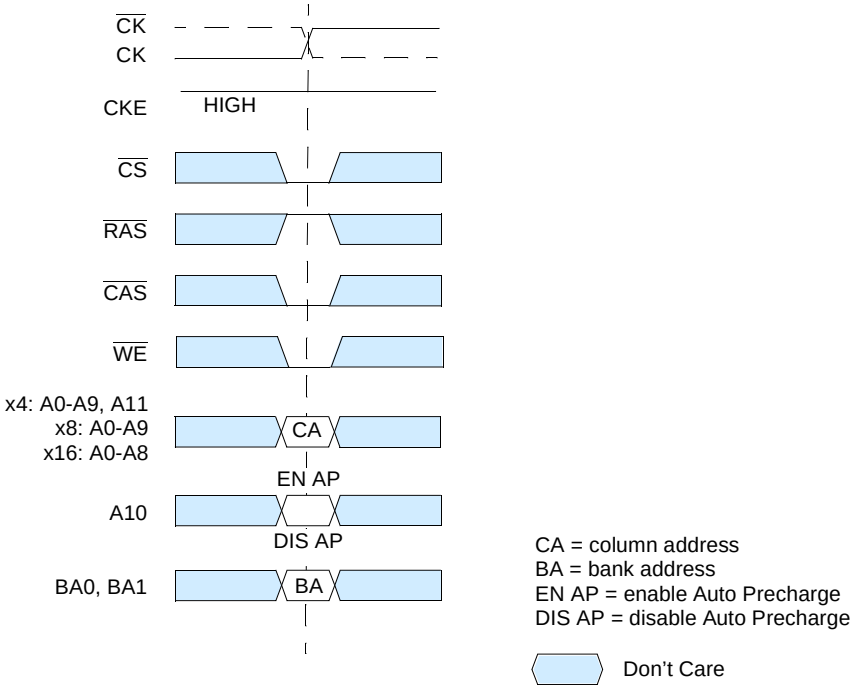
Data for any Write burst may be truncated by a subsequent Read command, as shown in the figures on *Write to Read: Interrupting (CAS Latency = 2; Burst Length = 8)* on page 37 to *Write to Read: Nominal DQSS, Interrupting (CAS Latency = 2; Burst Length = 8)* on page 39. Note that only the data-in pairs that are registered prior to the t_{WTR} period are written to the internal array, and any subsequent data-in must be masked with DM, as shown in the diagrams noted previously.

Data for any Write burst may be followed by a subsequent Precharge command. To follow a Write without truncating the write burst, t_{WR} should be met as shown on *Write to Precharge: Non-Interrupting (Burst Length = 4)* on page 40.

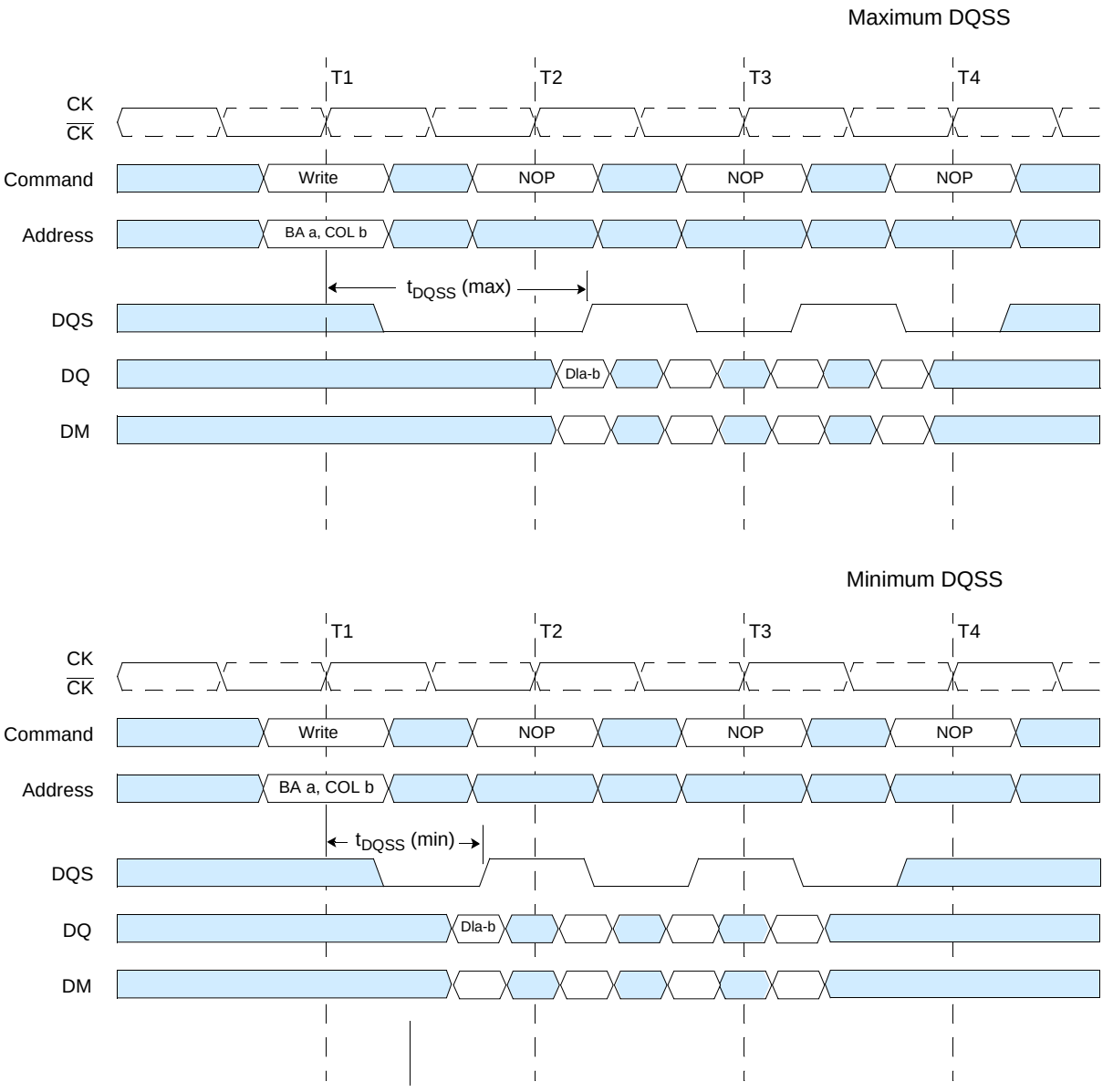
Data for any Write burst may be truncated by a subsequent Precharge command, as shown in the figures on *Write to Precharge: Interrupting (Burst Length = 4 or 8)* on page 41 to *Write to Precharge: Nominal DQSS (2 bit Write), Interrupting (Burst Length = 4 or 8)* on page 43. Note that only the data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any subsequent data in should be masked with DM. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

In the case of a Write burst being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same burst with Auto Precharge. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

Write Command



Write Burst (Burst Length = 4)

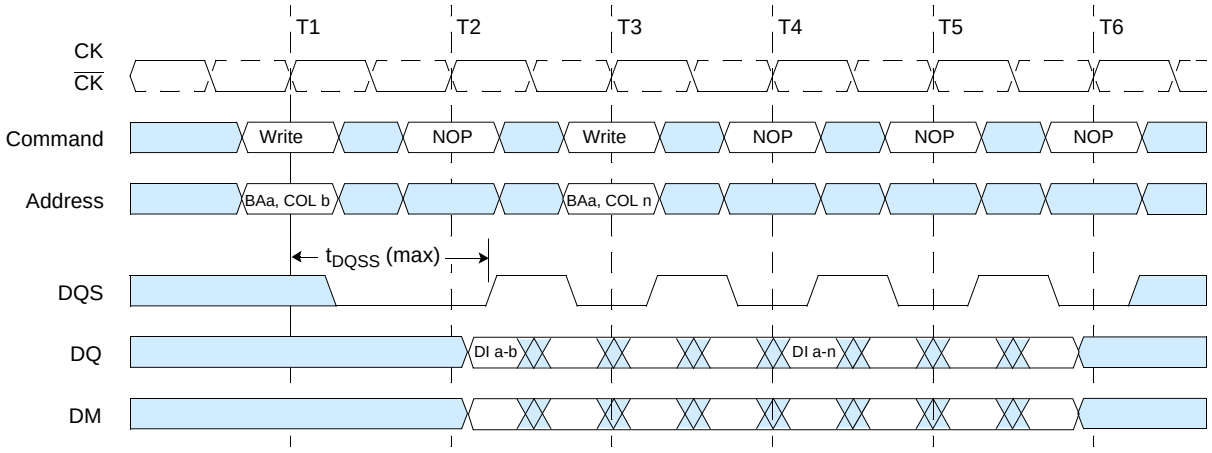


DI a-b = data in for bank a, column b.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
A non-interrupted burst is shown.
A10 is Low with the Write command (Auto Precharge is disabled).

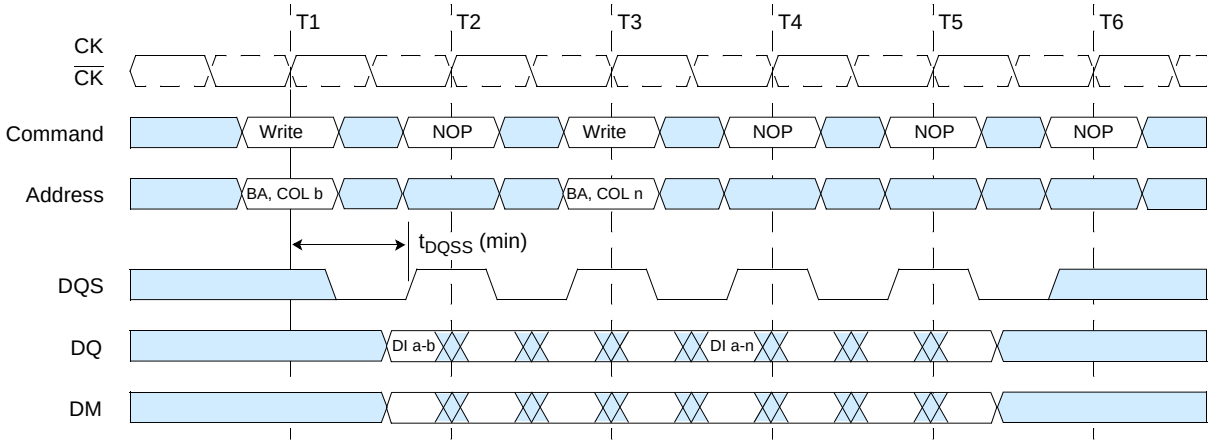
Don't Care

Write to Write (Burst Length = 4)

Maximum DQSS



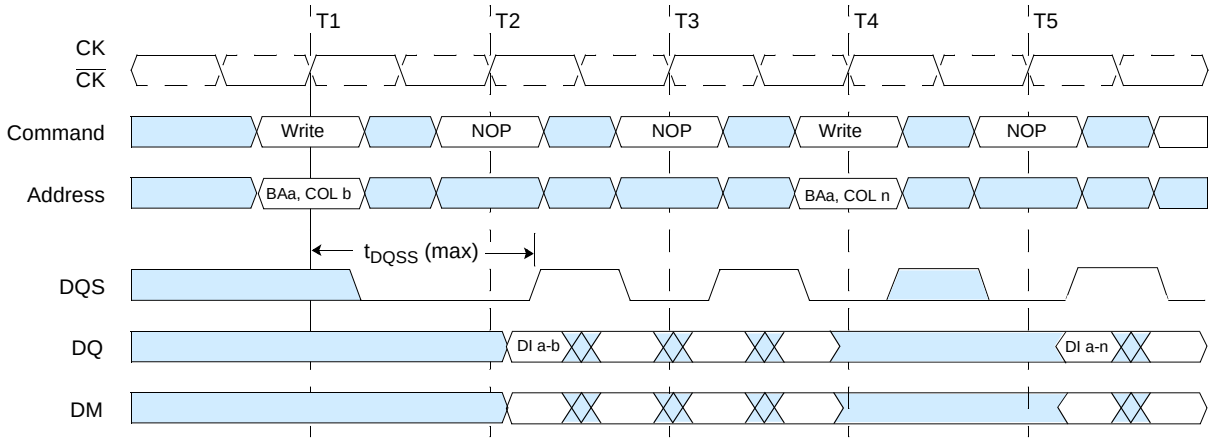
Minimum DQSS



DI a-b = data in for bank a, column b, etc.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
3 subsequent elements of data in are applied in the programmed order following DI a-n.
A non-interrupted burst is shown.
Each Write command may be to any bank.

Don't Care

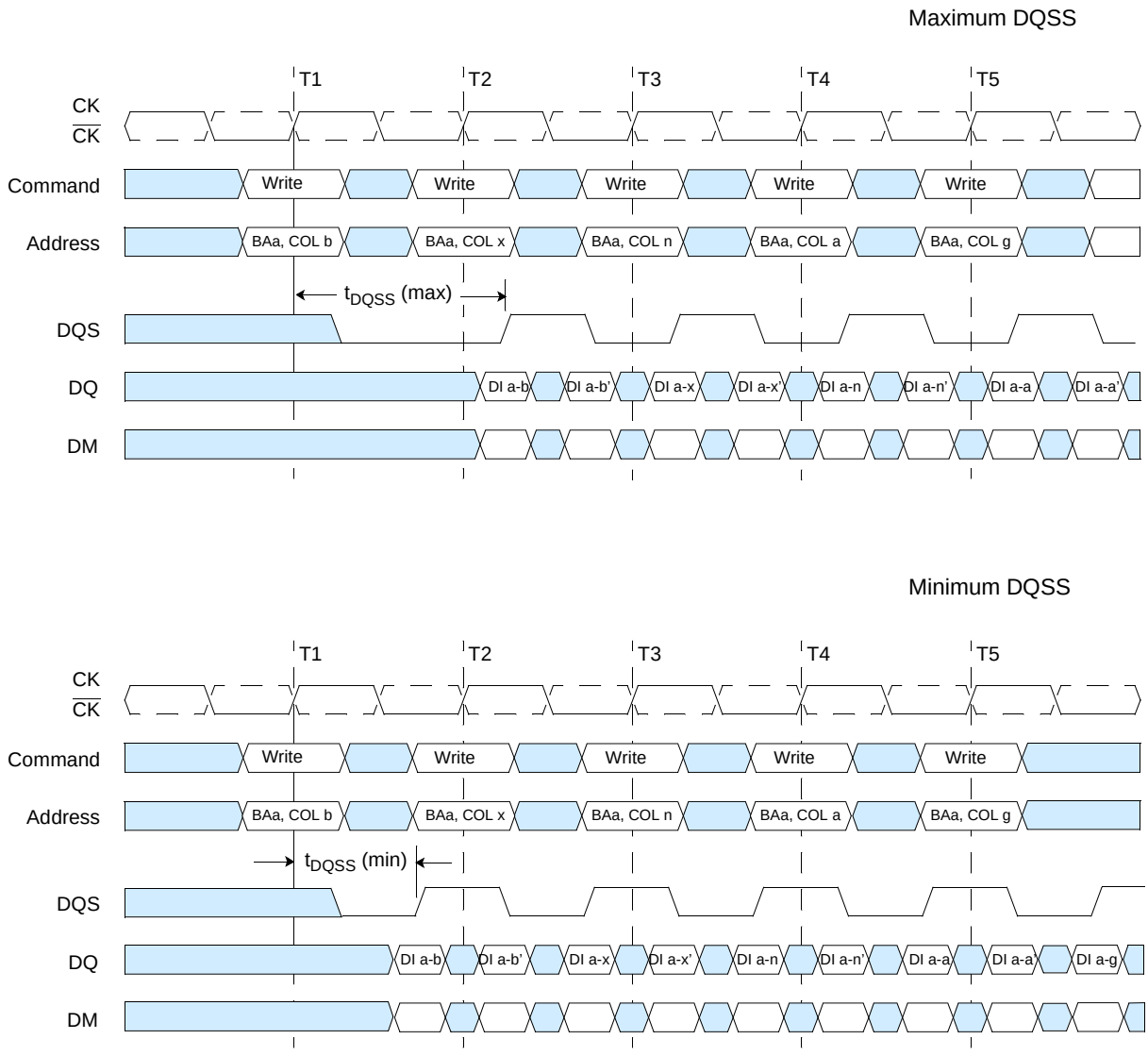
Write to Write: Max DQSS, Non-Consecutive (Burst Length = 4)



DI a-b, etc. = data in for bank a, column b, etc.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
3 subsequent elements of data in are applied in the programmed order following DI a-n.
A non-interrupted burst is shown.
Each Write command may be to any bank.

Don't Care

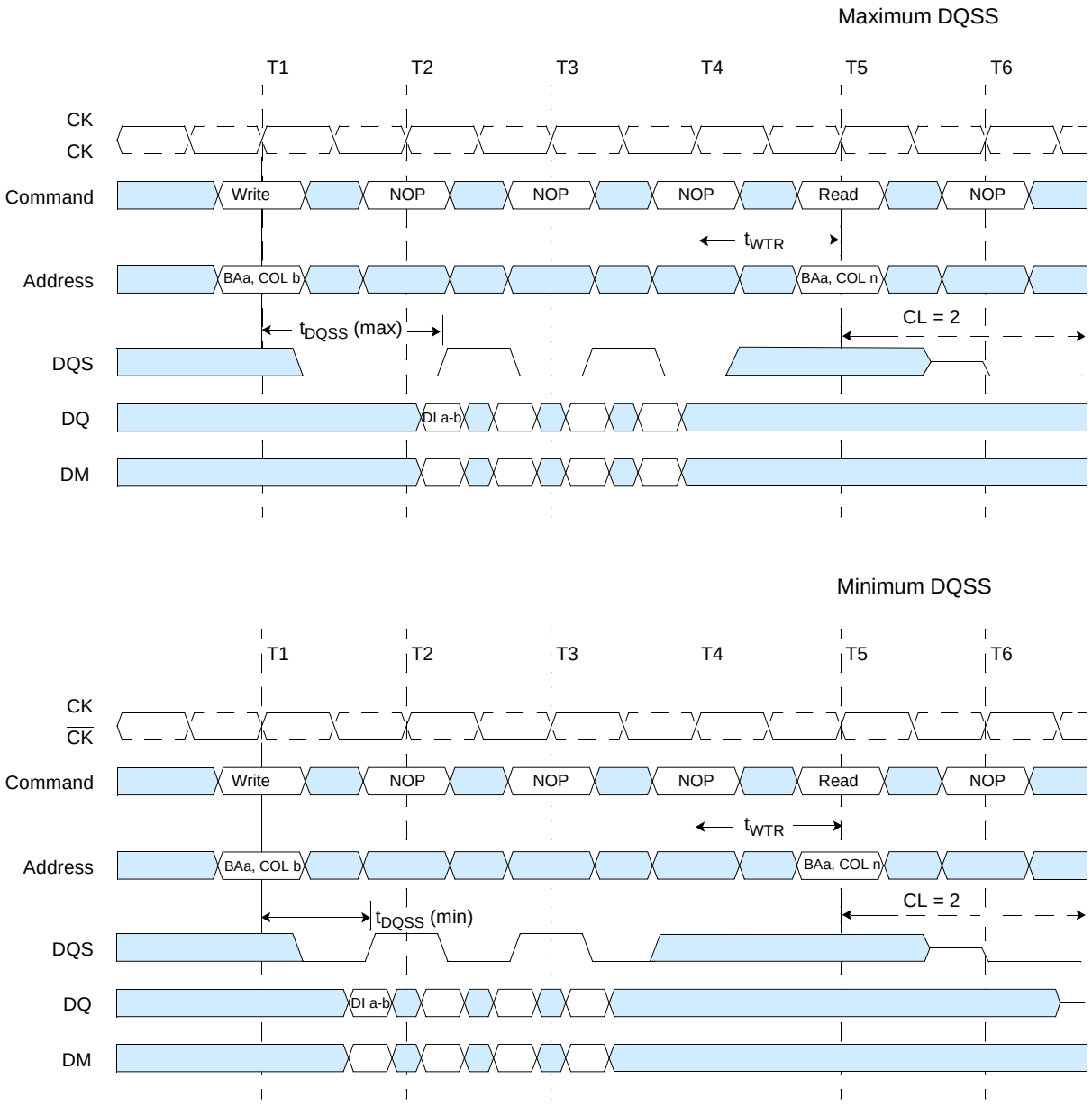
Random Write Cycles (Burst Length = 2, 4 or 8)



DI a-b, etc. = data in for bank a, column b, etc.
b', etc. = odd or even complement of b, etc. (i.e., column address LSB inverted).
Each Write command may be to any bank.

Don't Care

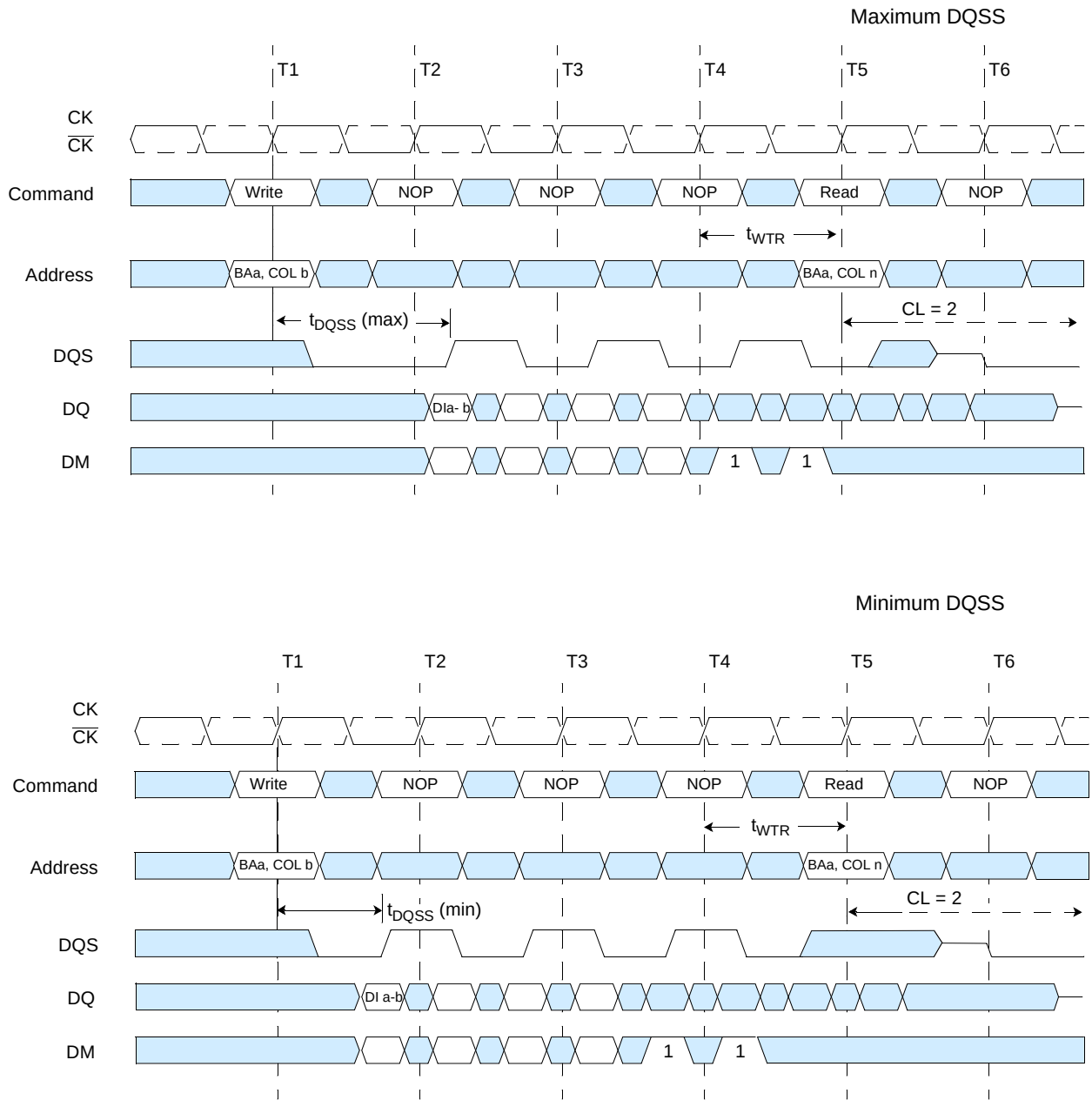
Write to Read: Non-Interrupting (CAS Latency = 2; Burst Length = 4)



DI a-b = data in for bank a, column b.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
A non-interrupted burst is shown.
t_{WTR} is referenced from the first positive CK edge after the last data in pair.
A10 is Low with the Write command (Auto Precharge is disabled).
The Read and Write commands may be to any bank.

Don't Care

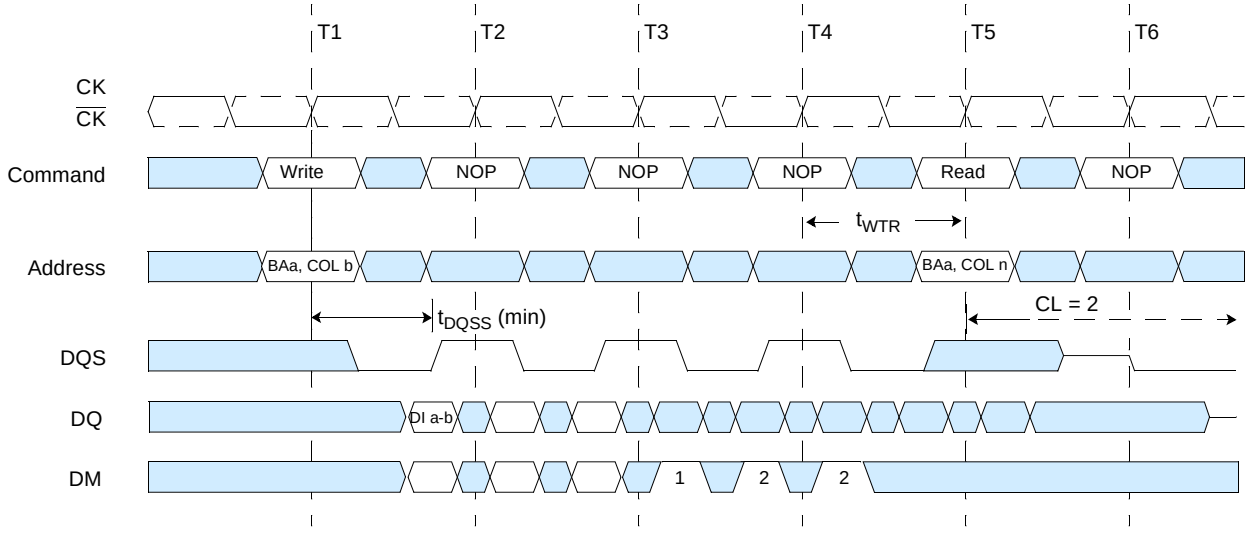
Write to Read: Interrupting (CAS Latency = 2; Burst Length = 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 4 data elements are written.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
t_{WTR} is referenced from the first positive CK edge after the last data in pair.
The Read command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
The Read and Write commands are not necessarily to the same bank.
1 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Write to Read: Minimum DQSS, Odd Number of Data (3 bit Write), Interrupting (CAS Latency = 2; Burst Length = 8)



DI a-b = data in for bank a, column b.

An interrupted burst is shown, 3 data elements are written.

2 subsequent elements of data in are applied in the programmed order following DI a-b.

t_{WTR} is referenced from the first positive CK edge after the last desired data in pair (not the last desired data in element)

The Read command masks the last 2 data elements in the burst.

A10 is Low with the Write command (Auto Precharge is disabled).

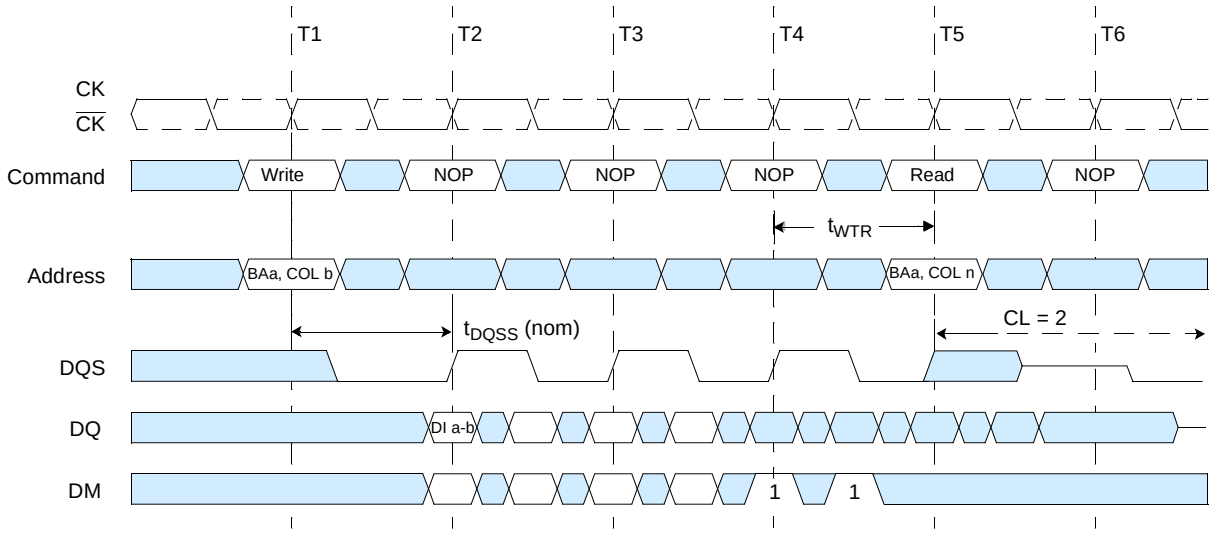
The Read and Write commands are not necessarily to the same bank.

1 = This bit is correctly written into the memory array if DM is low.

2 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

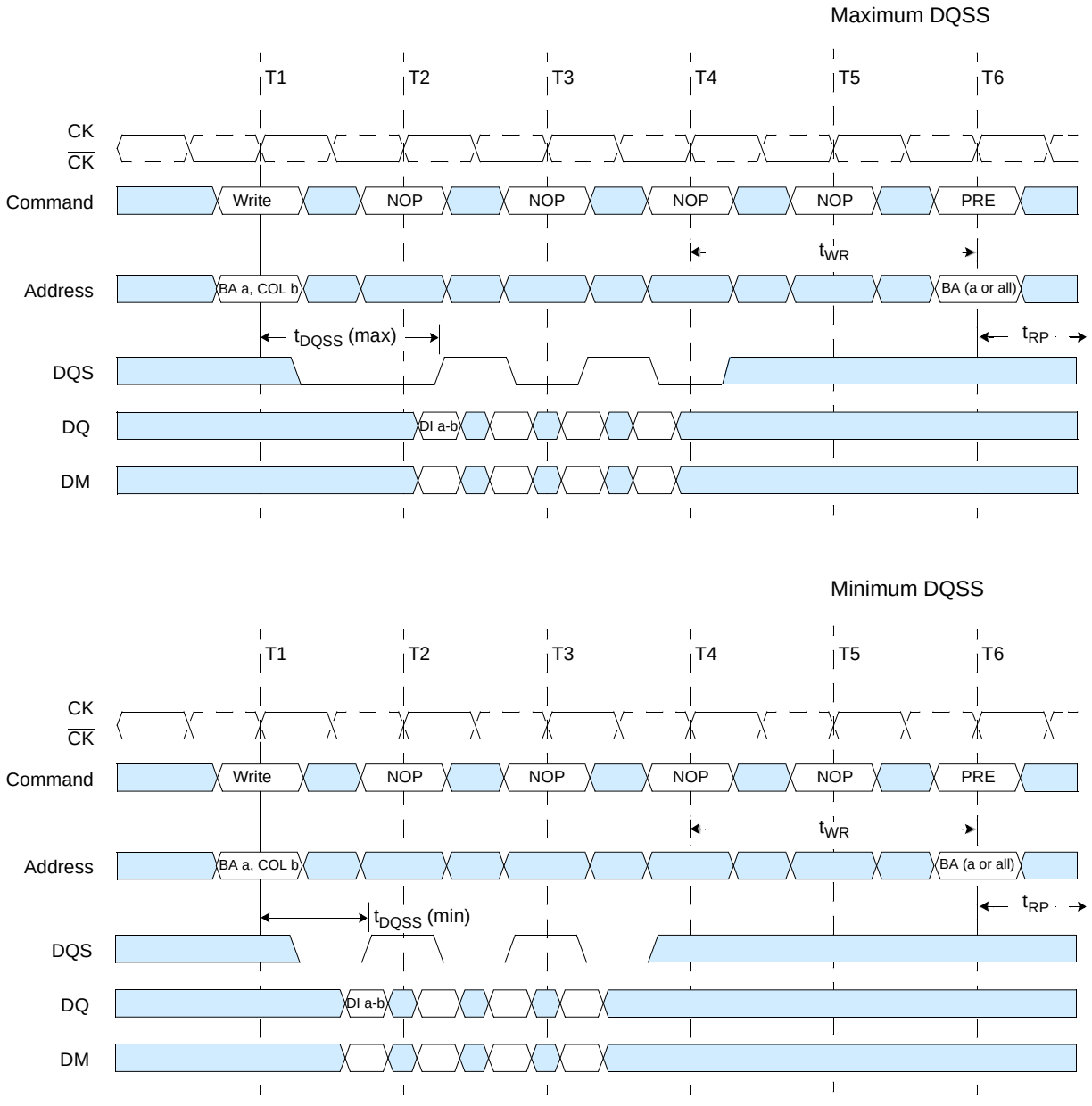
Write to Read: Nominal DQSS, Interrupting (CAS Latency = 2; Burst Length = 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 4 data elements are written.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
t_{WTR} is referenced from the first positive CK edge after the last desired data in pair.
The Read command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
The Read and Write commands are not necessarily to the same bank.
1 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

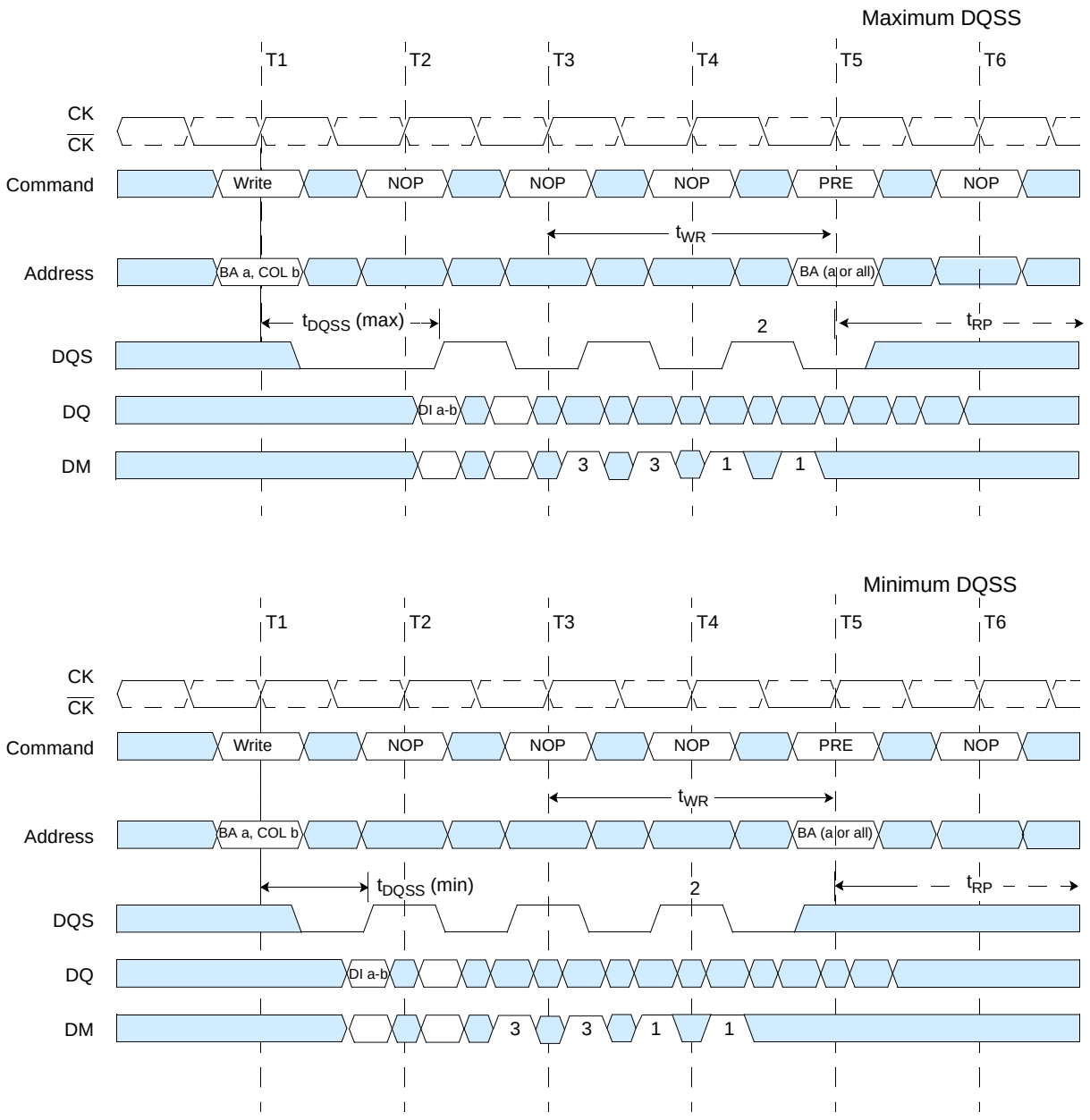
Write to Precharge: Non-Interrupting (Burst Length = 4)



DI a-b = data in for bank a, column b.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
A non-interrupted burst is shown.
t_{WR} is referenced from the first positive CK edge after the last data in pair.
A10 is Low with the Write command (Auto Precharge is disabled).

Don't Care

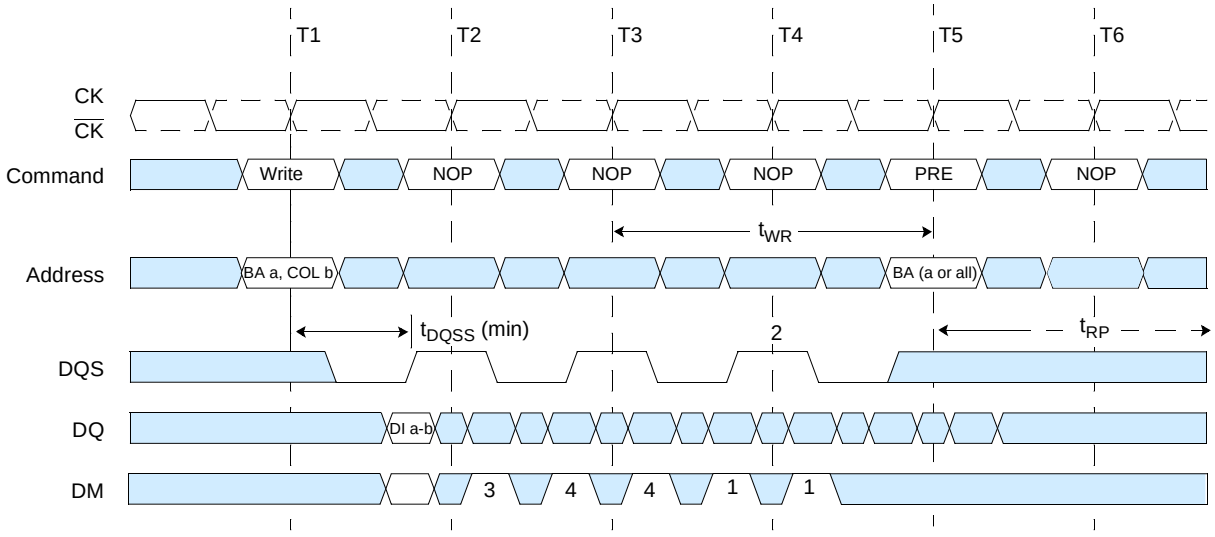
Write to Precharge: Interrupting (Burst Length = 4 or 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI a-b.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst, for burst length = 8.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

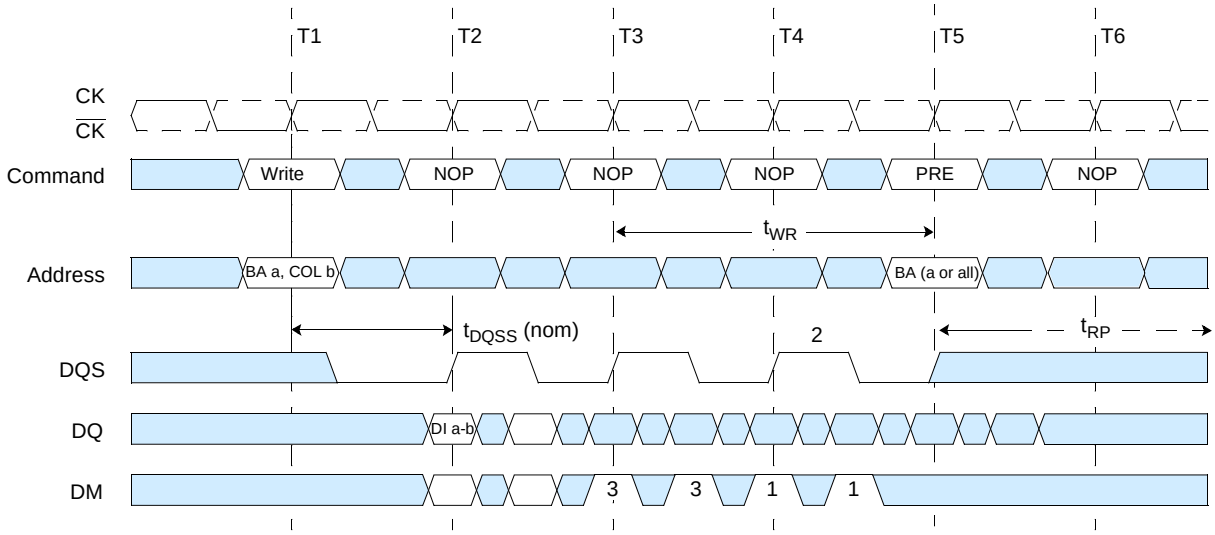
Write to Precharge: Minimum DQSS, Odd Number of Data (1 bit Write), Interrupting (Burst Length = 4 or 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 1 data element is written.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = This bit is correctly written into the memory array if DM is low.
4 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

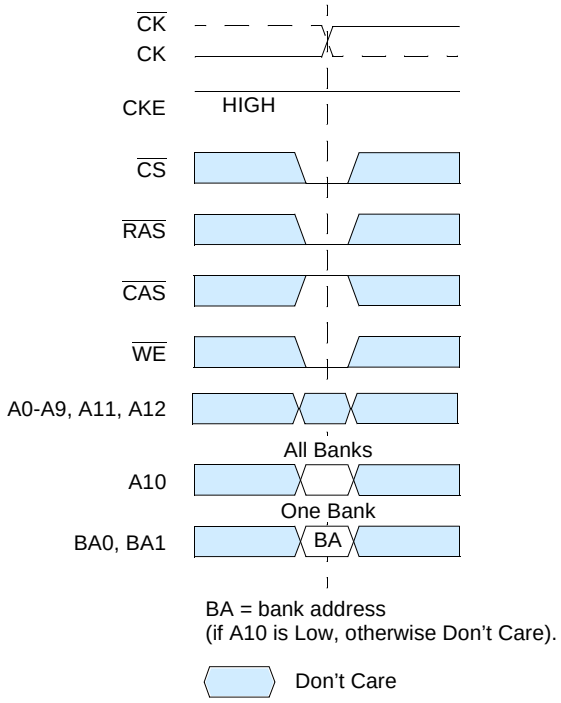
Write to Precharge: Nominal DQSS (2 bit Write), Interrupting (Burst Length = 4 or 8)



DI a-b = Data In for bank a, column b.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI a-b.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Precharge Command



Precharge

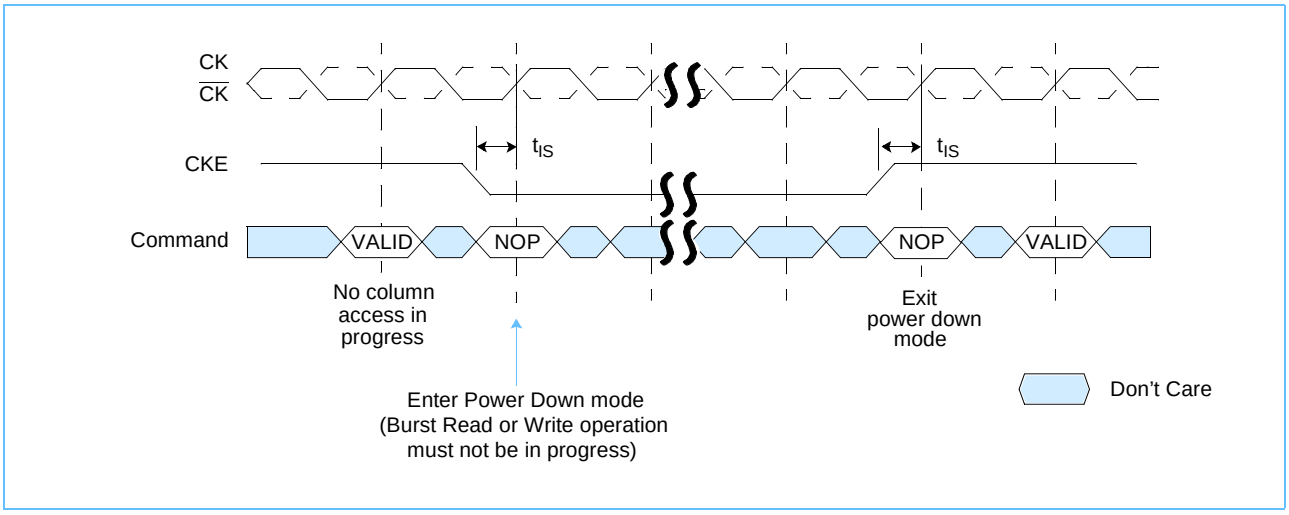
The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) is available for a subsequent row access some specified time (t_{RP}) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank.

Power-Down

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. The DLL is still running in Power Down mode, so for maximum power savings, the user has the option of disabling the DLL prior to entering Power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a Read command can be issued. In power-down mode, CKE Low and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are “Don’t Care”. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self refresh mode is preferred over the DLL-disabled power-down mode.

The power-down state is synchronously exited when CKE is registered HIGH (along with a Nop or Deselect command). A valid, executable command may be applied one clock cycle later.

Power Down



Truth Table 2: Clock Enable (CKE)

1. CKEn is the logic state of CKE at clock edge n: CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. COMMAND n is the command registered at clock edge n, and ACTION n is a result of COMMAND n.
4. All states and sequences not shown are illegal or reserved.

Current State	CKE n-1	CKEn	Command n	Action n	Notes
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	1
Power Down	L	L	X	Maintain Power-Down	
Power Down	L	H	Deselect or NOP	Exit Power-Down	
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	
All Banks Idle	H	L	AUTO REFRESH	Self Refresh Entry	
Bank(s) Active	H	L	Deselect or NOP	Active Power-Down Entry	
	H	H	See “Truth Table 3: Current State Bank n - Command to Bank n (Same Bank)” on page 47		

1. Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit (t_{XSNR}) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.

Truth Table 3: Current State Bank n - Command to Bank n (Same Bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation	1-6
	L	H	H	H	No Operation	NOP. Continue previous operation	1-6
Idle	L	L	H	H	Active	Select and activate row	1-6
	L	L	L	H	AUTO REFRESH		1-7
	L	L	L	L	MODE REGISTER SET		1-7
Row Active	L	H	L	H	Read	Select column and start Read burst	1-6, 10
	L	H	L	L	Write	Select column and start Write burst	1-6, 10
	L	L	H	L	Precharge	Deactivate row in bank(s)	1-6, 8
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	1-6, 10
	L	L	H	L	Precharge	Truncate Read burst, start Precharge	1-6, 8
	L	H	H	L	BURST TERMINATE	BURST TERMINATE	1-6, 9
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	1-6, 10, 11
	L	H	L	L	Write	Select column and start Write burst	1-6, 10
	L	L	H	L	Precharge	Truncate Write burst, start Precharge	1-6, 8, 11

1. This table applies when CKE n-1 was HIGH and CKE n is HIGH (see Truth Table 2: Clock Enable (CKE) and after t_{XSNR} / t_{XSRD} has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and t_{RP} has been met.
   - Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank.
   - Precharging: Starts with registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the idle state.
   - Row Activating: Starts with registration of an Active command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the “row active” state.
   - Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Deselect or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according Truth Table 4.
5. The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states.
   - Refreshing: Starts with registration of an Auto Refresh command and ends when t_{RFC} is met. Once t_{RFC} is met, the DDR SDRAM is in the “all banks idle” state.
   - Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR SDRAM is in the “all banks idle” state.
   - Precharging All: Starts with registration of a Precharge All command and ends when t_{RP} is met. Once t_{RP} is met, all banks is in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent Read burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
11. Requires appropriate DM masking.

Truth Table 4: Current State Bank n - Command to Bank m (Different bank)

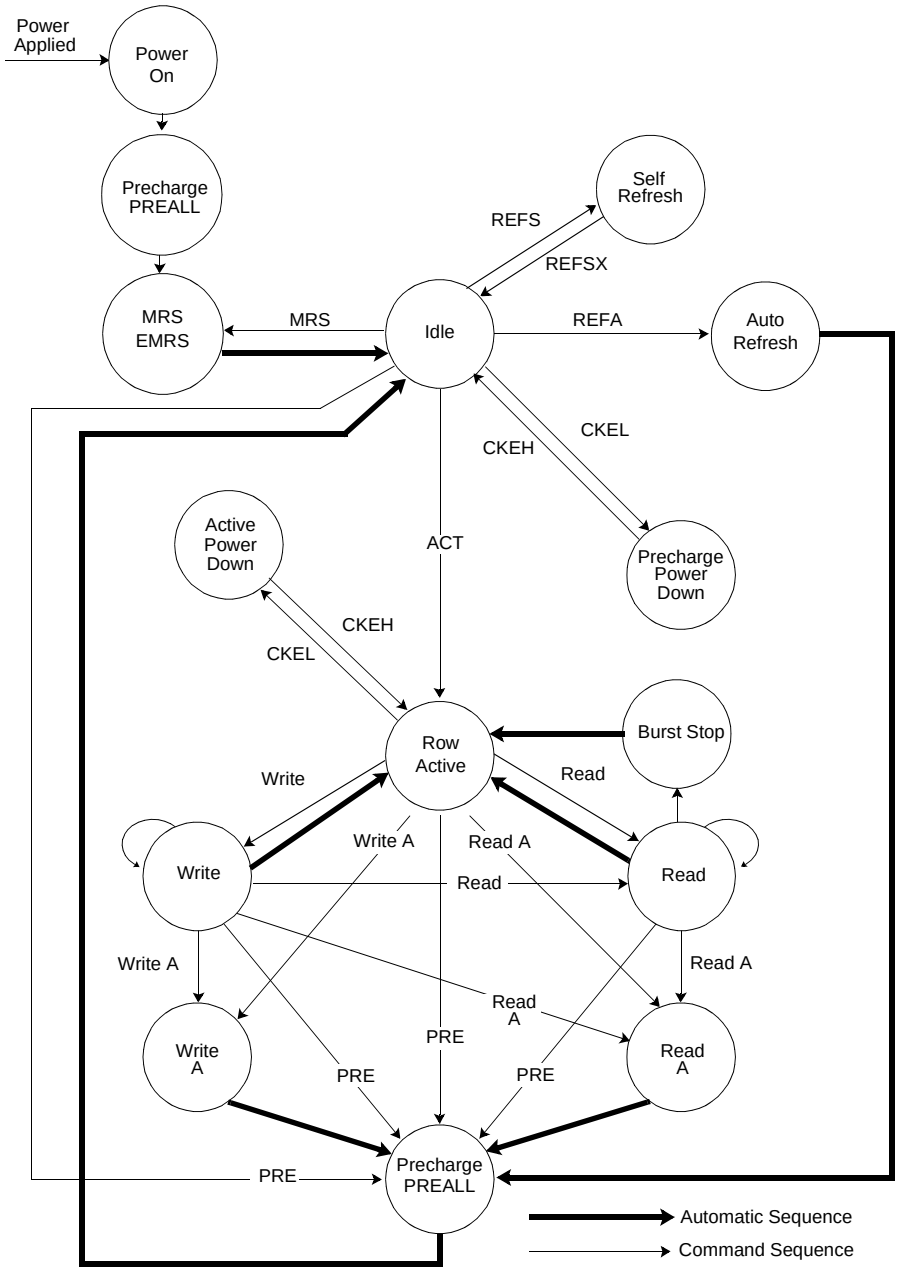
Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP/continue previous operation	1-6
	L	H	H	H	No Operation	NOP/continue previous operation	1-6
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m		1-6
Row Activating, Active, or Precharging	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start Read burst	1-7
	L	H	L	L	Write	Select column and start Write burst	1-7
	L	L	H	L	Precharge		1-6
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start new Read burst	1-7
	L	L	H	L	Precharge		1-6
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start Read burst	1-8
	L	H	L	L	Write	Select column and start new Write burst	1-7
	L	L	H	L	Precharge		1-6
Read (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start new Read burst	1-7,10
	L	H	L	L	Write	Select column and start Write burst	1-7,9,10
	L	L	H	L	Precharge		1-6
Write (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start Read burst	1-7,10
	L	H	L	L	Write	Select column and start new Write burst	1-7,10
	L	L	H	L	Precharge		1-6

1. This table applies when CKE n-1 was HIGH and CKE n is HIGH (see Truth Table 2: Clock Enable (CKE) and after t_{XSNR} / t_{XSRD} has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Read with Auto Precharge Enabled: See note 10.
   Write with Auto Precharge Enabled: See note 10.
4. AUTO REFRESH and Mode Register Set commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8. Requires appropriate DM masking.
9. A Write command may be applied after the completion of data output.
10. **Concurrent Auto Precharge:**
    This device supports “Concurrent Auto Precharge”. When a read with auto precharge or a write with auto precharge is enabled any command may follow to the other banks as long as that command does not interrupt the read or write data transfer and all other limitations apply (e.g. contention between READ data and WRITE data must be avoided). The mimimum delay from a read or write command with auto precharge enable, to a command to a different banks is summarized in table 5.

Truth Table 5: Concurrent Auto Precharge

From Command	To Command (different bank)	Minimum Delay with Concurrent Auto Precharge Support	Units
WRITE w/AP	Read or Read w/AP	1 + (BL/2) + tWTR	tCK
	Write ot Write w/AP	BL/2	tCK
	Precharge or Activate	1	tCK
Read w/AP	Read or Read w/AP	BL/2	tCK
	Write or Write w/AP	CL (rounded up)+ BL/2	tCK
	Precharge or Activate	1	tCK

Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

Operating Conditions

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	−0.5 to V_{DDQ}+ 0.5	V
V_{IN}	Voltage on Inputs relative to V_{SS}	−0.5 to +3.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	−0.5 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	−0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	−55 to +150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Input and Output Capacitances

Parameter	Package	Symbol	Min.	Max.	Units	Notes
Input Capacitance: CK, $\overline{CK}$	TSOP	C_{I1}	2.0	3.0	pF	1
	BGA		1.5	2.5		
Delta Input Capacitance CK, $\overline{CK}$	TSOP	C_{dI1}	-	0.25	pF	1
	BGA		-	0.25		
Input Capacitance: All other input-only pins	TSOP	C_{I2}	2.0	3.0	pF	1
	BGA		1.5	2.5		
Delta Input Capacitance: All other input-only pins	TSOP	C_{dI2}	-	0.5	pF	1
	BGA		-	0.5		
Input/Output Capacitance: DQ, DQS, DM	TSOP	C_{IO}	4.0	5.0	pF	1, 2
	BGA		3.5	4.5		
Delta Input/Output Capacitance : DQ, DQS, DM	TSOP	C_{dIO}	-	0.5	pF	1
	BGA		-	0.5		

1. These values are guaranteed by design and are tested on a sample base only. V_{DDQ} = V_{DD} = 2.5V ± 0.2V, f = 100MHz, T_A = 25°C, V_{OUT} (DC) = $V_{DDQ/2}$, VOUT (Peak to Peak) 0.2V. Unused pins are tied to ground .
2. DM inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level

Electrical Characteristics and DC Operating Conditions

(0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.5V ± 0.2V, V_{DD} = + 2.5V ± 0.2V)

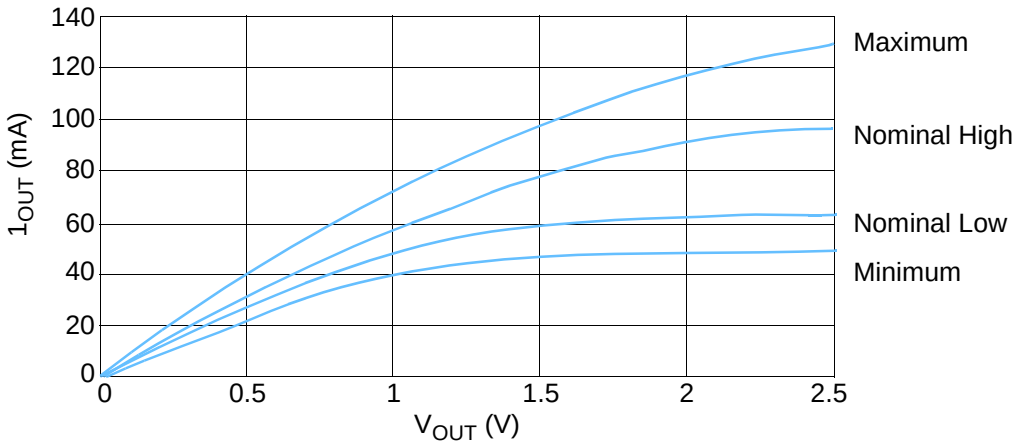
Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage	2.3	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{TT}	I/O Termination Voltage (System)	V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
$V_{IH(DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
$V_{IL(DC)}$	Input Low (Logic0) Voltage	– 0.3	V_{REF} – 0.15	V	1
$V_{IN(DC)}$	Input Voltage Level, CK and $\overline{CK}$ Inputs	– 0.3	V_{DDQ} + 0.3	V	1
$V_{ID(DC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.36	V_{DDQ} + 0.6	V	1, 4
VI_{Ratio}	VI-Matching Pullup Current to Pulldown Current	0.71	1.4		5
I_I	Input Leakage Current. Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	– 2	2	µA	1
I_{OZ}	Output Leakage Current (DQs are disabled; 0V ≤ V_{out} ≤ V_{DDQ}	– 5	5	µA	1
I_{OH}	Output High Current, Normal Strength Driver (V_{OUT} = 1.95 V, V_{TT} = 1.13 V)	– 16.2		mA	1
I_{OL}	Output Low Current, Normal Strength Driver (V_{OUT} = 0.35 V, V_{TT} = 1.17 V)	16.2		mA	1

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$
5. The ration of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

Normal Strength Pulldown and Pullup Characteristics

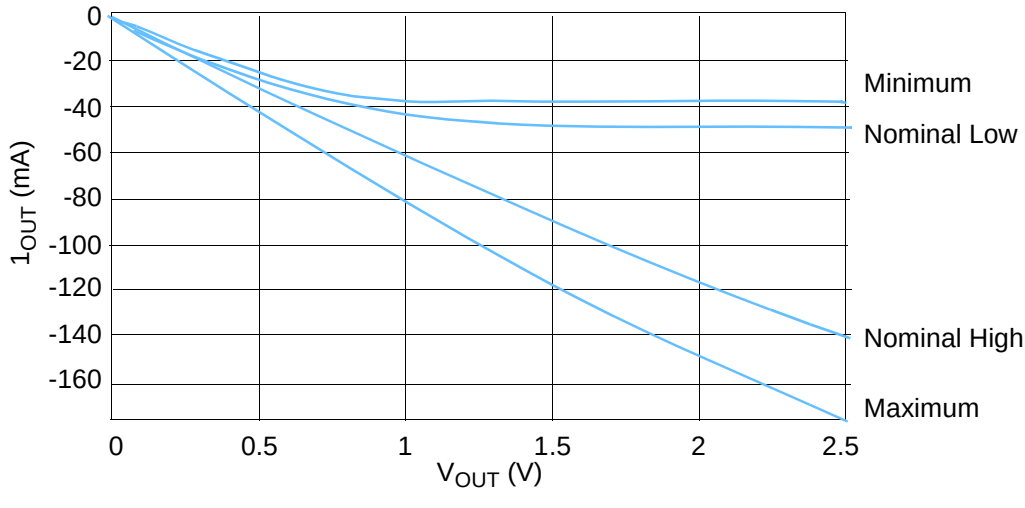
1. The nominal pulldown V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
2. The full variation in driver pulldown current from minimum to maximum process, temperature, and voltage lie within the outer bounding lines of the V-I curve.

Normal Strength Pulldown Characteristics



3. The nominal pullup V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
4. The full variation in driver pullup current from minimum to maximum process, temperature, and voltage lie within the outer bounding lines of the V-I curve.

Normal Strength Pullup Characteristics



5. The full variation in the ratio of the maximum to minimum pullup and pulldown current does not exceed 1.7, for device drain to source voltages from 0.1 to 1.0.
6. The full variation in the ratio of the nominal pullup to pulldown current should be unity ± 10%, for device drain to source voltages from 0.1 to 1.0V.

Normal Strength Pulldown and Pullup Currents

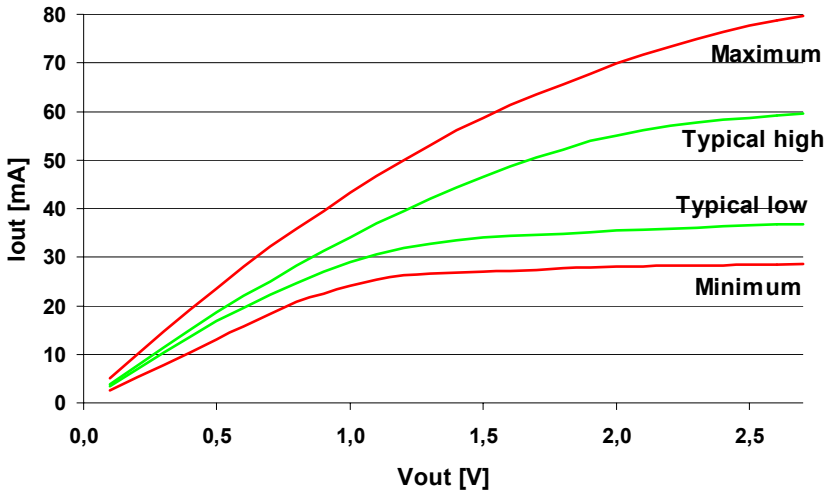
	Pulldown Current (mA)				Pullup Current (mA)			
Voltage (V)	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	6.0	6.8	4.6	9.6	–6.1	–7.6	–4.6	–10.0
0.2	12.2	13.5	9.2	18.2	–12.2	–14.5	–9.2	–20.0
0.3	18.1	20.1	13.8	26.0	–18.1	–21.2	–13.8	–29.8
0.4	24.1	26.6	18.4	33.9	–24.0	–27.7	–18.4	–38.8
0.5	29.8	33.0	23.0	41.8	–29.8	–34.1	–23.0	–46.8
0.6	34.6	39.1	27.7	49.4	–34.3	–40.5	–27.7	–54.4
0.7	39.4	44.2	32.2	56.8	–38.1	–46.9	–33.2	–61.8
0.8	43.7	49.8	36.8	63.2	–41.1	–53.1	–36.0	–69.5
0.9	47.5	55.2	39.6	69.9	–43.8	–59.4	–38.2	–77.3
1.0	51.3	60.3	42.6	76.3	–46.0	–65.5	–38.7	–85.2
1.1	54.1	65.2	44.8	82.5	–47.8	–71.6	–39.0	–93.0
1.2	56.2	69.9	46.2	88.3	–49.2	–77.6	–39.2	–100.6
1.3	57.9	74.2	47.1	93.8	–50.0	–83.6	–39.4	–108.1
1.4	59.3	78.4	47.4	99.1	–50.5	–89.7	–39.6	–115.5
1.5	60.1	82.3	47.7	103.8	–50.7	–95.5	–39.9	–123.0
1.6	60.5	85.9	48.0	108.4	–51.0	–101.3	–40.1	–130.4
1.7	61.0	89.1	48.4	112.1	–51.1	–107.1	–40.2	–136.7
1.8	61.5	92.2	48.9	115.9	–51.3	–112.4	–40.3	–144.2
1.9	62.0	95.3	49.1	119.6	–51.5	–118.7	–40.4	–150.5
2.0	62.5	97.2	49.4	123.3	–51.6	–124.0	–40.5	–156.9
2.1	62.9	99.1	49.6	126.5	–51.8	–129.3	–40.6	–163.2
2.2	63.3	100.9	49.8	129.5	–52.0	–134.6	–40.7	–169.6
2.3	63.8	101.9	49.9	132.4	–52.2	–139.9	–40.8	–176.0
2.4	64.1	102.8	50.0	135.0	–52.3	–145.2	–40.9	–181.3
2.5	64.6	103.8	50.2	137.3	–52.5	–150.5	–41.0	–187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Evaluation Conditions for I/O Driver Characteristics

	Nominal	Minimum	Maximum
Operating Temperature	25 °C	70 °C	0 °C
V_{DD} / V_{DDQ}	2.5V	2.3V	2.7V
Process Corner	typical	slow-slow	fast-fast

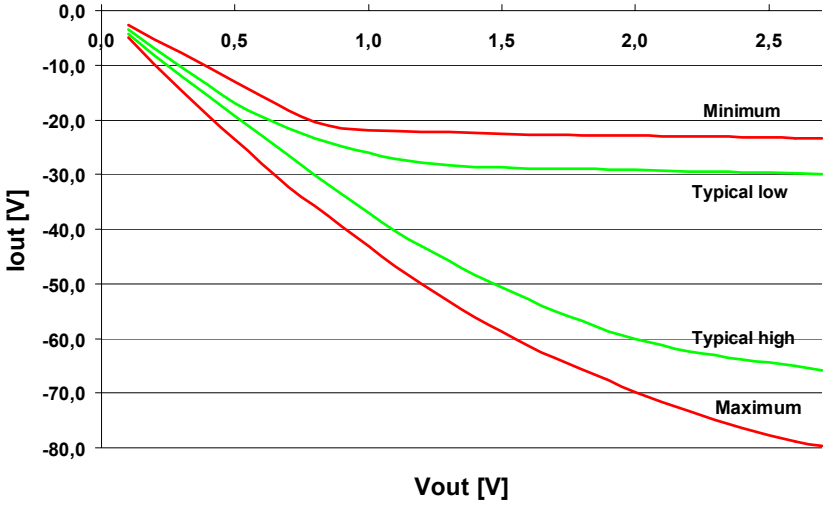
Weak Strength Pulldown and Pullup Characteristics

Weak Strength Pulldown Characteristics



1. The weak pulldown V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve
2. The weak pullup V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
3. The full variation in driver pullup current from minimum to maximum process, temperature, and voltage lie within the outer bounding lines of the V-I curve.

Weak Strength Pullup Characteristics



4. The full variation in the ratio of the maximum to minimum pullup and pulldown current does not exceed 1.7, for device drain to source voltages from 0.1 to 1.0.
5. The full variation in the ratio of the nominal pullup to pulldown current should be unity ± 10%, for device drain to source voltages from 0.1 to 1.0V.

Weak Strength Driver Pulldown and Pullup Currents

	Pulldown Current (mA)				Pullup Current (mA)			
Voltage (V)	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	3.4	3.8	2.6	5.0	-3.5	-4.3	-2.6	-5.0
0.2	6.9	7.6	5.2	9.9	-6.9	-8.2	-5.2	-9.9
0.3	10.3	11.4	7.8	14.6	-10.3	-12.0	-7.8	-14.6
0.4	13.6	15.1	10.4	19.2	-13.6	-15.7	-10.4	-19.2
0.5	16.9	18.7	13.0	23.6	-16.9	-19.3	-13.0	-23.6
0.6	19.6	22.1	15.7	28.0	-19.4	-22.9	-15.7	-28.0
0.7	22.3	25.0	18.2	32.2	-21.5	-26.5	-18.2	-32.2
0.8	24.7	28.2	20.8	35.8	-23.3	-30.1	-20.4	-35.8
0.9	26.9	31.3	22.4	39.5	-24.8	-33.6	-21.6	-39.5
1.0	29.0	34.1	24.1	43.2	-26.0	-37.1	-21.9	-43.2
1.1	30.6	36.9	25.4	46.7	-27.1	-40.3	-22.1	-46.7
1.2	31.8	39.5	26.2	50.0	-27.8	-43.1	-22.2	-50.0
1.3	32.8	42.0	26.6	53.1	-28.3	-45.8	-22.3	-53.1
1.4	33.5	44.4	26.8	56.1	-28.6	-48.4	-22.4	-56.1
1.5	34.0	46.6	27.0	58.7	-28.7	-50.7	-22.6	-58.7
1.6	34.3	48.6	27.2	61.4	-28.9	-52.9	-22.7	-61.4
1.7	34.5	50.5	27.4	63.5	-28.9	-55.0	-22.7	-63.5
1.8	34.8	52.2	27.7	65.6	-29.0	-56.8	-22.8	-65.6
1.9	35.1	53.9	27.8	67.7	-29.2	-58.7	-22.9	-67.7
2.0	35.4	55.0	28.0	69.8	-29.2	-60.0	-22.9	-69.8
2.1	35.6	56.1	28.1	71.6	-29.3	-61.2	-23.0	-71.6
2.2	35.8	57.1	28.2	73.3	-29.5	-62.4	-23.0	-73.3
2.3	36.1	57.7	28.3	74.9	-29.5	-63.1	-23.1	-74.9
2.4	36.3	58.2	28.3	76.4	-29.6	-63.8	-23.2	-76.4
2.5	36.5	58.7	28.4	77.7	-29.7	-64.4	-23.2	-77.7
2.6	36.7	59.2	28.5	78.8	-29.8	-65.1	-23.3	-78.8
2.7	36.8	59.6	28.6	79.7	-29.9	-65.8	-23.3	-79.7

Evaluation Conditions for I/O Driver Characteristics

	Nominal	Minimum	Maximum
Operating Temperature	25 °C	70 °C	0 °C
V_{DD} / V_{DDQ}	2.5V	2.3V	2.7V
Process Corner	typical	slow-slow	fast-fast

IDD Specification and Conditions

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter/Condition		DDR200 -8		DDR266A -7		DDR266 -7F		DDR333 -6		Unit	Notes
			typ.	max.	typ.	max.	typ.	max.	typ.	max.		4
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	x4/x8	70	90	75	100	83	110	85	110	mA	1, 2
		x16	72	95	77	105	86	115	88	115	mA	
IDD1	**Operating Current**: one bank; active/read/precharge; burst length 4; Refer to the following page for detailed test conditions.	x4/x8	80	100	90	110	98	120	100	120	mA	1, 2
		x16	83	105	94	115	102	125	104	125	mA	
IDD2P	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE <= VIL MAX		5	7	6	8	6	8	6	9	mA	1, 2
IDD2F	**Precharge Floating Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.		30	35	35	40	35	40	45	55	mA	1, 2
IDD2Q	**Precharge Quiet Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.		18	22	20	25	20	25	25	28	mA	1, 2
IDD3P	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE <= VIL MAX; VIN = VREF for DQ, DQS and DM.		13	16	15	18	15	18	18	21	mA	1, 2
IDD3N	**Active Standby Current**: one bank active; CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	x4/x8	40	45	50	55	50	55	60	65	mA	1, 2
		x16	42	50	52	60	52	60	63	70	mA	
IDD4R	**Operating Current**: one bank active; BL2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL2 for DDR200 and DDR266(A), CL3 for DDR333 and DDR400; IOUT = 0mA	x4/x8	79	95	95	115	95	115	110	140	mA	1, 2
		x16	89	110	107	130	107	130	124	160	mA	
IDD4W	**Operating Current**: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL2 for DDR200 and DDR266(A), CL3 for DDR333 and DDR400	x4/x8	85	105	105	125	105	125	125	145	mA	1, 2
		x16	96	120	119	140	119	140	141	165	mA	
IDD5	**Auto-Refresh Current**: tRC = tRFC MIN, distributed refresh		126	170	135	180	135	180	144	190	mA	1, 2
IDD6	**Self-Refresh Current**: CKE <= 0.2V; external clock on	standard version	1.5	2.5	1.5	2.5	1.5	2.5	1.5	2.5	mA	1, 2, 3
		low power version	1.20	1.25	1.20	1.25	1.20	1.25	1.20	1.25	mA	
IDD7	**Operating Current**: four bank; four bank interleaving with burst length 4; Refer to the following page for detailed test conditions.	x4/x8	150	210	171	225	171	225	208	270	mA	1, 2
		x16	158	220	180	235	180	235	218	285		

1. IDD specifications are tested after the device is properly initialized and measured at 100 MHz for DDR200, 133 MHz for DDR266(A) and 166 MHz for DDR333
2. Input slew rate = 1V/ns.
3. Enables on-chip refresh and address counters
4. Test condition for typical values : VDD = 2.5V ,Ta = 25°C, test condition for maximum values: test limit at VDD = 2.7V ,Ta = 10°C

Detailed test conditions for DDR SDRAM IDD1 and IDD7

IDD1 : Operating current : One bank operation

1. Only one bank is accessed with $t_{RC(min)}$, Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{out} = 0 mA
2. Timing patterns
   - ***DDR200*** (100Mhz, CL=2) : tCK = 10 ns, CL=2, BL=4, tRCD = 2 * tCK, tRAS = 5 * tCK
     Setup: A0 N R0 N N P0 N
     Read : A0 N R0 N N P0 N - repeat the same timing with random address changing
     50% of data changing at every burst
   - ***DDR266A*** (133Mhz, CL=2) : tCK = 7.5 ns, CL=2, BL=4, tRCD = 3 * tCK, tRC = 9 * tCK, tRAS = 5 * tCK
     Setup: A0 N N R0 N P0 N N N
     Read : A0 N N R0 N P0 N NN - repeat the same timing with random address changing
     50% of data changing at every burst
   - ***DDR333*** (166Mhz, CL=2.5) : tCK = 6 ns, CL=2.5, BL=4, tRCD = 3 * tCK, tRC = 9 * tCK, tRAS = 5 * tCK
     Setup: A0 N N R0 N P0 N N N
     Read : A0 N N R0 N P0 N N N - repeat the same timing with random address changing
     50% of data changing at every burst

3.Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

IDD7 : Operating current: Four bank operation

1. Four banks are being interleaved with $t_{RC(min)}$, Burst Mode, Address and Control inputs on NOP edge are not changing. I_{out} = 0 mA
2. Timing patterns
   - ***DDR200*** (100Mhz, CL=2) : tCK = 10 ns, CL=2, BL=4, tRRD = 2 * tCK, tRCD= 3 * tCK, Read with autoprecharge
     Setup: A0 N A1 R0 A2 R1 A3 R2
     Read : A0 R3 A1 R0 A2 R1 A3 R2- repeat the same timing with random address changing
     50% of data changing at every burst
   - ***DDR266A*** (133Mhz, CL=2) : tCK = 7.5 ns, CL=2, BL=4, tRRD = 2 * tCK, tRCD = 3 * tCK
     Setup: A0 N A1 R0 A2 R1 A3 R2 N R3
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 - repeat the same timing with random address changing
     50% of data changing at every burst
   - ***DDR333*** (166Mhz, CL=2.5) : tCK = 6 ns, CL=2.5, BL=4, tRRD = 2 * tCK, tRCD = 3 * tCK
     Setup: A0 N A1 R0 A2 R1 A3 R2 N R3
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 - repeat the same timing with random address changing
     50% of data changing at every burst

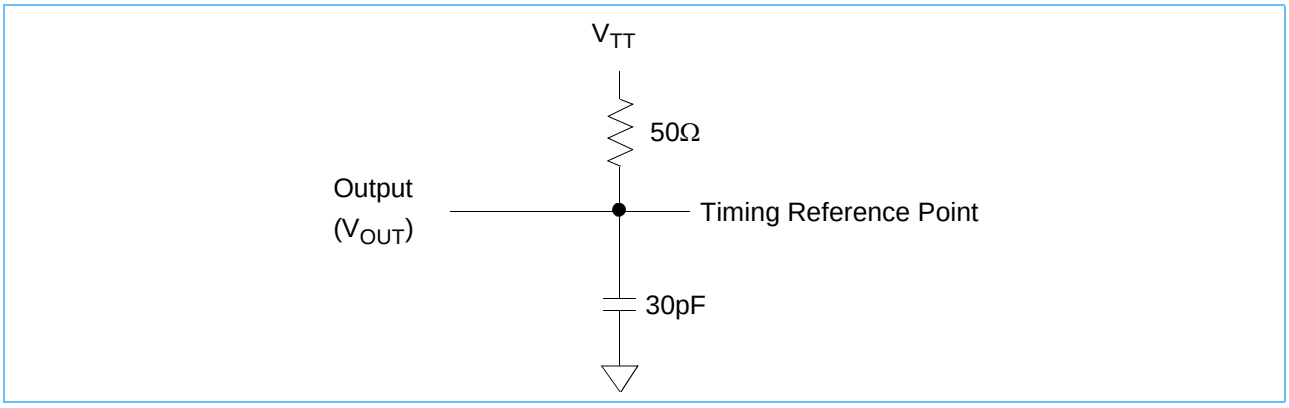
3.Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC Characteristics

(Notes 1-6 apply to the following Tables: Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. The figure below represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level)
6. For System Characteristics like Setup & Holdtime Derating for Slew Rate, I/O Delta Rise/Fall Derating,DDR SDRAM Slew Rate Standards, Overshoot & Undershoot specification and Clamp V-I characteristics see the latest JEDEC specification for DDR components

AC Output Load Circuit Diagram / Timing Reference Load



AC Operating Conditions)

(0 °C ≤ TA ≤ 70 °C; VDDQ = 2.5V ± 0.2V; VDD = 2.5V ± 0.2V)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH(AC)}$	Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	V_{REF} + 0.31		V	1, 2
$V_{IL(AC)}$	Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals		V_{REF} – 0.31	V	1, 2
$V_{ID(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.7	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX(AC)}$	Input Closing Point Voltage, CK and $\overline{CK}$ Inputs	0.5*V_{DDQ} – 0.2	0.5*V_{DDQ} + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Electrical Characteristics & AC Timing - Absolute Specifications

($0\ °C \le T_A \le 70\ °C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$) (Part 1 of 2)

Symbol	Parameter		DDR200 -8		DDR266A -7		DDR266 -7F		DDR333 -6		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$		− 0.8	+ 0.8	− 0.75	+ 0.75	− 0.75	+ 0.75	− 0.7	+ 0.7	ns	1-4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		− 0.8	+ 0.8	− 0.75	+ 0.75	− 0.75	+ 0.75	− 0.6	+ 0.6	ns	1-4
t_{CH}	CK high-level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CL}	CK low-level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{HP}	Clock Half Period		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		ns	1-4
t_{CK}	Clock cycle time	CL = 3.0	8	12	7	12	7	12	6	12	ns	1-4
t_{CK}		CL = 2.5	8	12	7	12	7	12	6	12	ns	1-4
t_{CK}		CL = 2.0	10	12	7.5	12	7.5	12	7.5	12	ns	1-4
t_{DH}	DQ and DM input hold time		0.6		0.5		0.5		0.45		ns	1-4
t_{DS}	DQ and DM input setup time		0.6		0.5		0.5		0.45		ns	1-4
t_{IPW}	Control & Addr. input pulse width (each input)		2.5		2.2		2.2		2.2		ns	1-4,10
t_{DIPW}	DQ and DM input pulse width (each input)		2.0		1.75		1.75		1.75		ns	1-4, 10
t_{HZ}	Data-out high-impedence time from CK/$\overline{CK}$		− 0.8	+ 0.8	− 0.75	+ 0.75	− 0.75	+ 0.75	− 0.7	+ 0.7	ns	1-4, 5
t_{LZ}	Data-out low-impedence time from CK/$\overline{CK}$		− 0.8	+ 0.8	− 0.75	+ 0.75	− 0.75	+ 0.75	− 0.7	+ 0.7	ns	1-4, 5
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	1-4
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	TSOP66		+ 0.6		+ 0.5		+ 0.5		+ 0.45	ns	1-4
		BGA		+ 0.6		+ 0.5		+ 0.5		+ 0.40	ns	1-4
t_{QHS}	Data hold skew factor	TSOP66		1.0		0.75		0.75		0.55	ns	1-4
		BGA		1.0		0.75		0.75		0.5	ns	1-4
t_{QH}	DQ output hold time from DQS		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns	1-4
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35		0.35		0.35		0.35		t_{CK}	1-4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		0.2		0.2		t_{CK}	1-4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		0.2		0.2		t_{CK}	1-4
t_{MRD}	Mode register set command cycle time		2		2		2		2		t_{CK}	1-4
t_{WPRES}	Write preamble setup time		0		0		0		0		ns	1-4, 7
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	1-4, 6
t_{WPRE}	Write preamble		0.25		0.25		0.25		0.25		t_{CK}	1-4
t_{IS}	Address and control input setup time	fast slew rate	1.1		0.9		0.9		0.75		ns	2-4, 10,11
		slow slew rate	1.1		1.0		1.0		0.8		ns	
t_{IH}	Address and control input hold time	fast slew rate	1.1		0.9		0.9		0.75		ns	
		slow slew rate	1.1		1.0		1.0		0.8		ns	

Electrical Characteristics & AC Timing - Absolute Specifications

($0\ °C \le T_A \le 70\ °C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$) (Part 2 of 2)

Symbol	Parameter	DDR200 -8		DDR266A -7		DDR266 -7F		DDR333 -6		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RPRE}	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	1-4
t_{RPST}	Read postamble	0.40	0.60	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	1-4
t_{RAS}	Active to Precharge command	50	120,000	45	120,000	45	120,000	42	70,000	ns	1-4
t_{RC}	Active to Active/Auto-refresh command period	70		65		60		60		ns	1-4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period	80		75		75		72		ns	1-4
t_{RCD}	Active to Read or Write delay	20		20		15		18		ns	1-4
t_{RP}	Precharge command period	20		20		15		18		ns	1-4
t_{RAP}	Active to Autoprecharge delay	20		20		20		18		ns	1-4
t_{RRD}	Active bank A to Active bank B command	15		15		15		12		ns	1-4
t_{WR}	Write recovery time	15		15		15		15		ns	1-4
t_{DAL}	Auto precharge write recovery + precharge time	(twr/tck) + (trp/tck)								t_{CK}	1-4,9
t_{WTR}	Internal write to read command delay	1		1		1		1		t_{CK}	1-4
t_{XSNR}	Exit self-refresh to non-read command	80		75		75		75		ns	1-4
t_{XSRD}	Exit self-refresh to read command	200		200		200		200		t_{CK}	1-4
t_{REFI}	Average Periodic Refresh Interval (8192 refresh commands per 64ms refresh period)		7.8		7.8		7.8		7.8	µs	1-4, 8

1. Input slew rate >= 1V/ns for DDR266 & DDR333 and = 1V/ns for DDR 200
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are >= 1.0 V/ns
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For each of the terms, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
10. These parameters guarantee device timing, but they are not necessarilty tested on each device
11. Fast slew rate >= 1.0 V/ns , slow slew rate >= 0.5 V/ns and < 1V/ns for command/address and CK & $\overline{CK}$ slew rate >1.0 V/ns, measured between VOH(ac) and VOL(ac)

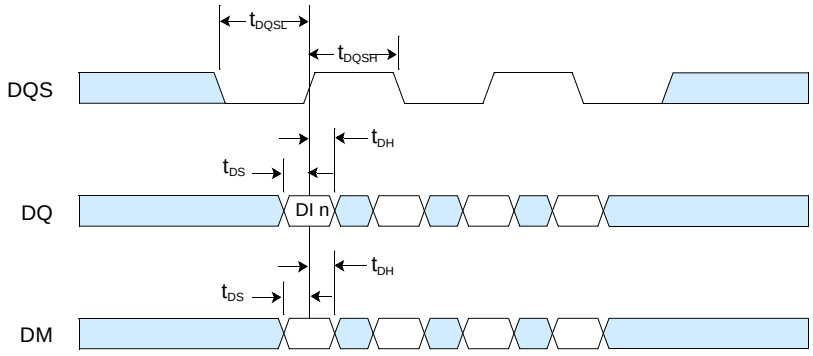
Electrical Characteristics & AC Timing for DDR266 - Applicable Specifications Expressed in Clock Cycles (tCK=133Mhz) ($0\ °C \le T_A \le 70\ °C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$,

Symbol	Parameter	sort	tCK = 133MHz		Units	Notes
			Min	Max		
t_{MRD}	Mode register set command cycle time		2		t_{CK}	1-54
t_{WPRE}	Write preamble		0.25		t_{CK}	1-5
t_{RAS}	Active to Precharge command		6	16000	t_{CK}	1-5
t_{RC}	Active to Active/Auto-refresh command period	DDR266A	9		t_{CK}	1-5
		DDR266	8		t_{CK}	1-5
t_{RFC}	Auto-refresh to Active/Auto-refresh command period		10		t_{CK}	1-5
t_{RCD}	Active to Read or Write delay	DDR266A	3		t_{CK}	1-5
		DDR266	2		t_{CK}	1-5
t_{RP}	Precharge command period	DDR266A	3		t_{CK}	1-5
		DDR266	2		t_{CK}	1-5
t_{RRD}	Active bank A to Active bank B command		2		t_{CK}	1-5
t_{WR}	Write recovery time		2		t_{CK}	1-5
t_{DAL}	Auto precharge write recovery + precharge time		5		t_{CK}	1-5
t_{WTR}	Internal write to read command delay		1		t_{CK}	1-5
t_{XSNR}	Exit self-refresh to non-read command		10		t_{CK}	1-5
t_{XSRD}	Exit self-refresh to read command		200		t_{CK}	1-5

1. Input slew rate = 1V/ns
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

Timing Diagrams

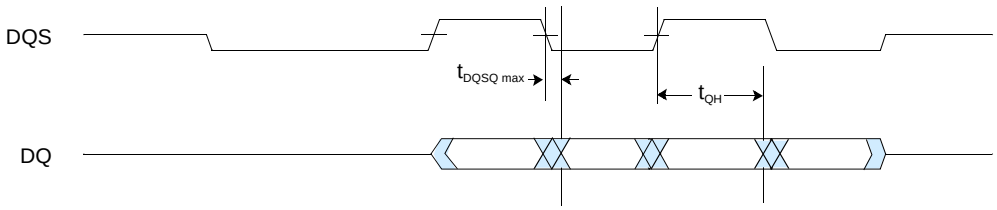
Data Input (Write) (Timing Burst Length = 4)



DI n = Data In for column n.
3 subsequent elements of data in are applied in programmed order following DI n.

Don't Care

Data Output (Read) (Timing Burst Length = 4)

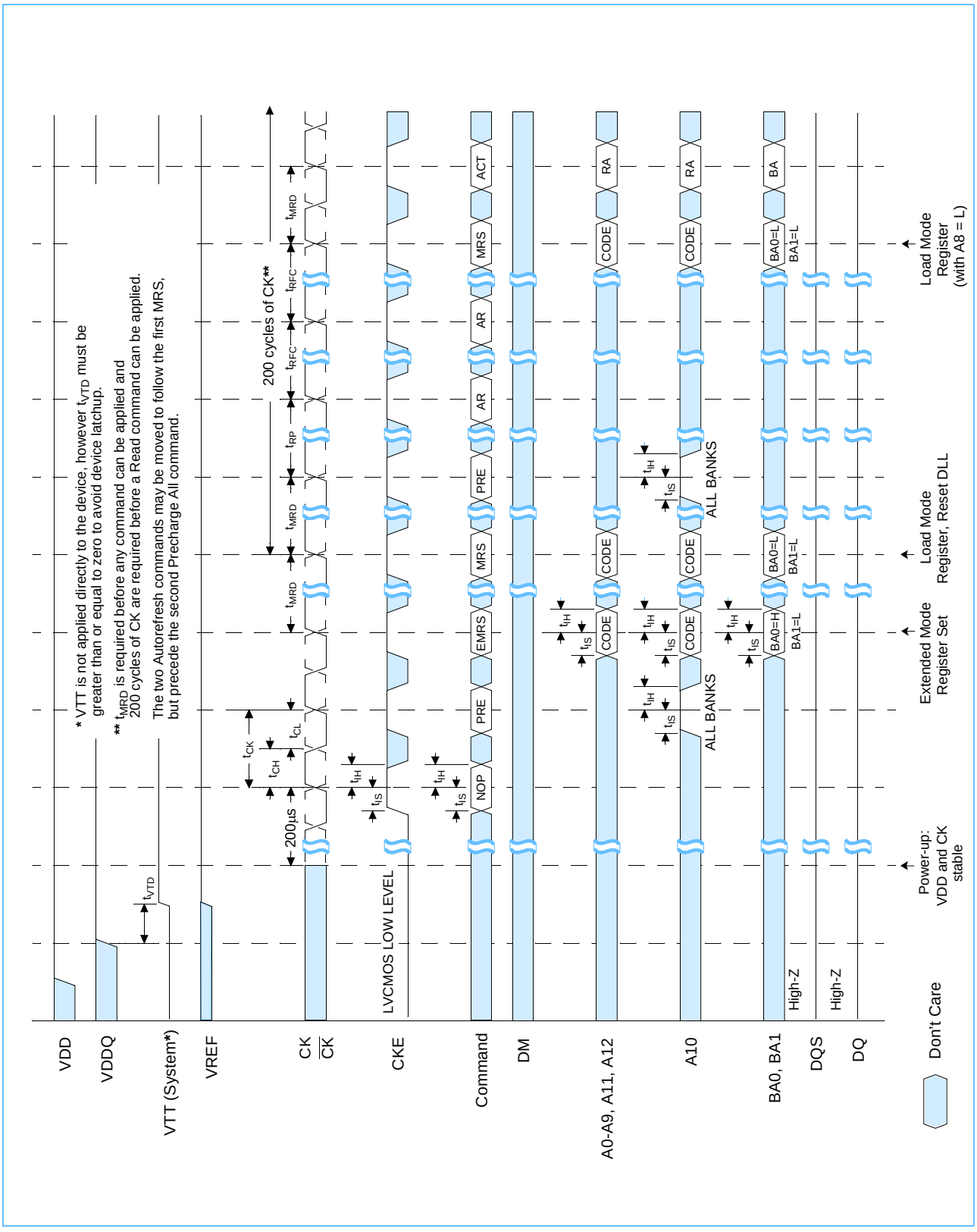


t_{QH} (Data output hold time from DQS)

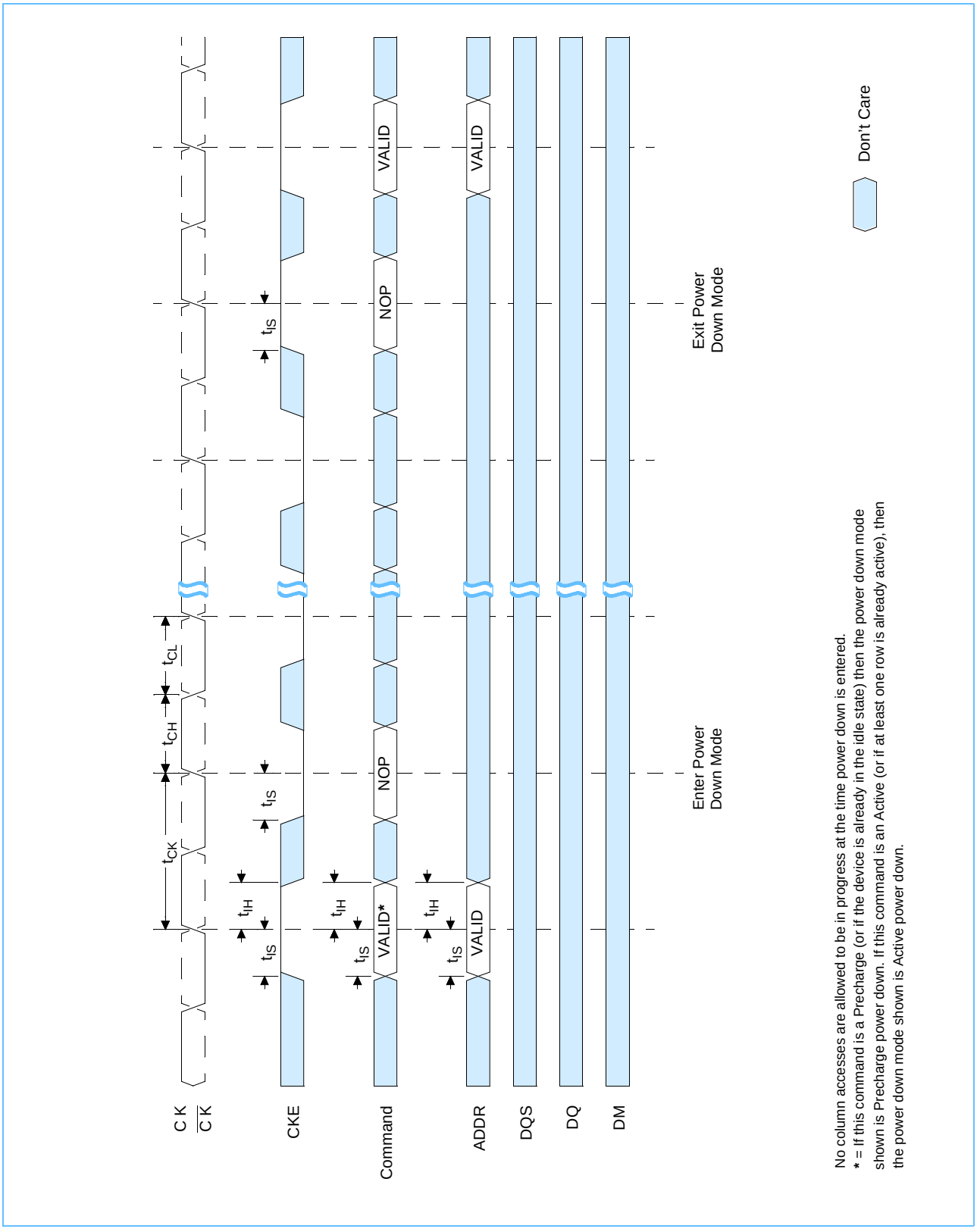
t_{DQSQ} and t_{QH} are only shown once and are shown referenced to different edges of DQS, only for clarify of illustration.
t_{DQSQ} and t_{QH} both apply to each of the four relevant edges of DQS.

$t_{DQSQ\ max.}$ is used to determine the worst case setup time for controller data capture.
t_{QH} is used to determine the worst case hold time for controller data capture.

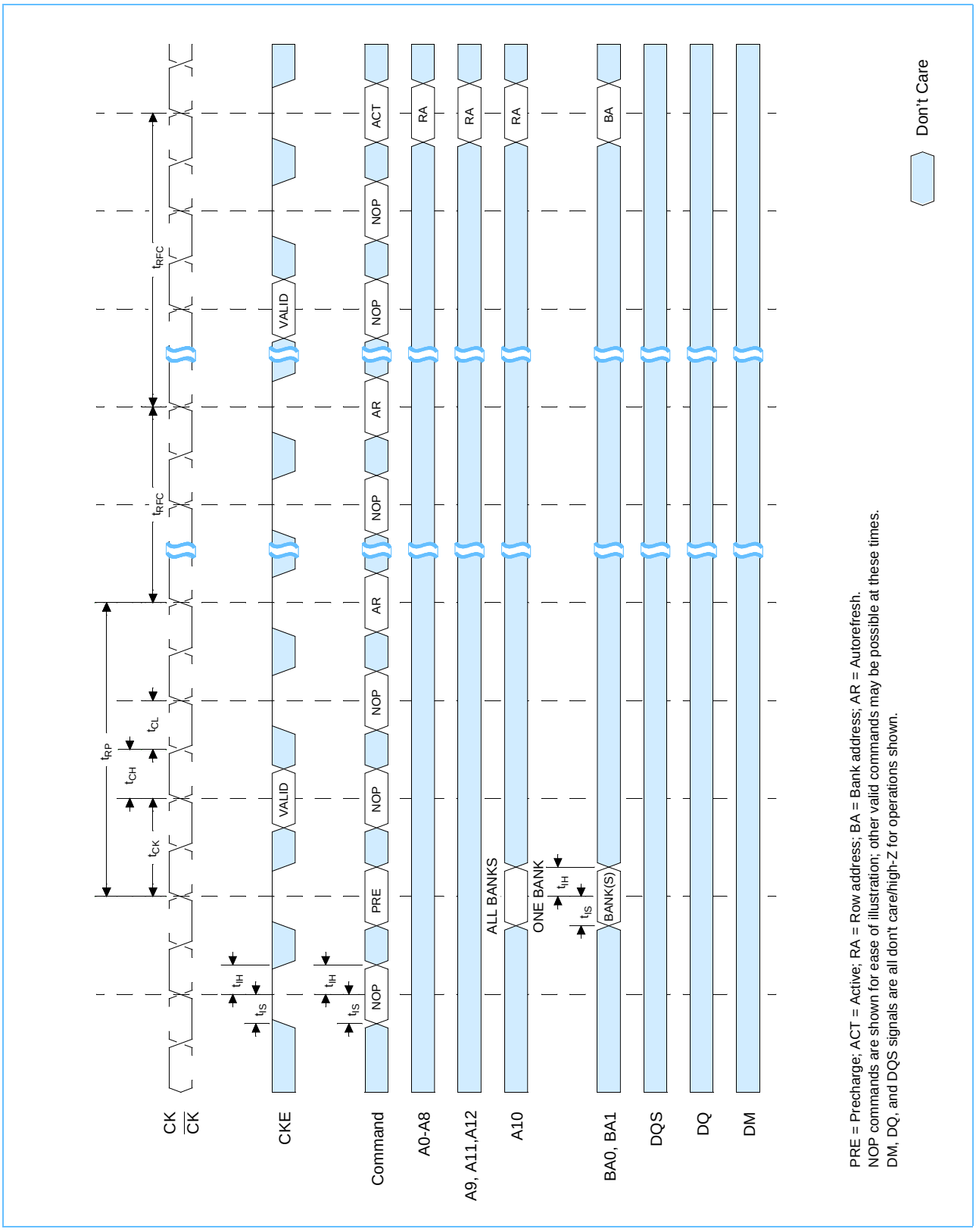
Initialize and Mode Register Sets



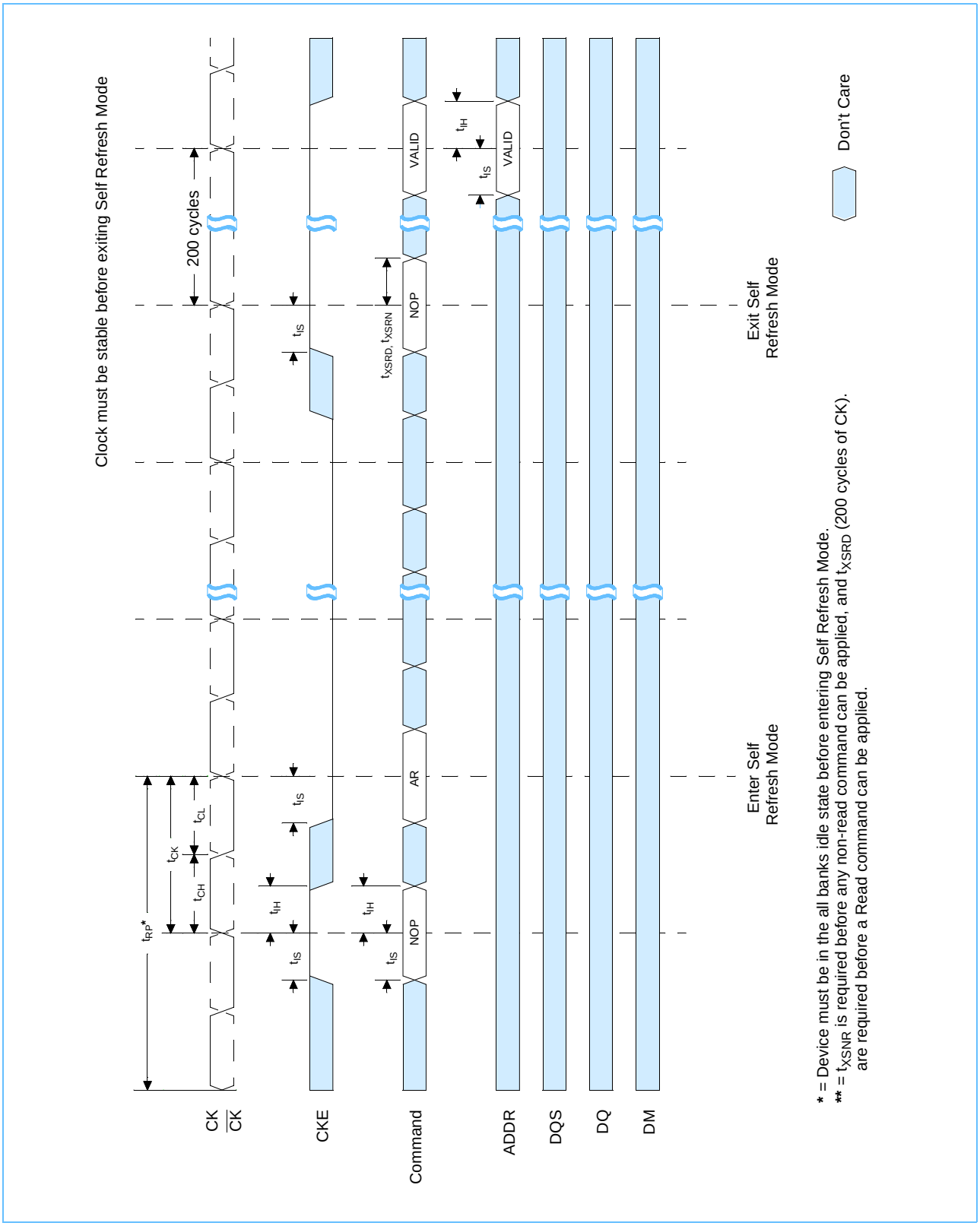
Power Down Mode



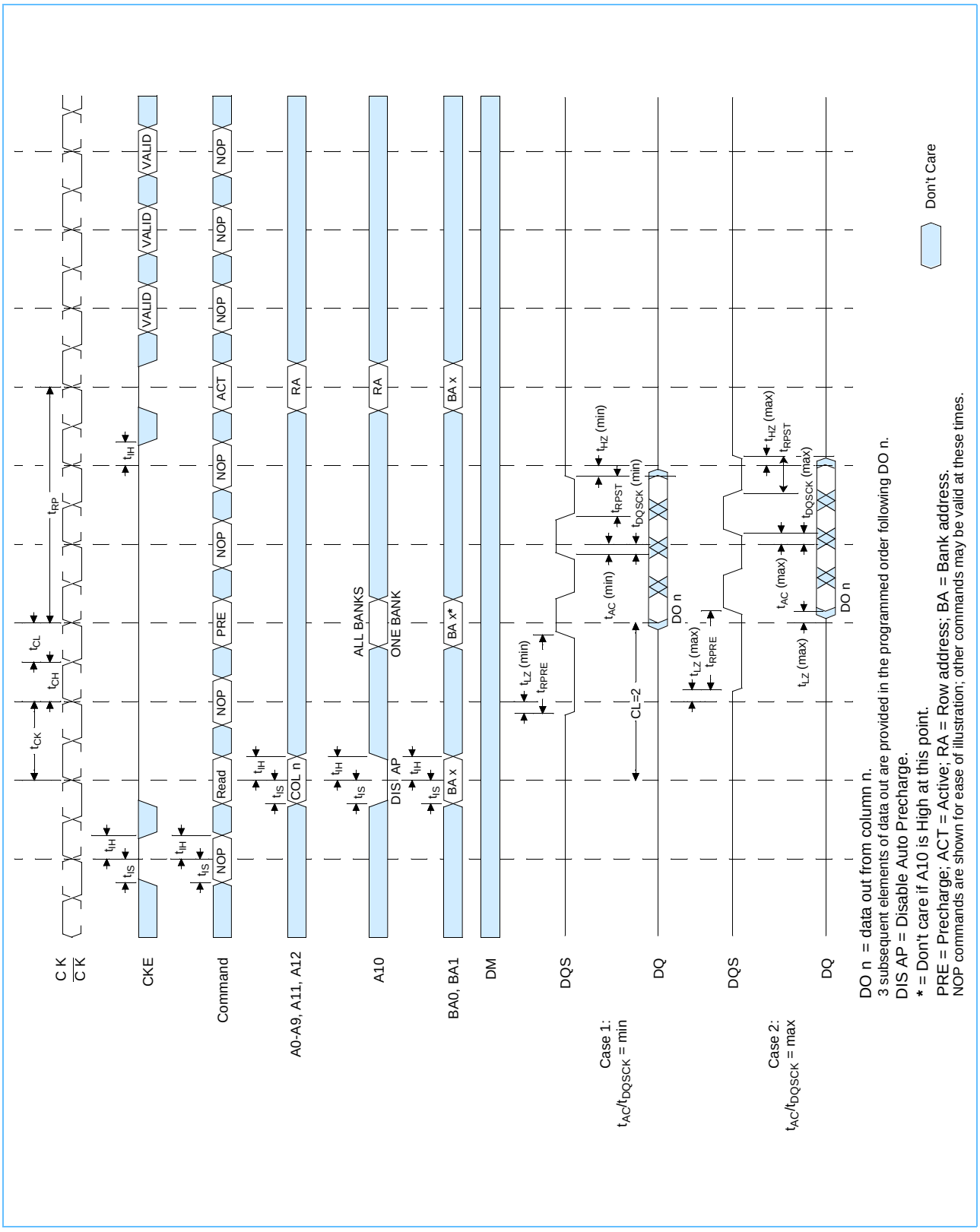
Auto Refresh Mode



Self Refresh Mode

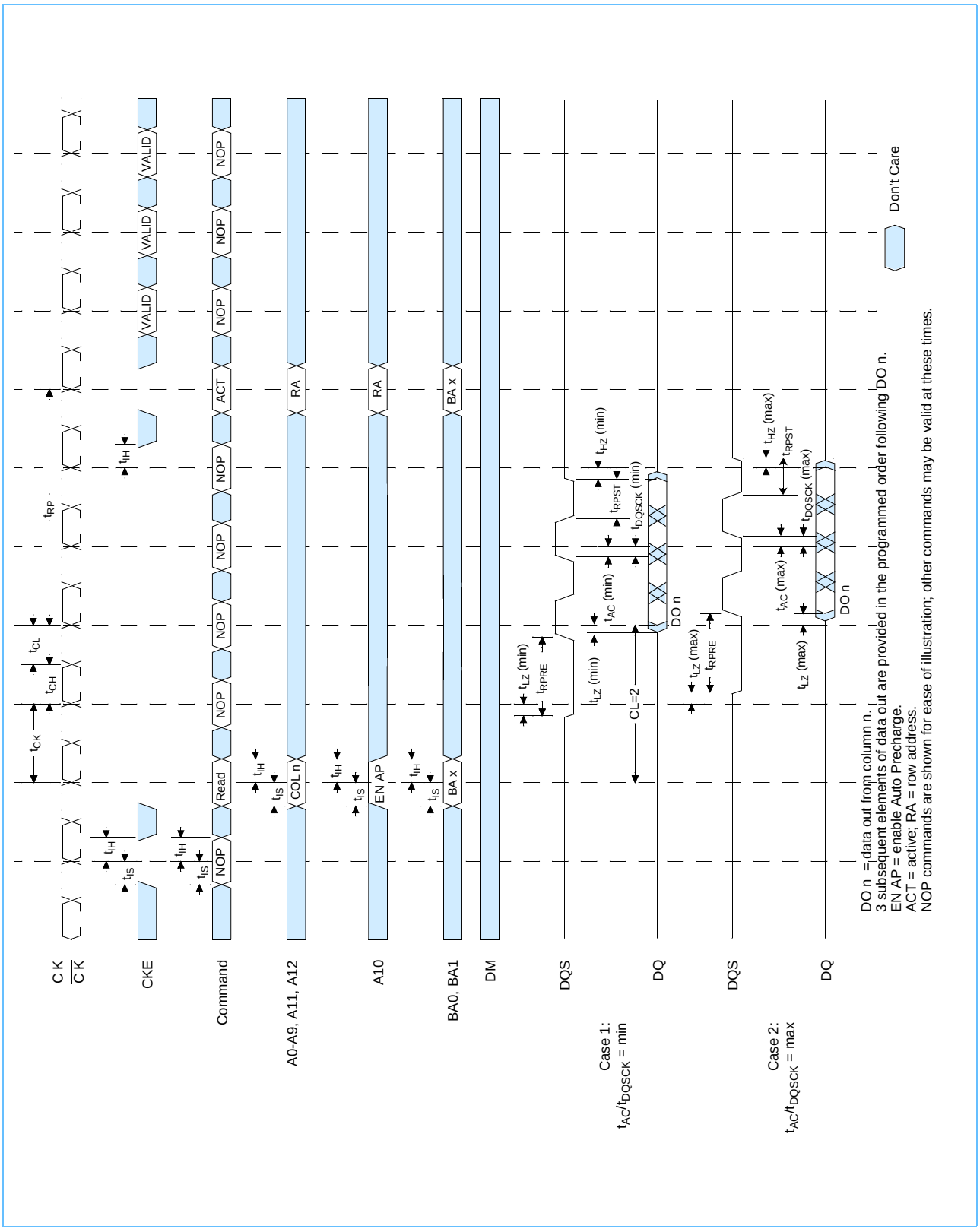


Read without Auto Precharge (Burst Length = 4)

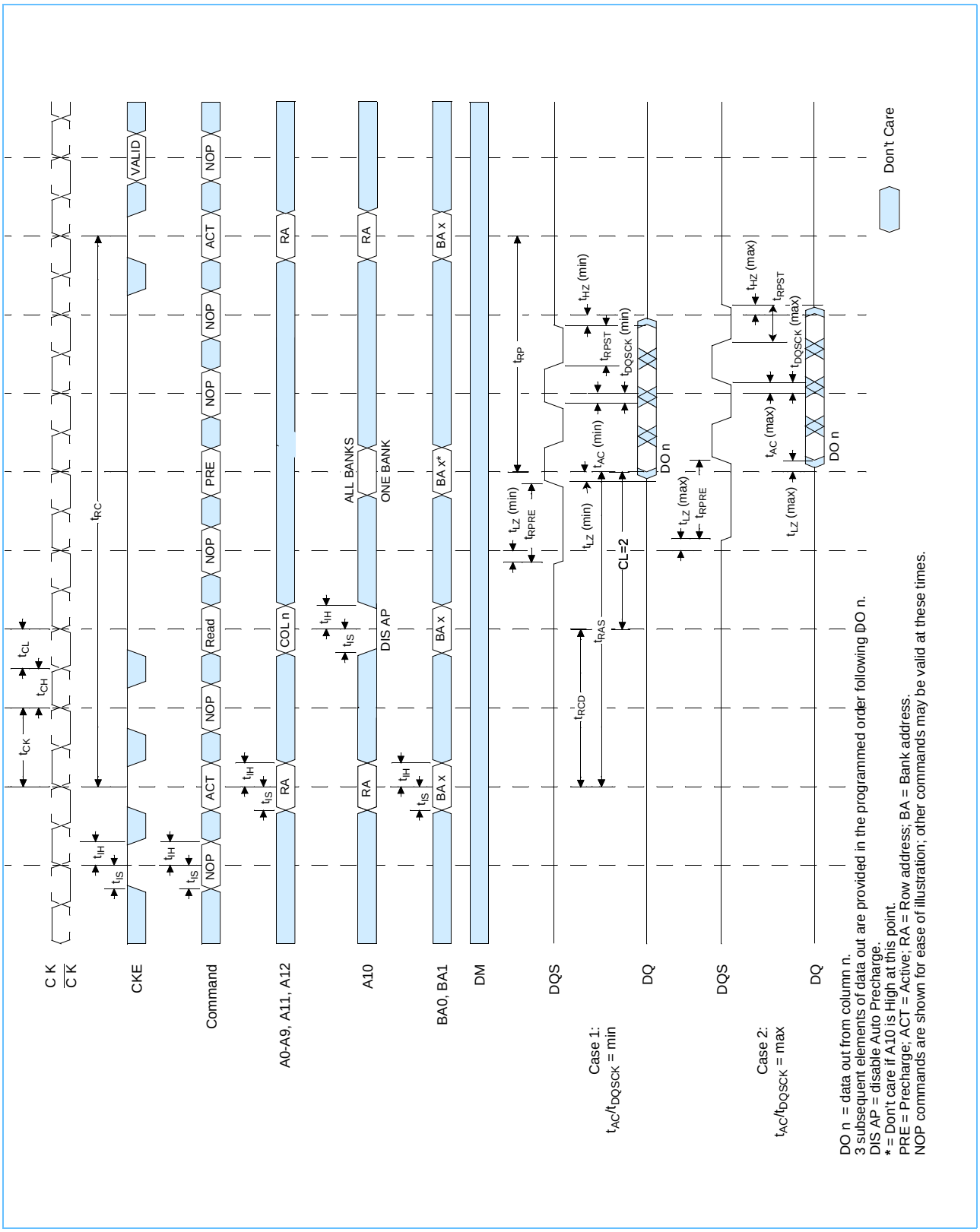


DO n = data out from column n.
3 subsequent elements of data out are provided in the programmed order following DO n.
DIS AP = Disable Auto Precharge.
* = Don't care if A10 is High at this point.
PRE = Precharge; ACT = Active; RA = Row address; BA = Bank address.
NOP commands are shown for ease of illustration; other commands may be valid at these times.

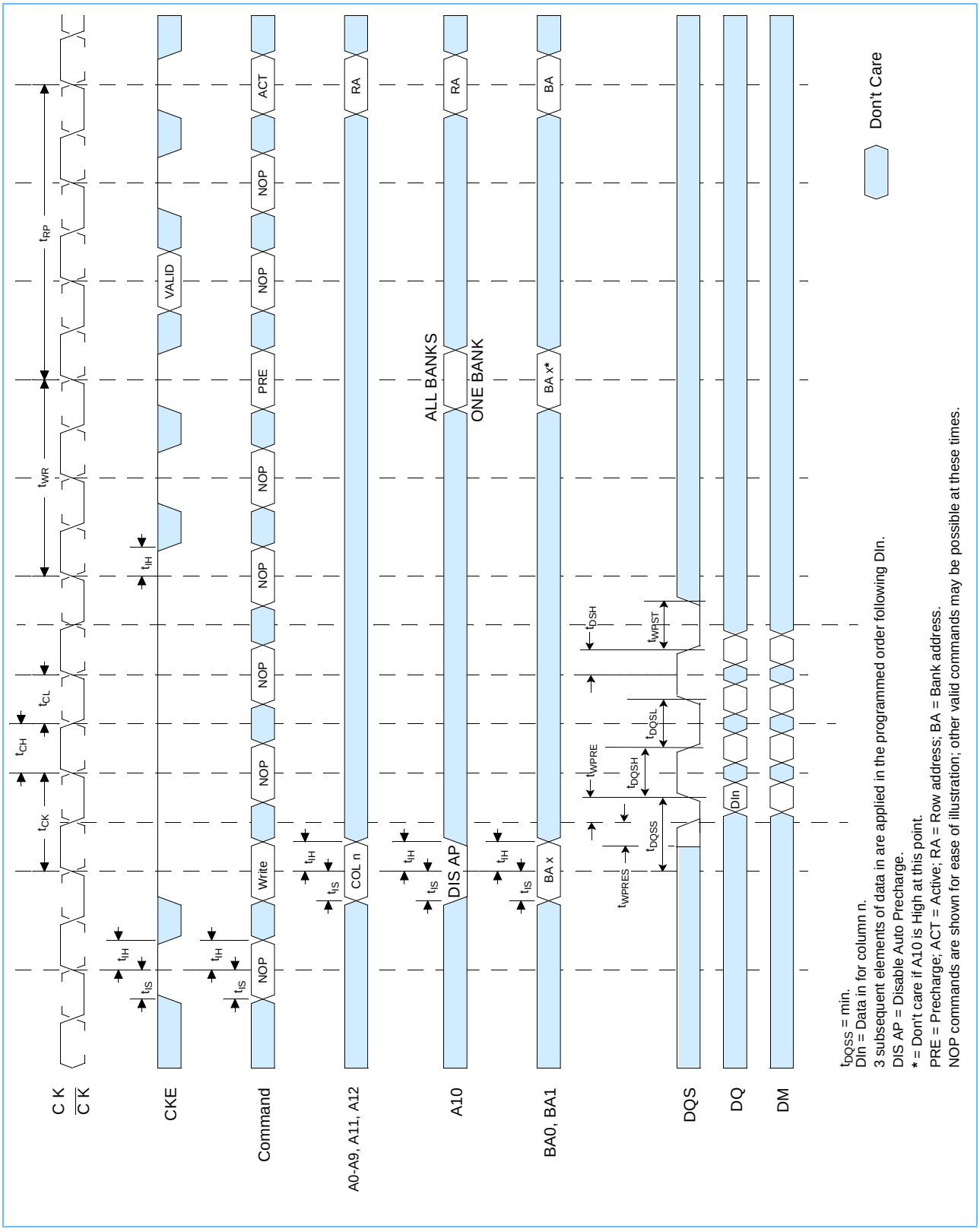
Read with Auto Precharge (Burst Length = 4)



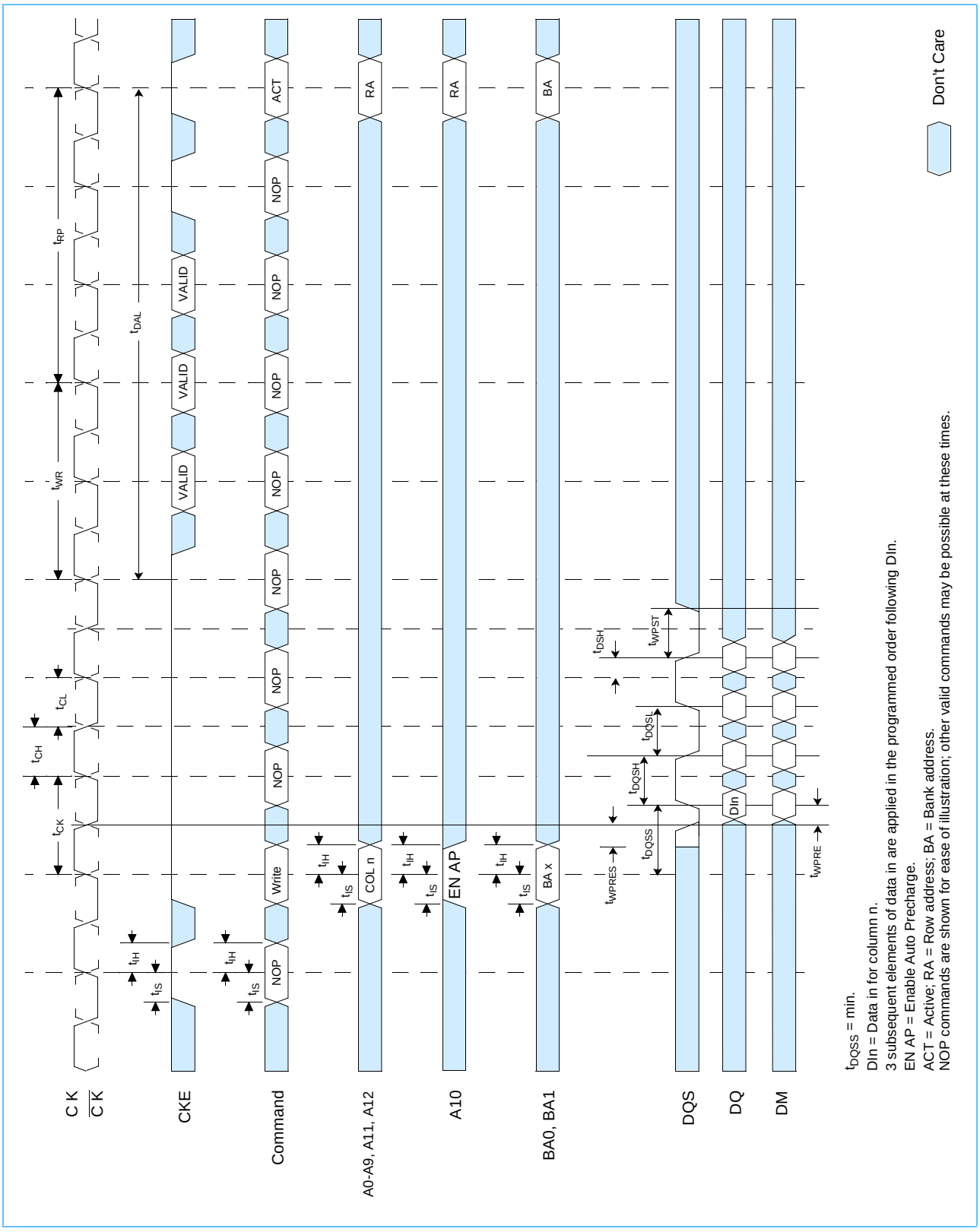
Bank Read Access (Burst Length = 4)



Write without Auto Precharge (Burst Length = 4)

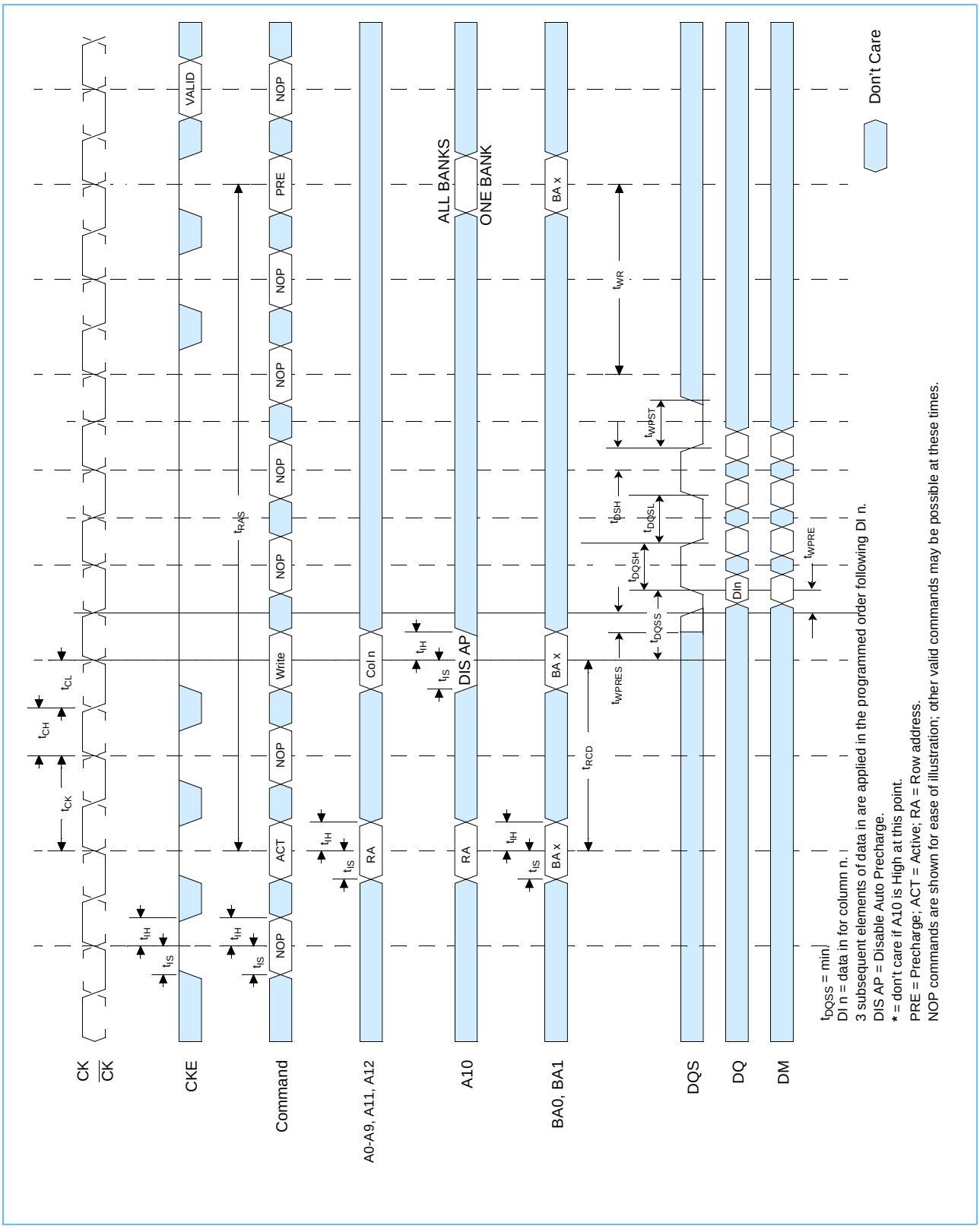


Write with Auto Precharge (Burst Length = 4)

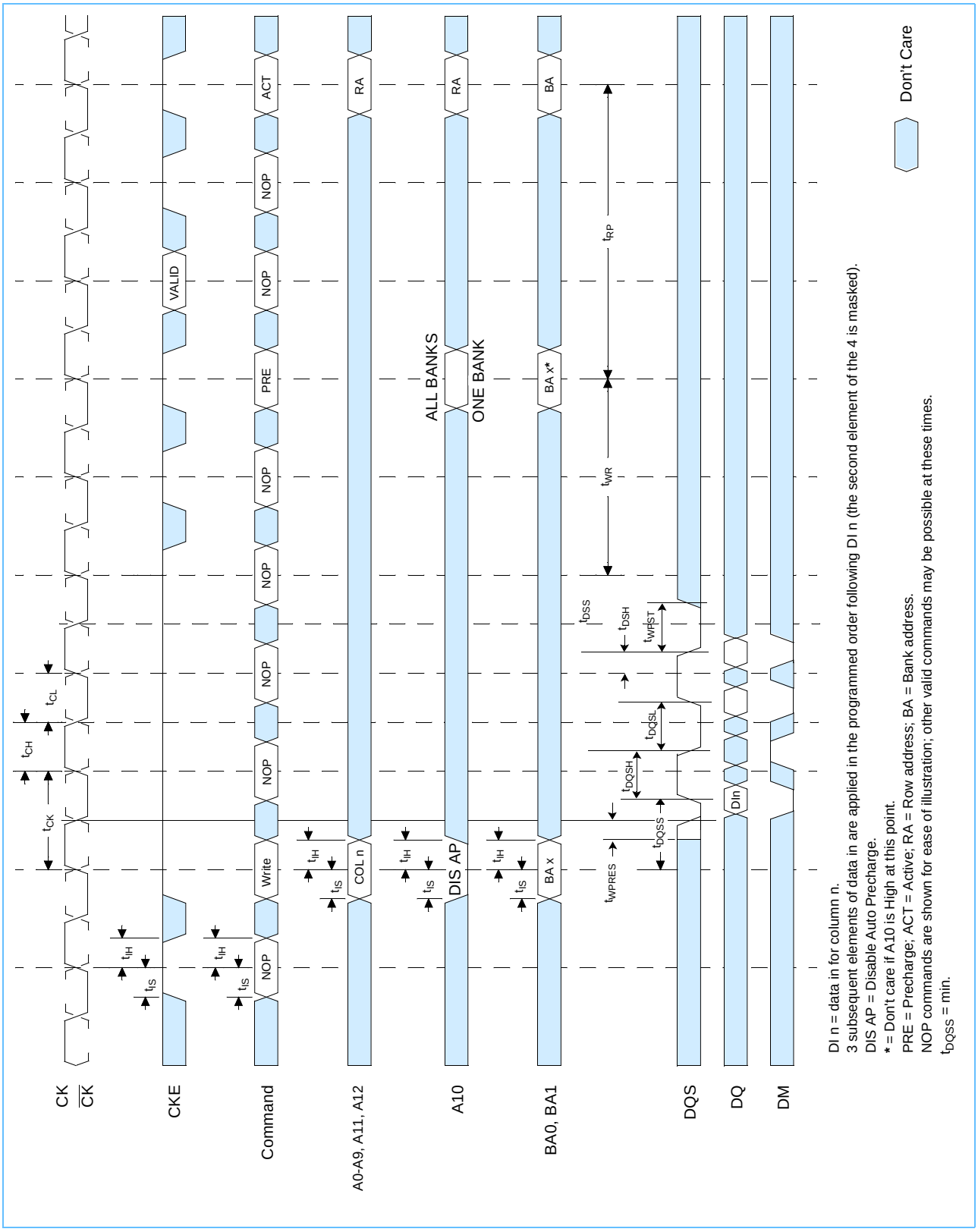


t_{DQSS} = min.
DIn = Data in for column n.
3 subsequent elements of data in are applied in the programmed order following DIn.
EN AP = Enable Auto Precharge.
ACT = Active; RA = Row address; BA = Bank address.
NOP commands are shown for ease of illustration; other valid commands may be possible at these times.

Bank Write Access (Burst Length = 4)

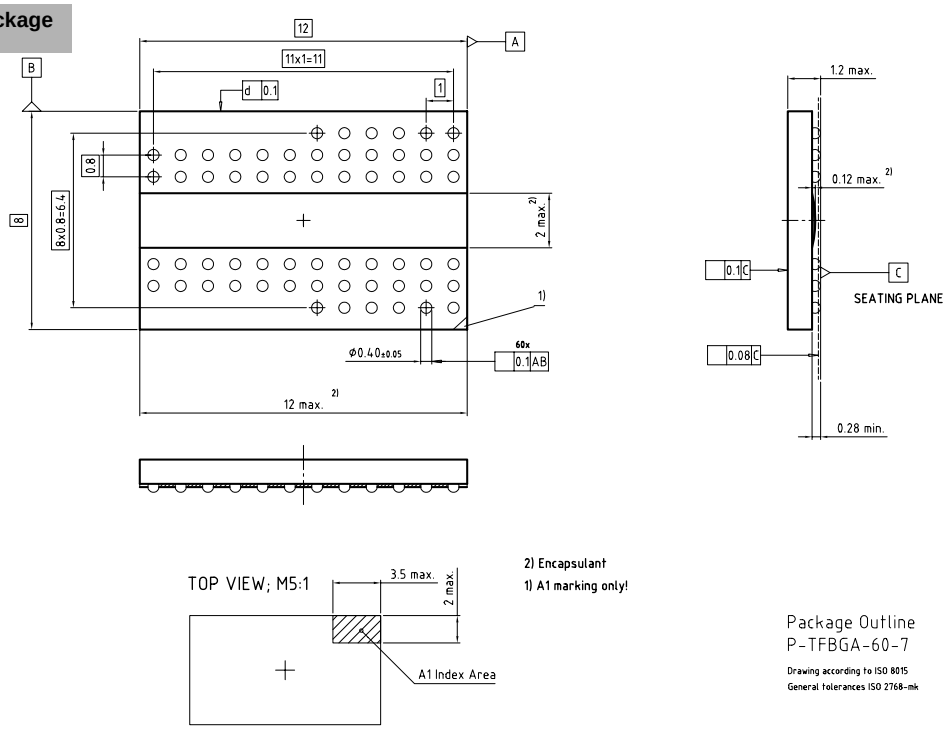


Write DM Operation (Burst Length = 4)



Package Dimensions

60 balls FBGA-Package
12mm x 8mm



Plastic Package, P-TSOPII-66
(400mil; 66 lead)
Thin Small Outline Package

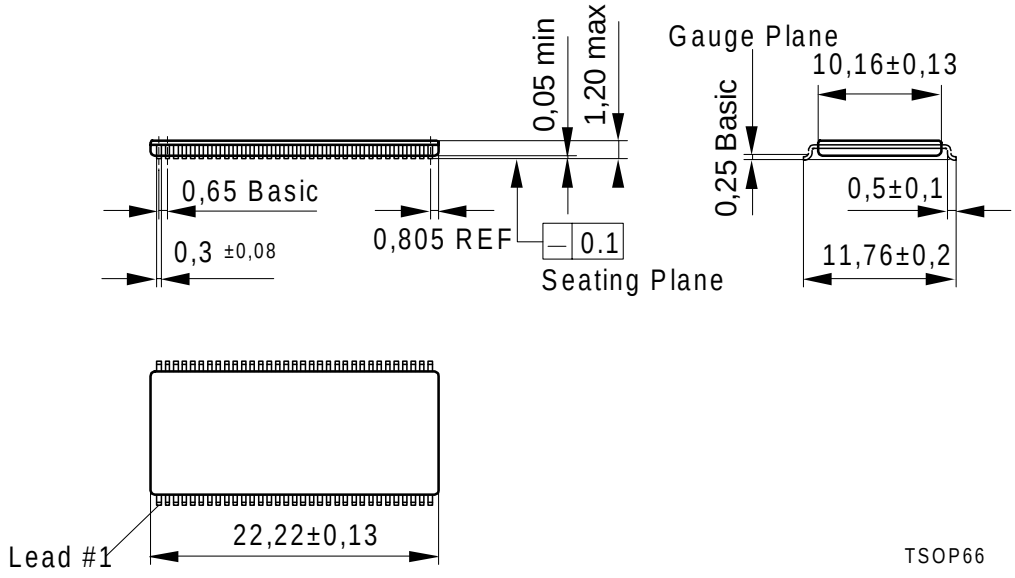


TABLE OF CONTENT

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