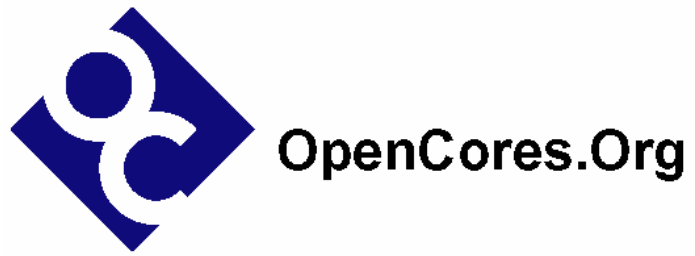

I²S Interface Specification

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Revision History

Rev.	Date	Author	Description
1.0	28/7/04	Geir Drange	Specification, first version
1.1	17/1/05	Geir Drange	RATIO equation correction

Contents

1

Introduction

The I²S-bus (Inter-IC Sound bus) is a serial link for transmitting stereo audio between devices in a system. Typical devices that use this bus are: ADC's, DAC's, DSP's, CPU's etc. The I²S bus was invented by Philips Semiconductor, but is now widely used by several semiconductor manufacturers.

The I²S interface core allows a Wishbone master to stream stereo audio to and from I²S capable devices.

2

Architecture

The I²S interface consists of two separate cores, a transmitter and a receiver. Both can operate in either master or slave mode. The I²S bus has 3 signals:

- SCK – clock
- WS – word select (left/right channel)
- SD – data

The master generates SCK and WS signals.

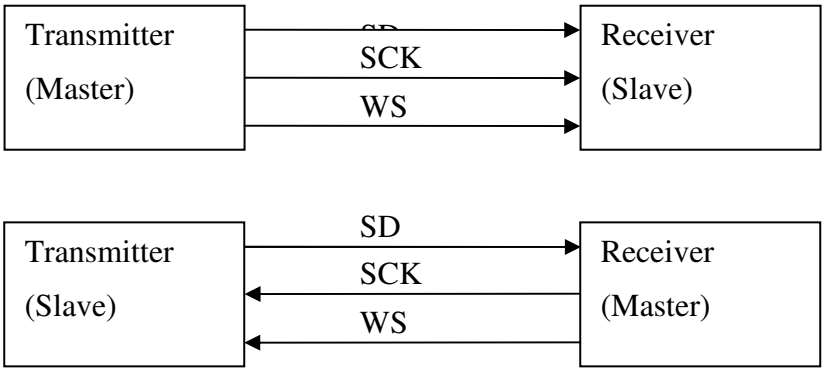

Figure 1: I²S Signal Direction

I²S signal timing:

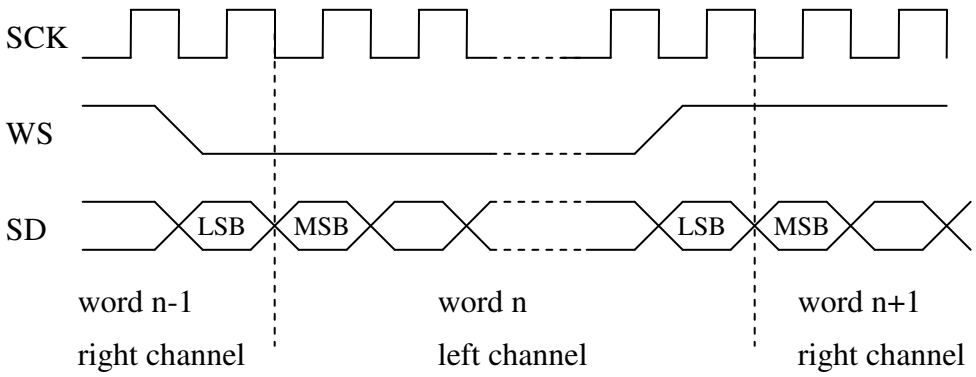

Figure 2: I²S Signal Timing

2.1 I²S Receiver

The receiver architecture is shown below.

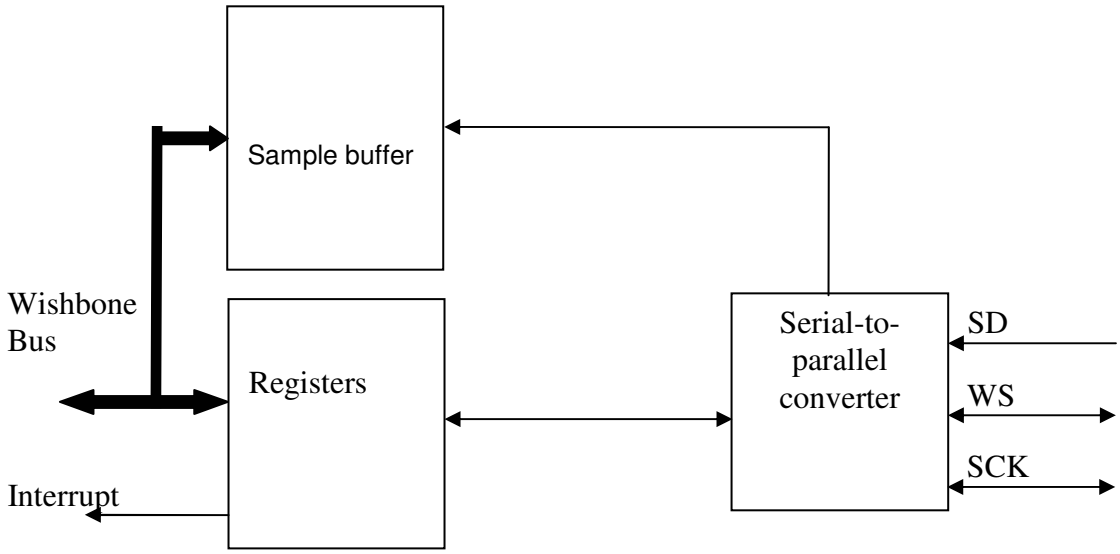

Figure 3: I²S Receiver Block Diagram

The serial to parallel converter receives serial data and stores audio data in the sample buffer. A set of registers define the operating mode of the receiver.

The size of the sample buffer is determined by the Wishbone address bus width. Minimum sample buffer size is 16bytes. The sample buffer is addressed by setting the most significant address bit to '1'. The sample buffer is divided in two equal parts, lower and upper, and the user will be notified when either is filled with audio data.

Master or slave mode is selected by a generic during compile time.

2.2 I²S Transmitter

The transmitter architecture is shown below.

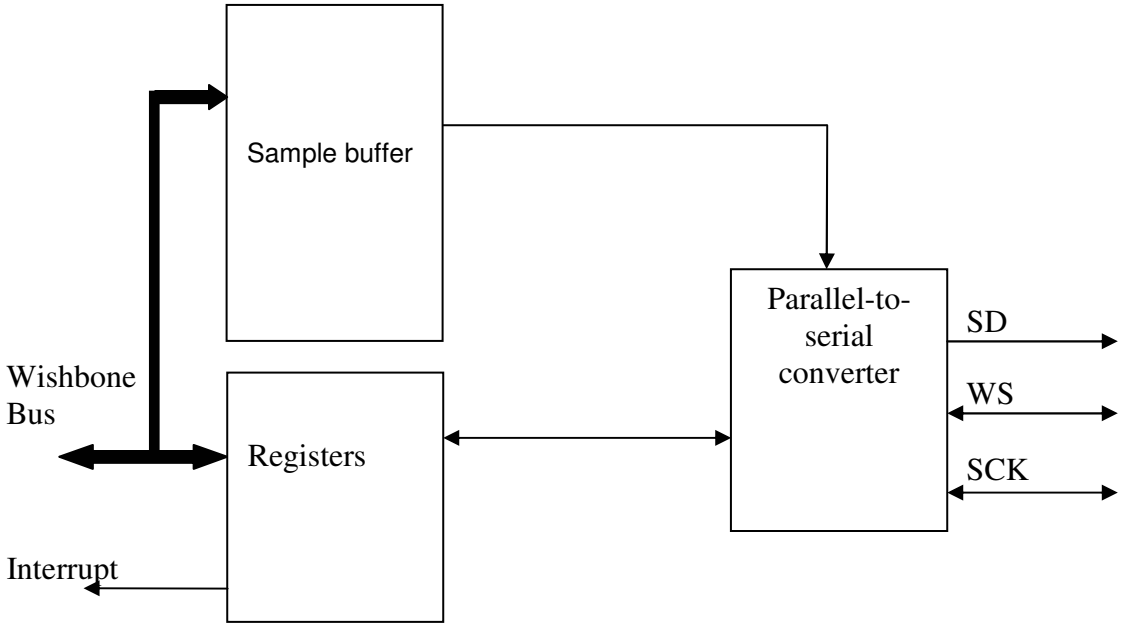

Figure 4: I²S Transmitter Block Diagram

A parallel to serial converter reads audio data from the sample buffer and transmits serial data on the SD line. A set of registers define the operating mode of the transmitter.

The size of the sample buffer is determined by the Wishbone address bus width. Minimum sample buffer size is 16bytes. The sample buffer is addressed by setting the most significant address bit to '1'. The sample buffer is divided in two equal parts, lower and upper, and the user will be notified when either is emptied of audio data.

Master or slave mode is selected by a generic during compile time.

3

Operation

This chapter contains operational guidelines for the cores.

3.1 Receiver

3.1.1 Resetting

The receiver is reset by a Wishbone bus reset or by clearing bit RXEN in RxConfig register.

3.1.2 Transferring data

If the receiver is master, set the RATIO bits in RxConfig to required I²S bit rate. Set RXEN to 1 to enable receiver.

3.2 Transmitter

3.2.1 Resetting

The transmitter is reset by a Wishbone bus reset or by clearing bit TXEN in TxConfig register.

3.2.2 Selecting transmit data rate

In master mode, the RATIO bits in TxConfig must be set to required bit rate.

$$bit\_rate = \frac{wishbone\_bus\_clock}{2 \cdot (RATIO + 2)}$$

The sample rate depends on the RES (data resolution) and bit rate:

$$sample\_rate = \frac{bit\_rate}{RES \cdot 2}$$

RATIO bits can then be calculated by:

$$RATIO = \frac{wishbone\_bus\_clock - sample\_rate \cdot RES \cdot 8}{sample\_rate \cdot RES \cdot 4}$$

3.2.3 Transferring data

Fill up the sample buffer with sample data then set the TXEN bit in TxConfig to start data transfer. Using interrupts, the lower or higher sample buffer can be filled up with new data as soon as its content has been transmitted.

4

Generics

The I²S interface has a number of generics that can be used to tailor the interface for various needs.

4.1 Generics for both transmitter and receiver

Name	Type	Range	Description
DATA_WIDTH	Integer	16/32	Wishbone data bus width. If using 16bit bus, some functionality is lost.
ADDR_WIDTH	Integer	5 - 32	Wishbone addresses bus width. The sample buffer occupies half the address range.

Table 1: Generics for transmitter and receiver

5

Registers

This section specifies all internal registers of the I²S interface.

5.1 I²S Receiver

5.1.1 Receiver registers - overview

Name	Address	Width	Access	Description
RxVersion	0x00	16/32	R	Version register
RxConfig	0x01	16/32	RW	Configuration register
RxIntMask	0x02	16/32	RW	Interrupt mask register
RxIntStat	0x03	16/32	RW	Interrupt status register

Table 2: Receiver registers

5.1.2 RxVersion – Description

The version register allows the SW to read out all the parameters that were used to generate the receiver.

Bit #	Access	Name	Description
31-16	R	-	Unused
15-13		-	Unused
12-6		ADRW	The value of **ADDR_WIDTH**
5		MAST	0: The receiver is slave 1: The receiver is master
4		DATW	0: **DATA_WIDTH** is 16bit 1: **DATA_WIDTH** is 32bit
3-0		VER	I²S version number = 1

Reset Value:

RxVersion: Depends on generics

5.1.3 RxConfig – Description

The configuration register controls the operation of the receiver. Note that only 16bit data resolution is supported when **DATA_WIDTH**=16.

Bit #	Access	Name	Description
31-22	R	-	Unused
21-16	RW	RES	Sample data resolution. Number of bits that are stored in each audio word in the sample buffer. Valid range is 16 to 32. If the received signal has fewer bits than set by RES, zero padding of LSB's is used. If the received signal has more bits than set by RES, LSB's are truncated.
15-8	RW	RATIO	**Master mode only:** Clock divider for the transmit frequency. The Wishbone bus clock is divided by a factor of (1+RATIO) to generate the serial transmit clock, SCK.
7-3	R	-	Unused
2	RW	RSWAP	0: Left channel is stored on even addresses 1: Left channel is stored on odd addresses
1		RINTEN	0: Interrupt output is disabled 1: Interrupt output is enabled
0		RXEN	0: Receiver is disabled 1: Receiver is enabled

Reset Value:

RxConfig: 0x0000

5.1.4 RxIntMask – Description

Set bit to 1 in the mask register to enable an interrupt source.

Bit #	Access	Name	Description
31-16	R	-	Unused
15-2	R	-	Unused
1		HSBF	Higher sample buffer full interrupt mask
0		LSBF	Lower sample buffer full interrupt mask

Reset Value:

RxIntMask: 0x0000

5.1.5 RxIntStat – Description

A bit in this register is set to 1 when an event occurs. If the corresponding bit in RxIntMask is set to 1, an interrupt is generated (if enabled). Write a 1 to a bit to clear the event. The interrupt signal goes inactive when all events have been cleared.

Bit #	Access	Name	Description

Bit #	Access	Name	Description
31-16	R	-	Unused
15-2	R	-	Unused
1		HSBF	Higher sample buffer full
0		LSBF	Lower sample buffer full

Reset Value:

RxIntStat: 0x0000

5.1.6 Receive sample data – Description

Format of data words in receive sample buffer:

Bit #	Access	Name	Description
31-16	R	DATH	Audio data if resolution is more than 16bits. Unused bits are 0.
15-0		DATL	Audio data. Bit 0 is LSB.

Reset Value:

Sample buffer: undefined

5.2 I²S Transmitter

5.2.1 Transmitter registers - overview

Name	Address	Width	Access	Description
TxVersion	0x00	16/32	R	Version register
TxConfig	0x01	16/32	RW	Configuration register
TxIntMask	0x02	16/32	RW	Interrupt mask register
TxIntStat	0x03	16/32	RW	Interrupt status register

Table 3: Transmitter registers

5.2.2 TxVersion – Description

The version register allows the SW to read out all the parameters that were used to generate the receiver.

Bit #	Access	Name	Description
31-16	R	-	Unused
15-13		-	Unused
12-6		ADRW	The value of **ADDR_WIDTH**
5		MAST	0: The transmitter is slave 1: The transmitter is master

Bit #	Access	Name	Description
4		DATW	0: **DATA_WIDTH** is 16bit 1: **DATA_WIDTH** is 32bit
3-0		VER	I²S version number = 1

Reset Value:

TxVersion: - depends on generics

5.2.3 TxConfig – Description

The configuration register controls the operation of the transmitter. Note that only 16bit data resolution is supported when **DATA_WIDTH**=16.

Bit #	Access	Name	Description
31-22	R	-	Unused
21-16	RW	RES	Sample data resolution. Number of bits that are transmitted from each audio word in the sample buffer. Valid range is 16 to 32.
15-8	RW	RATIO	**Master mode only:** Clock divider for the transmit frequency. The Wishbone bus clock is divided by a factor of (1+RATIO) to generate the serial transmit clock, SCK.
7-3	R	-	Unused
2	RW	TSWAP	0: Left channel is stored on even addresses 1: Left channel is stored on odd addresses
1		TINTEN	0: Interrupt output is disabled 1: Interrupt output is enabled
0		TXEN	0: Receiver is disabled 1: Receiver is enabled

Reset Value:

TxConfig: 0x0000

5.2.4 TxIntMask – Description

Set bit to 1 in the mask register to enable an interrupt source.

Bit #	Access	Name	Description
31-16	R	-	Unused
15-2	R	-	Unused
1	RW	HSBF	Higher sample buffer empty
0		LSBF	Lower sample buffer empty

Reset Value:

TxIntMask: 0x0000

5.2.5 TxIntStat – Description

A bit in this register is set to 1 when an event occurs. If the corresponding bit in TxIntMask is set to 1, an interrupt is generated (if enabled). Write a 1 to a bit to clear the event. The interrupt signal goes inactive when all events have been cleared.

Bit #	Access	Name	Description
31-16	R	-	Unused
15-2	R	-	Unused
1	RW	HSBF	Higher sample buffer empty
0		LSBF	Lower sample buffer empty

Reset Value:

TxIntStat: 0x0000

5.2.6 Transmit sample data – Description

Format of data words in transmit sample buffer.

Bit #	Access	Name	Description
31-16	W	DATH	Audio data if resolution is more than 16bits. If less than 32bit resolution, set MSB's to zero.
15-0		DATL	Audio data. Bit 0 is LSB.

Reset Value:

Sample buffer: undefined

6

Clocks

The I²S interface uses the Wishbone interface clock only.

Name	Source	Rates (MHz)			Remarks	Description
		Max	Min	Resolution		
wb_clk_i	-	-		-	Must be at least 8 times higher than I²S bit rate	System clock.

Table 4: List of clocks

7

IO Ports

7.1 Wishbone interface signals (receiver & transmitter)

Port	Width	Direction	Description
wb_ack_o	1	Output	Bus cycle acknowledge
wb_adr_i	8-32	Input	Address bus
wb_bte_i	2	Input	Burst type extension
wb_clk_i	1	Input	Clock
wb_cti_i	3	Input	Cycle type identifier
wb_cyc_i	1	Input	Valid bus cycle
wb_dat_i	16/32	Input	Data to core
wb_dat_o	16/32	Output	Data from core
wb_rst_i	1	Input	Asynchronous reset
wb_sel_i	1	Input	Select Input
wb_stb_i	1	Input	Strobe
wb_we_i	1	Input	Write enable

Table 5: Wishbone signals

Description	Specification
General description	16/32bit slave
Supported cycles	SLAVE, READ/WRITE SLAVE, BLOCK READ/WRITE SLAVE, Incrementing burst cycle (linear)
Data port, size Data port, granularity Data port, maximum operand size Data transfer ordering Data transfer sequencing	16 or 32bit 16 or 32bit 16 or 32bit Big/little endian Undefined

Wishbone properties

7.2 I²S Receiver signals, slave mode

Top level file is rx_i2s_tops.vhd.

Port	Width	Direction	Description
rx_sd_i	1	Input	I²S serial data in
rx_ws_i	1	Input	Word select signal
rx_sck_i	1	Input	Serial clock

Table: Receiver signals, slave

7.3 I²S Receiver signals, master mode

Top level file is rx_i2s_topm.vhd.

Port	Width	Direction	Description
rx_sd_i	1	Input	I²S serial data in
rx_ws_o	1	Output	Word select signal
rx_sck_o	1	Output	Serial clock

Table: Receiver signals, master

7.4 I²S Transmitter signals, slave mode

Top level file is tx_i2s_tops.vhd.

Port	Width	Direction	Description
tx_sd_o	1	Output	I²S serial data out
tx_ws_i	1	Input	Word select signal
tx_sck_i	1	Input	Serial clock

Table: Transmitter signals, slave

7.5 I²S Transmitter signals, master mode

Top level file is tx_i2s_topm.vhd.

Port	Width	Direction	Description
tx_sd_o	1	Output	I²S serial data out
tx_ws_o	1	Output	Word select signal
tx_sck_o	1	Output	Serial clock

Table: Transmitter signals, master