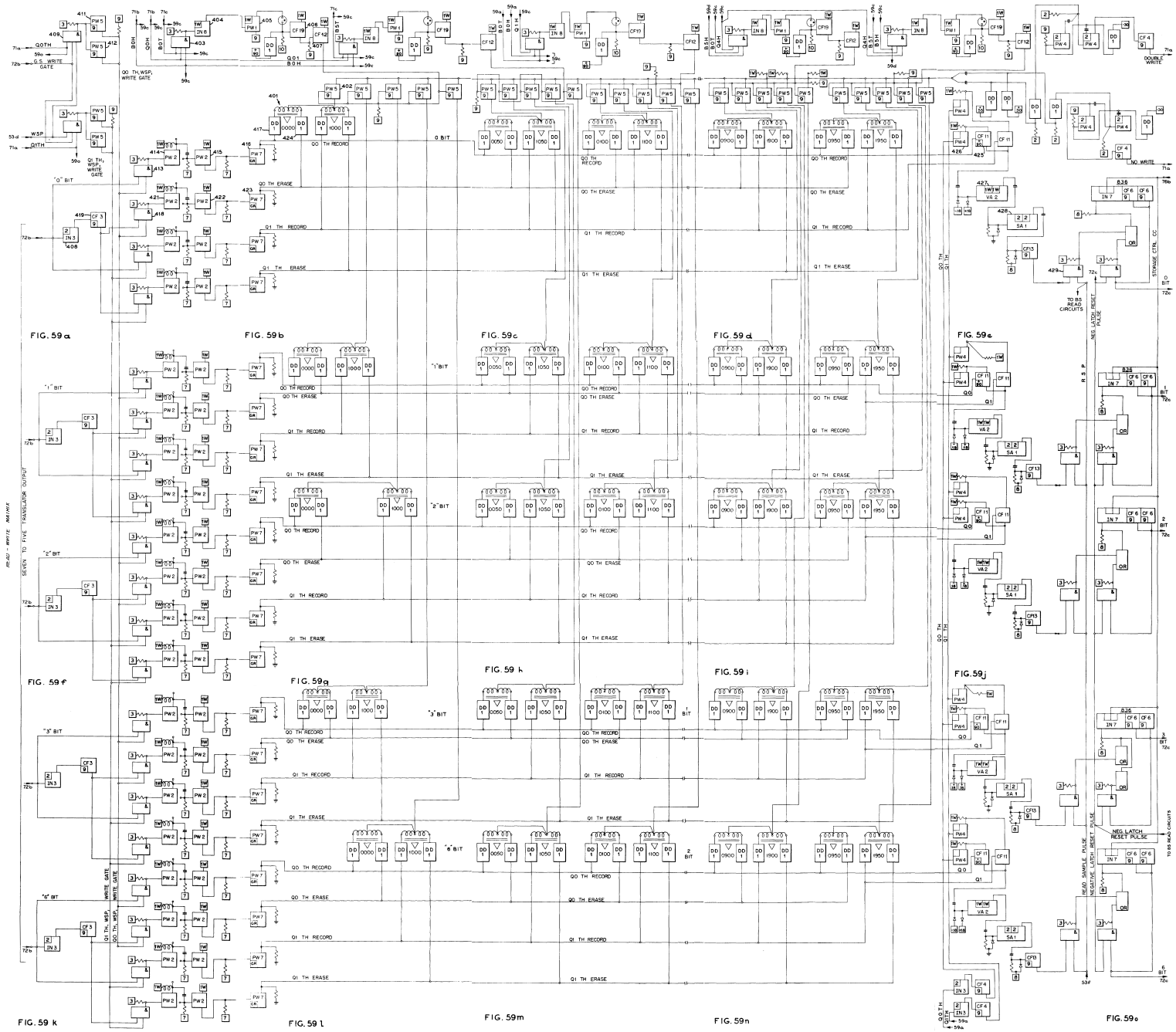
READ - WRITE MATRIX
SEVEN TO FIVE TRANSLATOR OUTPUT
FIG. 59a
FIG. 59b
FIG. 59c
FIG. 59d
FIG. 59e
FIG. 59f
FIG. 59g
FIG. 59h
FIG. 59i
FIG. 59j
FIG. 59k
FIG. 59l
FIG. 59m
FIG. 59n
FIG. 59o
"0" BIT
"1" BIT
"2" BIT
"3" BIT
"6" BIT
0 BIT
1 BIT
2 BIT
3 BIT
6 BIT
Q0 TH RECORD
Q0 TH ERASE
Q1 TH RECORD
Q1 TH ERASE
WRITE GATE
NEG. LATCH RESET PULSE
NEG. SINGLE PULSE
TO 85 READ CIRCUITS
STORAGE CTRL. CC
DOUBLE WRITE
NO WRITE