IrDA Core Specification

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Revision History

Rev.	Date	Author	Description
0.1	30/1/01	Jacob Gorban	First Draft

Contents

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Introduction

IrDA core enables infrared (IR) wireless serial communication between various devices one in the vicinity of the other, up to 1 meter distance using standard IR transceivers. It implements the lower (physical) level of OSI structure.

The IR communication is a half-duplex protocol defined for the following baud rates: 2400 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps and also 576000 bps, 1152000 bps and 4000000 bps.

There are three different modulation techniques defined for the various data rates:

- Communication speeds up to 115.2kb/s use protocol scheme similar to serial UART communication.
- The 0.576Mb/s and 1.152Mb/s differ in their pulse duration and encoding scheme.
- The 4Mb/s speed uses a totally different modulation and encoding scheme – 4PPM.

The specifications of this core are based on the following documents:

- Infrared Data Association Serial infrared Physical Layer Specifications, version 1.3, Oct 1998.
- Infrared Data Association Serial infrared Link Access Protocol (IrLAP), version 1.1, June 1996.

Features:

- Designed for all standard IR transceivers.
- Implements WISHBONE bus interface
- Up to 4Mbit communication speed
- Programmable clock selection
- Loopback option for testing
- Works with WISHBONE bus clock
- Can request DMA transfers

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IO ports

2.1 WISHBONE interface signals

Port	Width	Direction	Description
CLK_I	1	Input	Block's clock input
RST_I	1	Input	Synchronous Reset
ADR_I	4	Input	Used for register selection
DAT_I	8	Input	Data input
DAT_O	8	Output	Data output
WE_I	1	Input	Write or read cycle selection
STB_I	1	Input	Specifies transfer cycle
CYC_I	1	Input	A bus cycle is in progress
ACK_O	1	Output	Acknowledge of a transfer
INT_O	1	Output	Interrupt output
DMA_REQ_T	1	Output	DMA transfer request for transmitter
DMA_ACK_T	1	Input	DMA end of transfer acknowledgment
DMA_REQ_R	1	Output	DMA transfer request from receiver
DMA_ACK_R	1	Input	DMA end of transfer acknowledgment

2.2 External connections

Port	Width	Direction	Description
TX_O	1	Output	The output to the IR transmitter off chip
RX_I	1	Input	The input from the off chip IR receiver

These signals need to be connected to external IR transceiver via two pins on the chip.

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Clocks

Clocks table:

Name	Source	Rates (MHz)			Remarks	Description
		Max	Min	Resolution		
clk_wb	Wishbone bus	?	?	?	None	Wishbone bus clock

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Registers

The register access is divided between the 2 modes of operation: SIR and MIR/FIR. Only one register can be accessed in both modes: Master Control Register (MCTR).
In SIR mode MIR/SIR register are not accessible and only UART registers are visible. The UART in the IrDA controller is identical to the UART core. However, not all its features are required for SIR transmissions.

The registers for MIR/FIR mode appear after the description of registers in SIR mode.

4.1 Registers list in SIR mode

Name	Address	Width	Access	Description
Master Control Register (MCTR)	8	8	R/W	Controls global settings of the core
Receiver Buffer	0	8	R	Receiver FIFO output
Transmitter Holding Register (THR)	0	8	W	Transmit FIFO input
Interrupt Enable	1	8	RW	Enable/Mask interrupts generated by the UART
Interrupt Identification	2	8	R	Get interrupt information
FIFO Control	2	8	W	Control FIFO options
Line Control Register	3	8	RW	Control connection
Modem Control	4	8	W	Controls modem (ignore)
Line Status	5	8	R	Status information
Modem Status	6	8	R	Modem Status (ignore)

In addition, there are 4 Clock Divisor registers that together form one 32-bit register (as opposed to the 2 8-bit registers in the 16550). The expansion is to accommodate higher clock speed of modern systems, especially since this is not a stand-alone chip but a SoC core.

The registers can be accessed when the 7th (DLAB) bit of the Line Control Register is set to ‘1’. At this time the above registers at addresses 0-3 can’t be accessed.

Name	Address	Width	Access	Description
Divisor Latch Byte 1 (LSB)	0	8	RW	The LSB of the divisor latch
Divisor Latch Byte 2	1	8	RW	Second byte of DL
Divisor Latch Byte 3	4	8	RW	Third byte of DL
Divisor Latch Byte 4 (MSB)	5	8	RW	The MSB of the divisor latch

4.1.1 Master Control register

Master Control registers is available both in SIR and in MIR/FIR modes. It controls the global parameters of the controller, like global enable, mode select etc.

Bit #	Access	Description
0	R/W	Core_En, IrDA Core Enable '1' – the core is enabled. '0' – the core communication is disabled.
1	R/W	Mode, Select transmit/receive mode '0' – Receive mode '1' – Transmit mode
2	R/W	Loopback mode select '0' – No loopback '1' – Loopback mode enabled
4:3	R/W	Master_Speed, Select the type of modulation used based on speed group '00' – Low speed, SIR (2.4kbps to 115.2kbps) '01' – High speed, FIR (4Mbps) '10' – Medium speed (MIR), half speed (0.576Mbps). '11' – Medium speed (MIR), full speed (1.152Mbps).
5	R/W	Negate (complement) transmitter output. Set to 1 if you want to negate output signal to accommodate transceivers that send signal on low input. '0' – No negation process. High level signal drives the LED '1' – Complement output signals.
6	R/W	Negate received signals. '0' – Don't complement input signal '1' – Complement input signals.
7	R/W	Use DMA for data transmission. '0' – DMA transfers will not be requested '1' – DMA is used for data transfer, both reception and transmission.

Reset value: 00h

4.1.2 Interrupt Enable Register (IER)

This register allows enabling and disabling interrupt generation by the UART.

Bit #	Access	Description
0	RW	Received Data available interrupt '0' – disabled '1' – enabled
1	RW	Transmitter Holding Register empty interrupt '0' – disabled '1' – enabled
2	RW	Receiver Line Status Interrupt '0' – disabled '1' – enabled
3	RW	Modem Status Interrupt '0' – disabled '1' – enabled
7-4	RW	Reserved. Should be logic '0'.

Reset Value: 0000h

4.1.3 Interrupt Identification Register (IIR)

The IIR enables the programmer to retrieve what is the current highest priority pending interrupt.
Bit 0 indicates that an interrupt is pending when it's logic '0'. When it's '1' – no interrupt is pending.
The following table displays the list of possible interrupts along with the bits they enable, priority, and their source and reset control.

Bit 3	Bit 2	Bit 1	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	1	1	1st	Receiver Line Status	Parity, Overrun or Framing errors or Break Interrupt	Reading the Line Status Register
0	1	0	2nd	Receiver Data available	FIFO trigger level reached	FIFO drops below trigger level
1	1	0	2nd	Timeout Indication	There's at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 Char times.	Reading from the FIFO (Receiver Buffer Register)
0	0	1	3rd	Transmitter Holding Register empty	Transmitter Holding Register Empty	Writing to the Transmitter Holding Register or reading the IIR.
0	0	0	4th	Modem Status	CTS, DSR, RI or DCD.	Reading the Modem status register.

Bits 4 and 5: Logic '0'.
Bits 6 and 7: Logic '1' for compatibility reason.

4.1.4 FIFO Control Register (FCR)

The FCR allows selection of the FIFO trigger level (the number of bytes in FIFO required to enable the Received Data Available interrupt). In addition, the FIFOs can be cleared using this register.

Bit #	Access	Description
0	W	Ignored (Used to enable FIFOs in NS16550D). Since this UART only supports FIFO mode, this bit is ignored.
1	W	Writing a '1' to bit 1 clears the Receiver FIFO and resets its logic. But it doesn't clear the shift register.
2	W	Writing a '1' to bit 2 clears the Transmitter FIFO and resets its logic. The shift register is not cleared.
5-3	W	Ignored
7-6	W	Define the Receiver FIFO Interrupt trigger level '00' – 1 byte '01' – 4 bytes '10' – 8 bytes '11' – 14 bytes

4.1.5 Line Control Register (LCR)

The line control register allows the specification of the format of the asynchronous data communication used. A bit in the register also allows access to the Divisor Latches, which define the baud rate. Reading from the register is allowed to check the current settings of the communication.

Bit #	Access	Description
1-0	RW	Select number of bits in each character '00' – 5 bits '01' – 6 bits '10' – 7 bits '11' – 8 bits
2	RW	Specify the number of generated stop bits '0' – 1 stop bit '1' – 1.5 stop bits when 5-bit character length selected and 2 bits otherwise Note that the receiver always checks the first stop bit only.
3	RW	Parity Enable '0' – No parity '1' – Parity bit is generated on each outgoing character and is checked on each incoming one.
4	RW	Even Parity select '0' – Odd number of '1' is transmitted and checked in each word (data and parity combined). In other words, if the data has an even number of '1' in it, then the parity bit is '1'. '1' – Even number of '1' is transmitted in each word.
5	RW	Stick Parity bit. '0' – Stick Parity disabled '1' - If bits 3 and 4 are logic '1', the parity bit is transmitted and checked as logic '0'. If bit 3 is '1' and bit 4 is '0' then the parity bit is transmitted and checked as '1'.
6	RW	Break Control bit '1' – the serial out is forced into logic '0' (break state). '0' – break is disabled
7	RW	Divisor Latch Access bit. '1' – The divisor latches can be accessed '0' – The normal registers are accessed

4.1.6 Modem Control Register (MCR)

The modem control register allows transferring control signals to a modem connected to the UART.

Ignore this register in IrDA.

4.1.7 Line Status Register (LSR)

Bit #	Access	Description
0	R	Data Ready (DR) indicator. '0' – No characters in the FIFO '1' – At least one character has been received and is in the FIFO.
1	R	Overrun Error (OE) indicator '1' – If the FIFO is full and another character has been received in the receiver shift register. If another character is starting to arrive, it will overwrite the data in the shift register but the FIFO will remain intact. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. '0' – No overrun state
2	R	Parity Error (PE) indicator '1' – The character that is currently at the top of the FIFO has been received with parity error. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. '0' – No parity error in the current character
3	R	Framing Error (FE) indicator '1' – The received character at the top of the FIFO did not have a valid stop bit. The UART core tries re-synchronizing by assuming that the bit received was a start bit. Of course, generally, it might be that all the following data is corrupt. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. '0' – No framing error in the current character
4	R	Break Interrupt (BI) indicator '1' – A break condition has been reached in the current character. The break occurs when the line is held in logic 0 for a time of one character (start bit + data + parity + stop bit). In that case, one zero character enters the FIFO and the UART waits for a valid start bit to receive next character. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. '0' – No break condition in the current character
5	R	Transmit FIFO is empty. '1' – The transmitter FIFO is empty. Generates Transmitter Holding Register Empty interrupt. The bit is cleared in the

Bit #	Access	Description
		following cases: The LSR has been read, the IIR has been read or data has been written to the transmitter FIFO. '0' – Otherwise
6	R	Transmitter Empty indicator. '1' – Both the transmitter FIFO and transmitter shift register are empty. The bit is cleared upon reading from the register or upon writing data to the transmit FIFO. '0' – Otherwise
7	R	'1' – At least one parity error, framing error or break indications have been received and are inside the FIFO. The bit is cleared upon reading from the register. '0' – Otherwise.

4.1.8 Modem Status Register (MSR)

The register displays the current state of the modem control lines. Also, four bits also provide an indication in the state of one of the modem status lines. These bits are set to '1' when a change in corresponding line has been detected and they are reset when the register is being read.

Ignore this register in IrDA.

4.1.9 Divisor Latches

The divisor latches can be accessed by setting the 7th bit of LCR to '1'. You should restore this bit to '0' after setting the divisor latches in order to restore access to the other registers that occupy the same addresses. The 4 bytes form one 32-bit register, which is internally accessed as a single number. You should therefore set all 4 bytes of the register to ensure normal operation. The register is set to the default value of 0 on reset, which disables all serial I/O operations in order to ensure explicit setup of the register in the software. The value set should be equal to (system clock speed) / (16 x desired baud rate).

4.2 Registers list in MIR/FIR modes

Name	Address	Width	Access	Description
Master Control Register (MCTR)	8	8	R/W	Controls global settings of the core
Transmitter FIFO	0	32	W	Write to this address to send data in all modes
Receiver FIFO	0	32	R	Read from this register to retrieve data in all modes
Interrupt Enable Register	1	8	R/W	Defines interrupt conditions
Interrupt Identification Register	2	8	R	Describes pending interrupts
FIFO Control Register	3	8	R/W	Allows control of FIFO parameters
Line Control Register	4	8	R/W	Break output and end of frame behavior control
Outgoing Frame Data Length Register	5	16	R/W	Controls end of frame in another fashion
Incoming Frame Data Length Register	6	16	R	Length of received incoming data
Clock Divisor Register	7	32	R/W	Define internal clock generation

4.2.1 Master Control register

Master Control registers is available both in SIR and in MIR/FIR modes. It controls the global parameters of the controller, like global enable, mode select etc.

Bit #	Access	Description
0	R/W	Core_En, IrDA Core Enable '1' – the core is enabled. '0' – the core communication is disabled.
1	R/W	Mode, Select transmit/receive mode '0' – Receive mode '1' – Transmit mode
2	R/W	Loopback mode select '0' – No loopback '1' – Loopback mode enabled
4:3	R/W	Master_Speed, Select the type of modulation used based on speed group '00' – Low speed, SIR (2.4kbps to 115.2kbps) '01' – High speed, FIR (4Mbps) '10' – Medium speed (MIR), half speed (0.576Mbps). '11' – Medium speed (MIR), full speed (1.152Mbps).
5	R/W	Negate (complement) transmitter output. Set to 1 if you want to negate output signal to accommodate transceivers that send signal on low input. '0' – No negation process. High level signal drives the LED '1' – Complement output signals.
6	R/W	Negate received signals. '0' – Don't complement input signal '1' – Complement input signals.
7	R/W	Use DMA for data transmission. '0' – DMA transfers will not be requested '1' – DMA is used for data transfer, both reception and transmission.

Reset value: 00h

4.2.2 Interrupt Enable Register

Write to this register to enable or disable specific interrupts.
Read from this register to check what interrupts are enabled.
An interrupt is enabled by writing a '1' to the appropriate bit.

Bit #	Access	Description
0	R/W	Receiver FIFO trigger level reached interrupt
1	R/W	Received End of Frame
2	R/W	CRC check on input data failed
3	R/W	Receiver FIFO overrun
4	R/W	Receiver Error This interrupt will be requested when illegal data has been received or break was detected.
5	R/W	Transmitter FIFO low interrupt. This interrupt will be requested based on the Transmitter low trigger level.
6	R/W	Transmitter underrun. The transmitter wants to send more data but no data is available in the FIFO. In this case the controller will transmit a break for the receiving side to abort reception.
7	R/W	Reserved

Reset value: 00h

4.2.3 Interrupt Identification (Status) Register

This is a read only register that displays the current status of the controller. It can be either used to identify the interrupt received or to check the status at any time by reading from it. The status bits in the register are always set, regardless of the settings in the Interrupt Enable register but will not generate an interrupt if masked. Bits 0 to 6 correspond to bits 0 to 6 in Interrupt Enable Register. Bit 7 provides additional information.

Bit #	Access	Description
0	R	Receiver FIFO trigger level reached. This bit will be set when the number of word in the receiver FIFO is above the high trigger level. It will be cleared when data is read from the FIFO and its count drops trigger level. The matching interrupt, if enabled, will be issued on the rising edge of this bit. If the DMA mode is enabled then a DMA request to read the data will be sent.
1	R	Received End of Frame. This bit will be set when the last byte in frame is within the receiver FIFO. An interrupt is generated on rising edge.
2	R	CRC check on input data failed. This bit is raised when after receiving the frame the CRC check on incoming data is failed. This bit is cleared after reading from the register.
3	R	Receiver FIFO overrun error occurred. This bit is raised when the FIFO is full and new data was received. In that case the new data won't be transferred to the FIFO but the bit will be set and any new data will overwrite the previous received byte. The bit is cleared upon reading from the register.
4	R	Receiver Error. This bit is set when an unexpected or illegal data has been received. This can be a break in transmission, illegal 4PPM chip values in 4Mbit mode or framing errors. This bit is cleared upon reading from the register.
5	R	Transmitter FIFO is low. This bit is raised and held while the count of words in the FIFO is below the lower trigger level. This is an indicator that new data can be written to the controller. If the DMA mode is enabled then a DMA request to transmit new data will be sent.
6	R	Transmitter underrun. The transmitter wants to send more data but no data is available in the FIFO. The controller will transmit a break. This bit is cleared upon reading from the register.
7	R	Controller Busy. This bit is set while the transmitter is busy transmitting or receiving data. It is clear when the controller is idle or transmits a Serial infrared Interaction Pulse (SIP) and the transmit FIFO is empty.

4.2.4 FIFO Control Register

This register allows setting the trigger levels of FIFO and allows clearing them. When reading from bits that are write only a '0' is placed in them.

Bit #	Access	Description
1:0	R/W	Set receiver FIFO trigger level (Number of words in FIFO that will set bit 0 in Status register). '00' – 8 words '01' – 10 words '10' – 12 words '11' – 14 words
2	W	Clear Receiver FIFO. Write '1' to this bit to clear receiver FIFO.
3	W	Reserved
5:4	R/W	Set transmitter FIFO trigger level – number of words in FIFO that an equal or smaller amount of words in FIFO will set bit 5 of the status register and request an interrupt and a DMA transfer. '00' – 2 words '01' – 4 words '10' – 6 words '11' – 8 words
6	W	Clear Transmitter FIFO. Write '1' to clear the FIFO. This will result in aborted frame and transmitting a break.
7	R/W	End of frame. Write to this bit to change behavior on transmitter FIFO underrun condition. '0' – The transmitter FIFO underrun will result in aborted frame and an interrupt will be raised if it is enabled. '1' – The FIFO underrun will result in normal termination of outgoing frame, i.e. the calculated CRC will be sent, followed by the frame stop sequence. The interrupt will be generated in this case, too, if enabled. Set this bit to '1' just before sending the last data to the controller if you don't use Count Outgoing Data mode. Reset this bit in response to FIFO underrun interrupt or when sending next frame.

Reset: 00110011b

4.2.5 Line Control Register

The Line Control register controls setting the break condition and the End of Frame logic.

When break is enabled, the output of the controller is forced into break (no signal) but all other logic of the controller works as usual.

Bit #	Access	Description
0	R/W	Force break. '0' – transmission is enabled '1' – transmission is disabled. The output pin is forced to break state (zero) regardless of what the transmitter is doing.
1	R/W	Count Outgoing Data mode select When enabled, the controller will count the bytes being transmitted in each frame and compare it to the number stored in Outgoing Frame Data Length register. When the count will have reached the designated number the controller will end the frame in normal fashion. Look at the OFDL register for more information. When this mode is disabled, the controller will know when to end the frame by using bit 7 of FIFO Control register. See bit 7 in FCR for more information on this mode of operation. '0' – Count Outgoing Data mode disabled '1' – Count Outgoing Data mode enabled
7:2	R/W	Reserved

4.2.6 Outgoing Frame Data Length Register (OFDL)

Set this 16-bit register to the length in bytes of the outgoing frame before sending next frame. The length of the frame is calculated on the information field only (address, control and data fields only) without the CRC and flags. This register is used when operating in Count Outgoing Data mode. When in this mode, the amount of data transferred to the controller is counted and when the count is reached the controller finishes sending the frame in normal fashion by transmitting CRC field, STO flag and then the SIP. The counter then resets. Writing to this register also resets the counter, so only write to it before starting transmitting new frame.

Bit #	Access	Description
15:0	R/W	Length of outgoing frame

4.2.7 Incoming Frame Data Length Register (IFDL)

This is a read only 16-bit wide register that reflects the length of the frame currently being received. At the end of frame reception when the Received End of Frame interrupt occurs, this register reflects the length of the information field received in that frame, not counting the CRC field and other flags. The register resets its count on the start of next frame reception, when a new STA field has been detected. It usually better to read this register in response to the Received End of Frame interrupt. At that time the register will reflect the final size of the frame and will allow the driver to find a way to handle receiving the last of the frame's bytes.

Bit #	Access	Description
15:0	R	Length of the frame being received

4.2.8 Clock Divisor Register

Use this register to define the clock for the MIR and FIR modes. In MIR mode the clock at the output should be 4 x 1.152MHz = 4.608 MHz. In FIR mode, the clock should be a multiple of 8Mhz in the range 40Mhz to 96Mhz.

Bit #	Access	Description
9:0	R/W	Base Count (BC). The base number by which the clock should be divided. This loaded first into the internal counter. Range is 1 to 1024.
16:10	R/W	Base Count Iterations (BCI). This number defines the number of times that the Base Count pulses are counted before going into Secondary Count. Range is 1 to 128.
18:17	R/W	Secondary Behavior (SB). '00' – The clock is always divided by the Base Count. After the BC is reached and enable is generated, the internal counter is reset to the base count. '01' – After BCI of BC were performed, the internal counter is loaded with a value of BC-1. This count is performed once and then everything starts from the beginning. '10' – After BCI of BC were performed, the internal counter is loaded with a value of BC+1. This count is performed once and then everything starts from the beginning. '11' – Illegal value.
31-19	R/W	Reserved.

The clock is generated in the following way:

```
Do forever:
      For (Base Count Iterations) do
            Load Internal Counter (IC) with Base Count (BC)
            Wait until IC reaches zero  (count BC clocks)
            Assert Enable pulse
      End For
      Case Secondary Behavior
            '00' : break (go to start)
            '01' : Load IC with BC-1
            '02' : Load IC with BC+1
      End Case
      Wait until IC reaches zero  (count BC clocks)
      Assert Enable pulse
End Do
```

5

Operation

5.1 Reset defaults

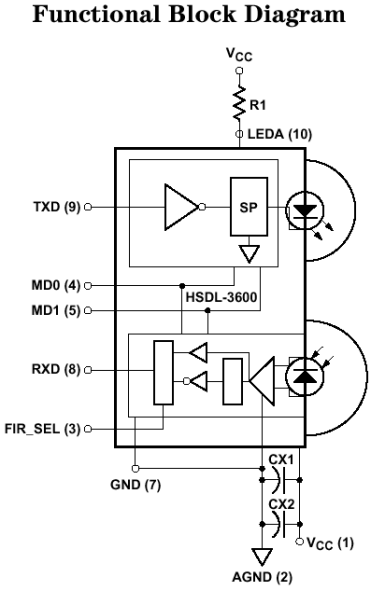
Upon receiving the [RST_I] signal the core will reset itself to the SIR mode. But the UART will not be initialized in a defined way. The receiver will be disabled, the core will be set to transmit mode. All FIFO buffers will be emptied. All WISHBONE signals cleared.
The core should then be programmed to the desired state using the control registers.

5.2 IR protocol

The IR protocol is somewhat complex and is too big to describe in this document, mostly because it is defined differently for the three modulation modes.
Please refer to the following references for information about the IR protocol:

- Infrared Data Association Serial infrared Physical Layer Specifications, version 1.3, Oct 1998: Section 5.
- Infrared Data Association Serial infrared Link Access Protocol (IrLAP), version 1.1, June 1996: Section 10 (Appendix D)

5.3 Interfacing with the HP HSDL-3600 transceiver (example)



The HP HSDL-3600 transceiver has 5 pins responsible for its control and communication. These can be seen on the left side of the included block diagram. The TXD (9) receives the digital data to be transmitted. The RXD (8) reflects the data received from the photo-diode. FIR_SEL (3) is responsible for selection of receiver speed between SIR (slow IR, up to 115.2Khz) and MIR/FIR (up to 4Mbit). The MD0 (4) and MD1 (5) pins control the state of the transceiver. The transceiver can be set up to transmit in three different power levels (full, 2/3, 1/3). If we choose operating at maximum output power than MD0 and MD1 should both be '0'. In this mode when MD0 is changed to '1', the device enters power saving mode. So, we'll connect MD1 to ground on the PCB and the MD0 with FIR_SEL pins will be controlled by GPIO pins, for example.

5.4 Using the core

Until the core is enabled, only the Master Control Register (MCR) is accessible.

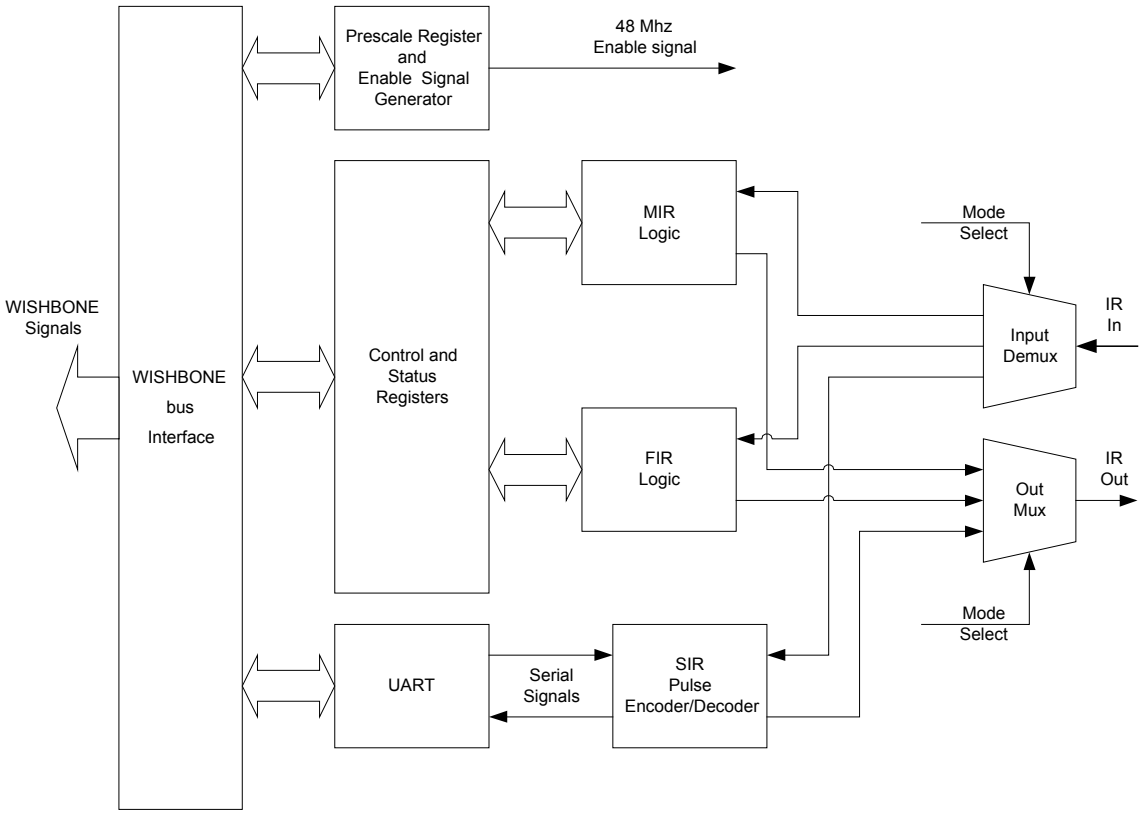
1. Determine if the IR transceiver uses positive logic (like HP HSDL-3600) or complemented logic.
2. Determine the mode in which you wish to work. Usually, before any connection is established, the IR communication is set to the default settings of 9600 bps, 8 data bits, No parity, 1 stop bit.
3. Determine if you wish to use DMA for transfers. DMA usage is extremely recommended for MIR and FIR communication and is optional in SIR mode.
4. Write the setting to the MCR enabling the controller.
5. Based on the mode of operation perform the subsequent initialization
6. In SIR mode (UART):
   - 6.1. Set the Line Control Register to 10000011b setting the communication parameters and allowing access to the Divisor Latches.
   - 6.2. Write the desired value into the 4 Divisor Latch bytes to create desired baud rate
   - 6.3. Set the Line Control Register to 00000011b to return access to normal registers.
   - 6.4. Define the FIFO trigger level in FIFO Control register.
   - 6.5. Set the interrupts you want to enable in Interrupt Enable register. Consider interrupt usage versus DMA operation.
7. In MIR/FIR mode:
   - 7.1. Based on current mode set the Clock Divisor Register to the desired settings.
   - 7.2. Define interrupts in Interrupt Enable Register.
   - 7.3. Set the FIFO Control Register. Pay attention to bit 7.
   - 7.4. Set bit 1 in Line Control Register to the desired mode of end of frame operation.

You can now begin sending data, if in transmit mode. In MIR and FIR modes pay attention to the way you wish to define the end of frame. If you use frame length, make sure to preprogram the Outgoing Frame Data Length register before starting new frame. If you use FIFO underrun control don't forget to change the corresponding bit in FIFO control register before the end of frame is transmitted.

6

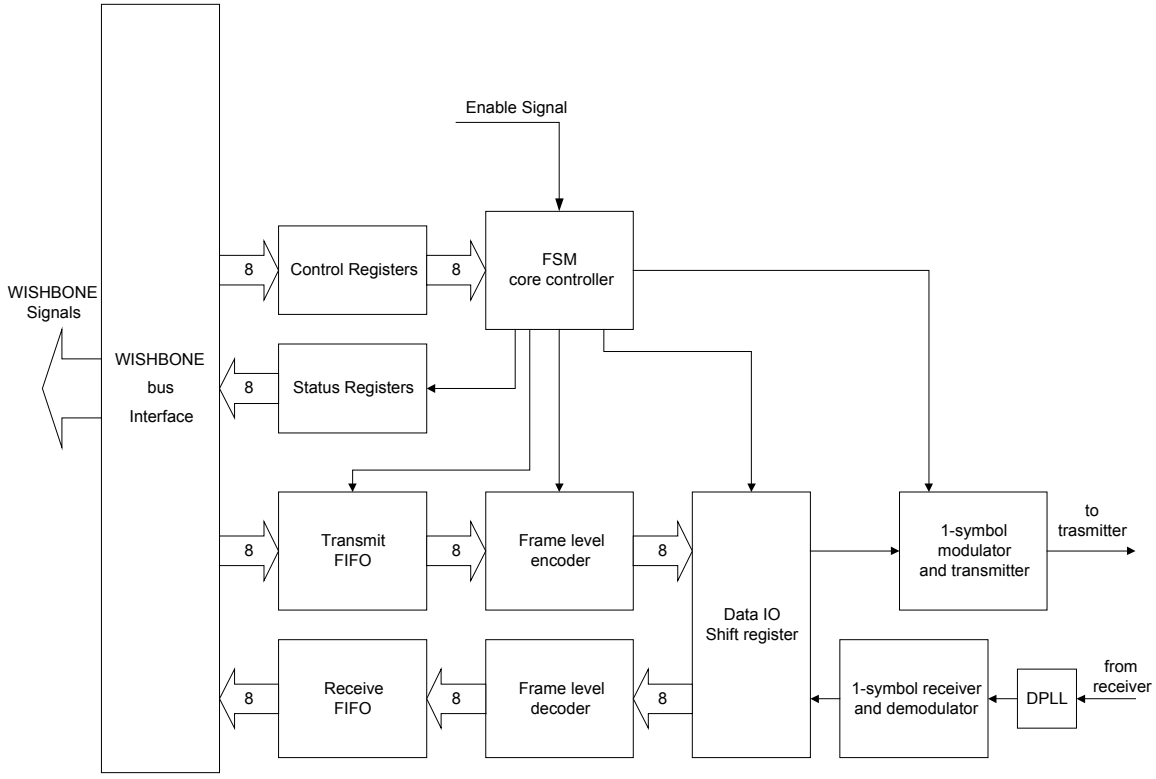
Architecture

Top Level Block Diagram



The core can operate in 3 different encodings and so it has division between them in its structure. The SIR (Serial infrared) encoding operates by using a standard UART as its controller. The MIR and FIR modes have their own control blocks. The output of the 3 blocks is multiplexed based on the current operating mode before leaving the core and the input signal in demultiplexed in a similar way.

The following diagram shows the architecture for one mode (MIR or FIR).



The enable signal is derived from the input clock, the pre-scale register and additional logic that creates the signal in required frequency for the current mode.

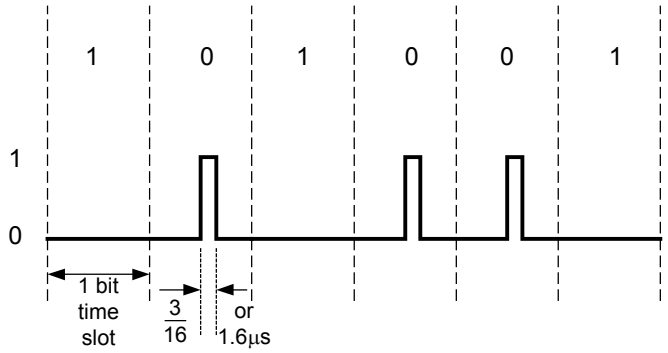
The Frame Level Encoder calculates CRC for the sent data, performs bit stuffing in MIR mode, creates start and stop sequences and sends data down the line to the Data Shift Register.

The Frame Level Decoder calculates the CRC on incoming data, performs bit de-stuffing in MIR, compares the calculated CRC to the received one and reports any errors detected in the process.

The 1-symbol modulator creates the signal to be sent to the IR transceiver bit by bit as received from the UART in SIR, Data IO Shift Register in MIR and 2-bit signals in FIR mode.

The signal generated in SIR is as follows:
On logic ‘1’ the LED is off.
On logic ‘0’ a pulse is created starting the center of the bit time and lasting 3/16 of bit time period or 1.6µs (3/16 bit times at 115.2 kbps) depending on the current settings.

The following figure displays the output for the input 101001 (in sending order) in SIR encoding:



In MIR mode, the encoding is similar but the pulse is ¼ of the bit time.
In FIR mode the encoding is somewhat more complex as it transfers 2 bits per pulse.
Refer to IrDA physical level specification for further information.