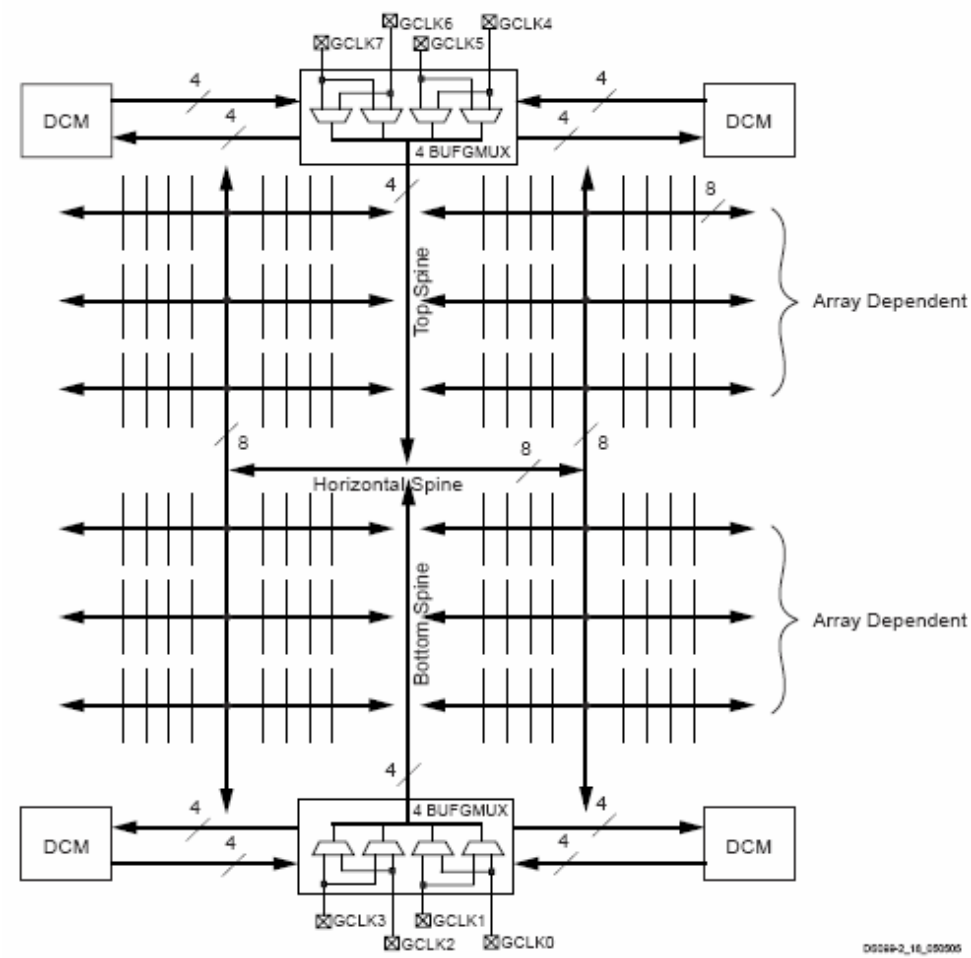
EE3810 – Lecture 23

Advanced Features of Xilinx FPGAs

FPGA Clock Distribution

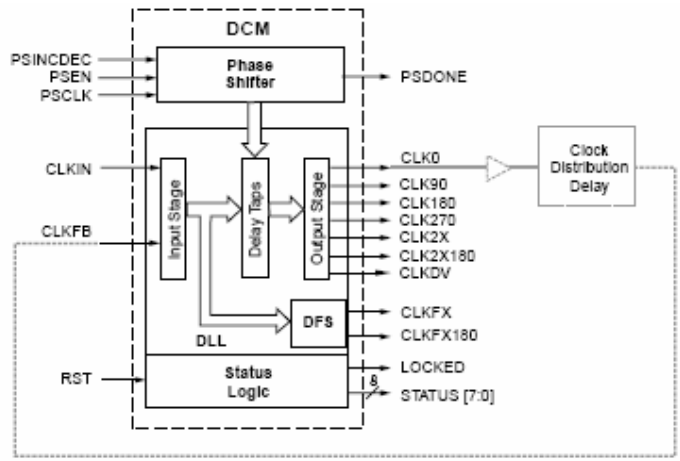


Digital Clock Manager

- The Spartan 3 has 8 internal global clock buses, and 4 Digital Clock Managers.
- The Digital Clock Managers allow:
  - multiplying or dividing an external clock
  - eliminating clock skew
  - phase shifting

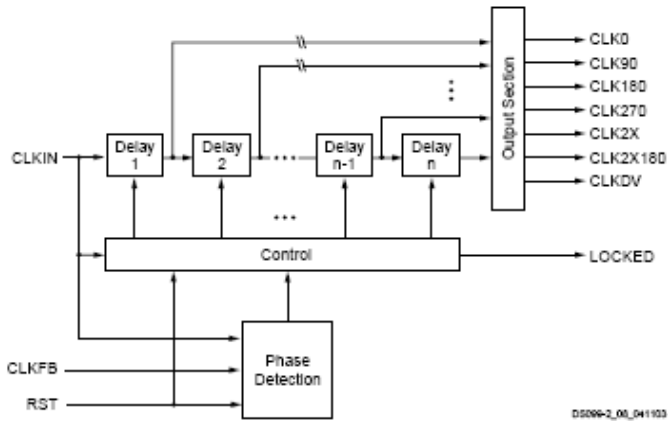
The DCM Has Four Main Blocks

- Delay Lock Loop
  - uses feedback to deskew clock.
- Digital Freq Synth
  - Generates clocks
- Phase Shifter
  - Adjusts phase relationships of output clocks
- Status Logic



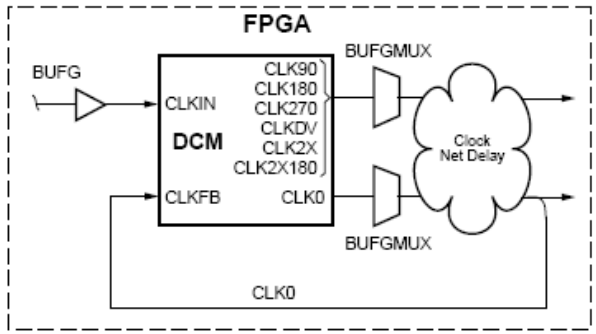
Delay Locked Loop

- CLKIN is used as a reference signal.
- CLKFB is a feedback signal from the end of the clock distribution network.
- Clock skew is compensated by correcting phase differences.

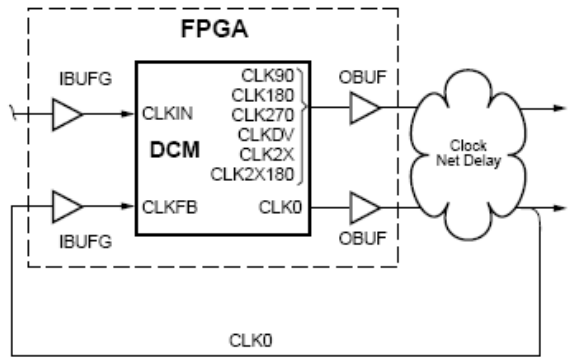


Example Clock Feedback

- CLK0 (or CLK2X) is used as a reference signal.
- A correction is applied to the other clocks.
- The clock netwotk may extend off-chip.

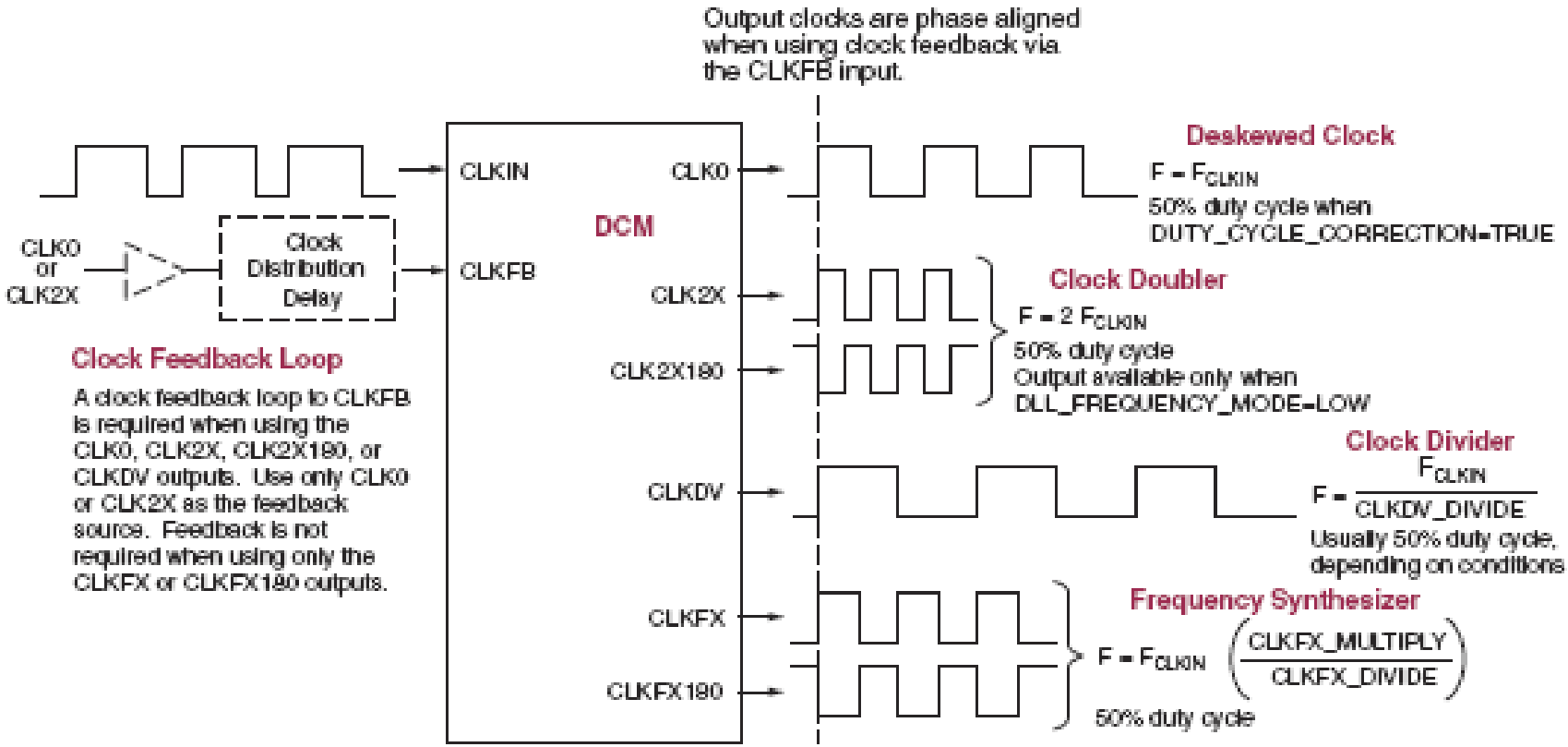


(a) On-Chip with CLK0 Feedback



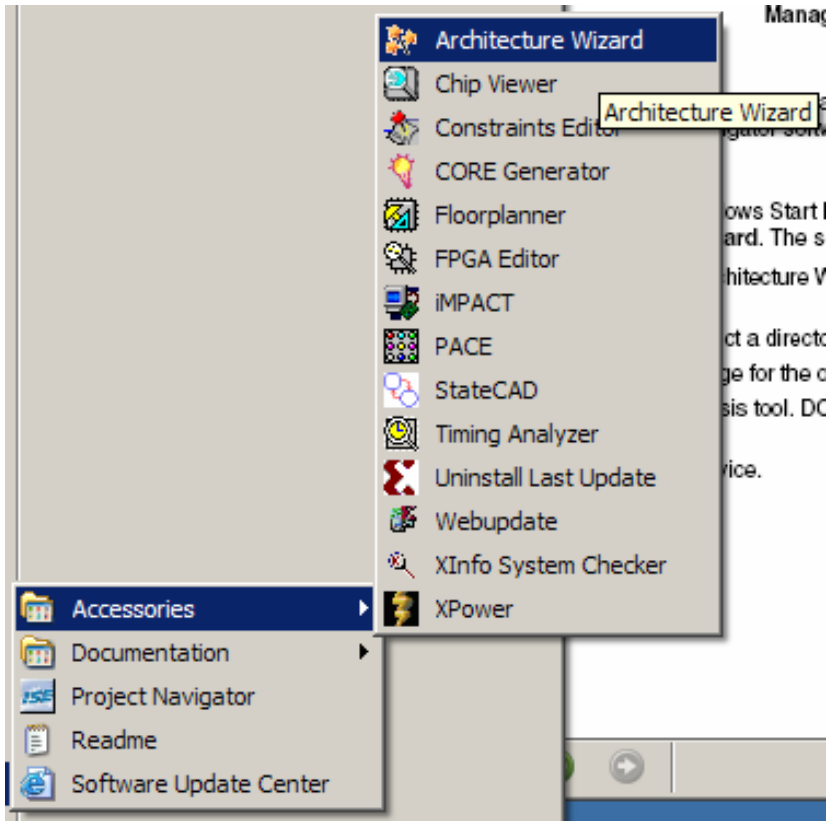
(c) Off-Chip with CLK0 Feedback

Digital Frequency Synthesizer



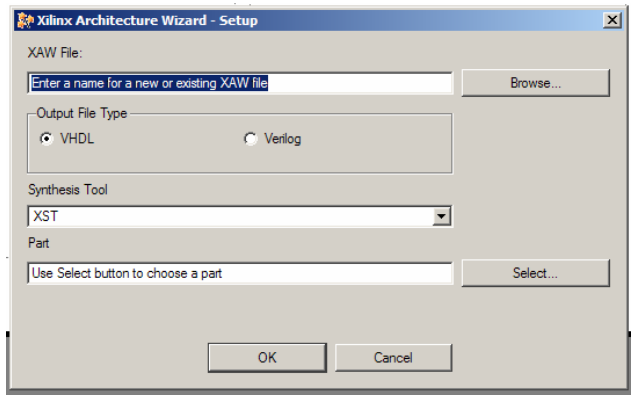
Xilinx Architecture Wizard

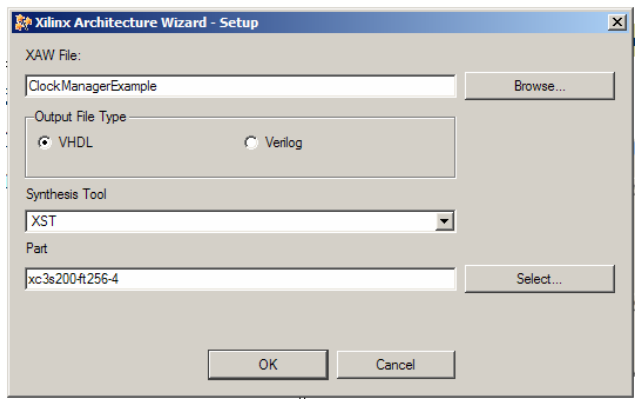
- From the start menue for ISE, go to “Accessories” and pick “Architecture Wizard”
- Note that there are several other tools available as well.



Architecture Wizard

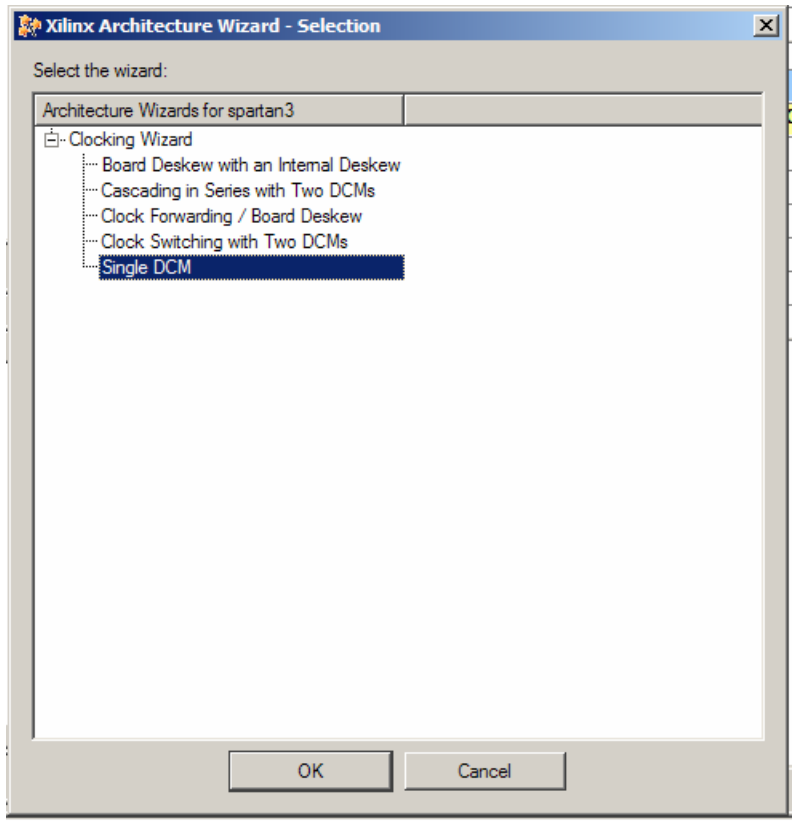
- The initial screen prompts for a file name.
- Enter a file name and select the part type you're targeting.





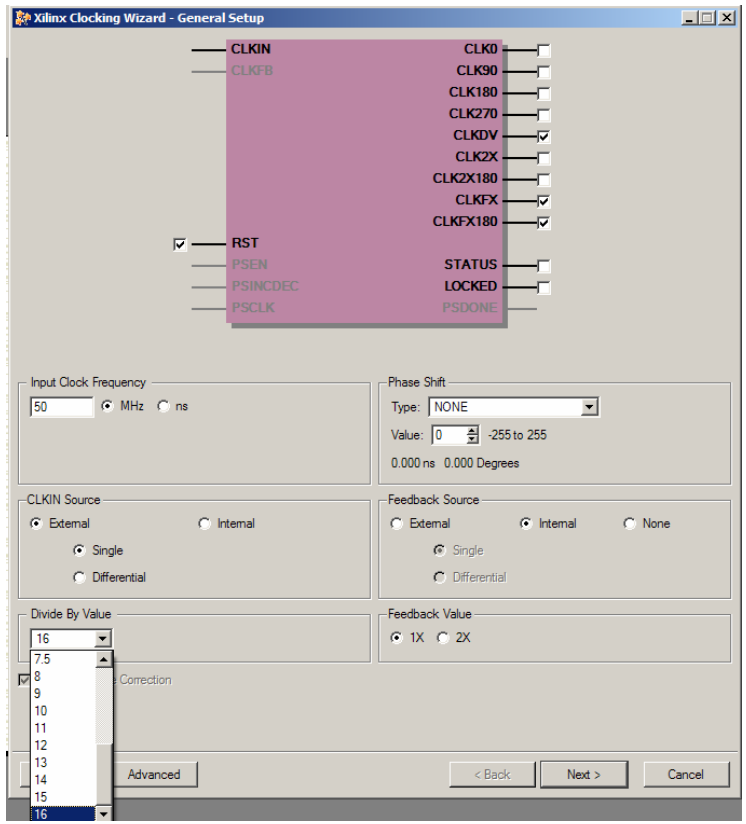
Creating a Single DCM

- For this example, we'll invoke a single DCM for our design.
- Select the appropriate configuration in the Wizard.



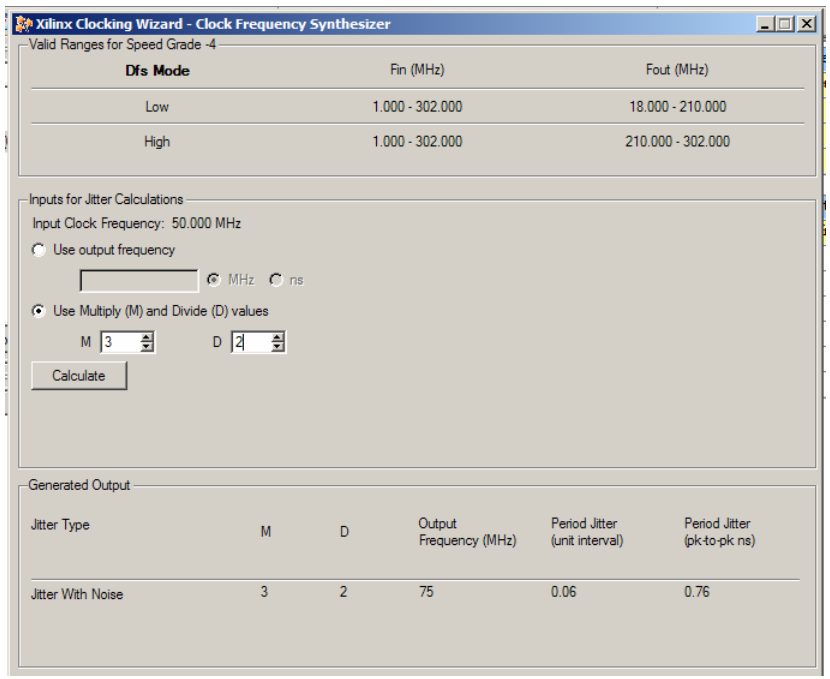
Options in Wizard

- In this example we'll enable the DFS to provide a divide by 16 clock and we'll use both clock multiplier phases.



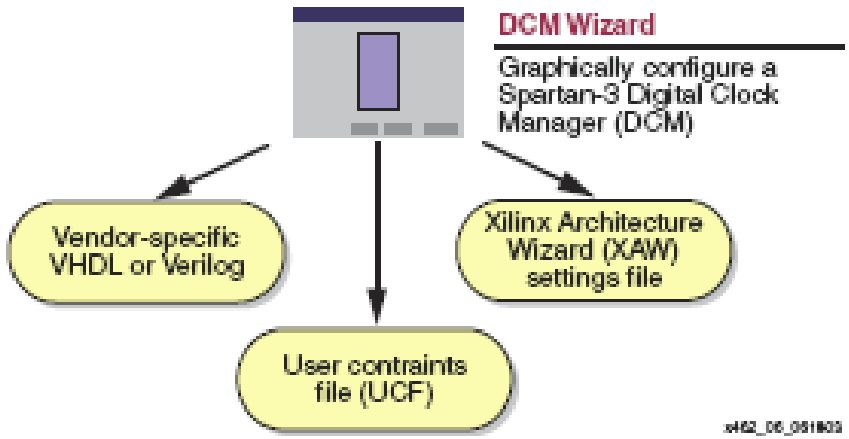
Multipliers and Dividers

- To generate a clock, the input may be
  - multiplied by 1-32
  - divided by 1-32
- For this example I want to create a 75 MHz clock from a 50MHz clock.



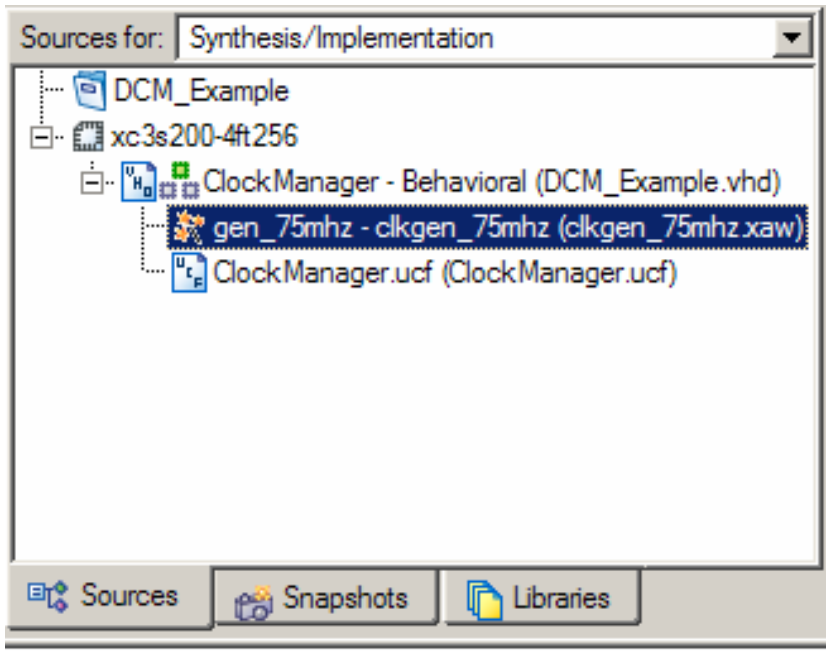
Wizard Output Files

- The Wizard creates three files:
  - .vhd – contains the component definitions for the clock manager.
  - .xaw – contains architecture wizard settings
  - .ucf – user constraints file.



Add the .XAW File

- Adding the .xaw file to the design is done through the “add source” menu.
- The .xaw file can also be created from within project manager.



VHDL Source

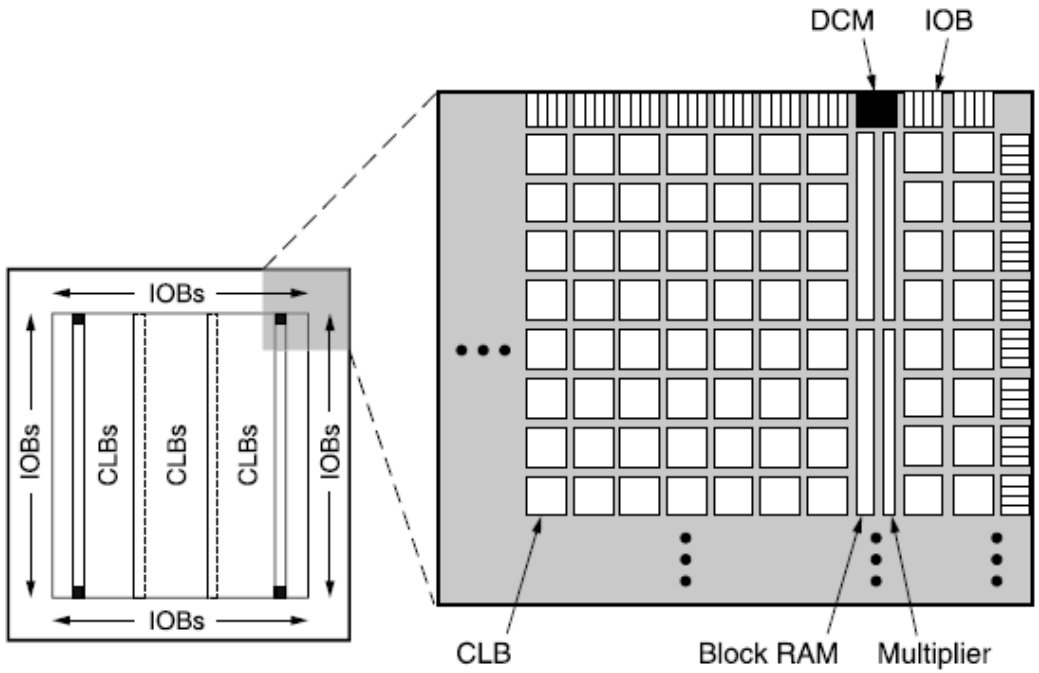
```
entity ClockManager is
    Port ( clk_50mhz     : in  std_logic;
           clk_75mhz     : out  std_logic;
           clk_75mhz_180 : out std_logic);
end ClockManager;

architecture Behavioral of ClockManager is
   component clkgen_75mhz
   port ( CLKIN_IN        : in    std_logic;
          RST_IN          : in    std_logic;
          CLKFX_OUT       : out   std_logic;
          CLKFX180_OUT    : out   std_logic;
          CLKIN_IBUFG_OUT : out   std_logic;
          LOCKED_OUT      : out   std_logic );
          end component;
begin
   gen_75mhz: clkgen_75mhz
   port map( CLKIN_IN        => clk_50mhz,
             RST_IN          => '0',
             CLKFX_OUT       => clk_75mhz,
             CLKFX180_OUT    => clk_75mhz_180,
             CLKIN_IBUFG_OUT => open,
             LOCKED_OUT      => open );
end Behavioral;
```

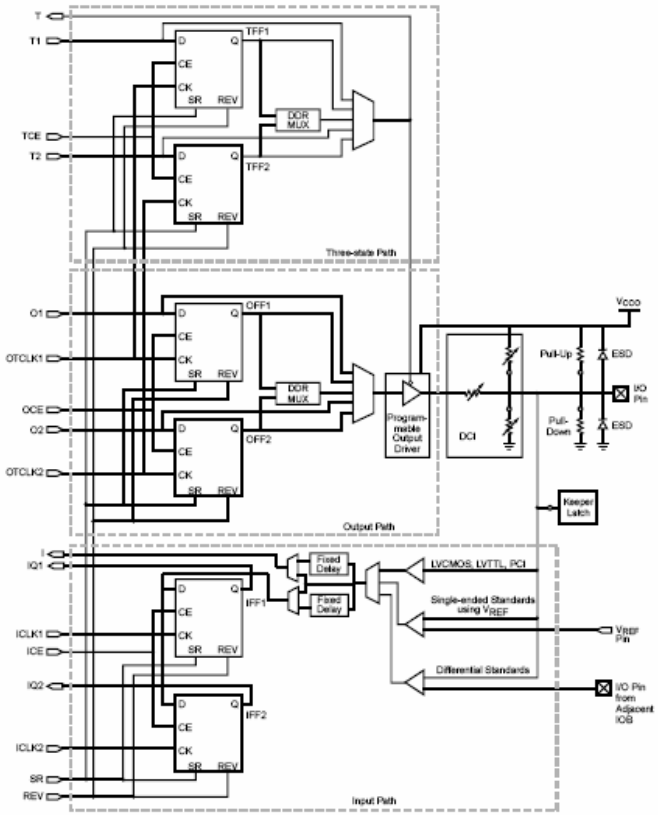
DCM Output


Tek Stop
Ch3 Freq
75.02MHz
Ch2 2.00 V M 20.0ns A Ch3 3.40 V
Ch3 2.00 V
24 Apr 2006

Xilinx FPGA Organization



IO Buffer Details



Example IO Buffer Configurations

Table 7: **Single-Ended I/O Standards (Values in Volts)**

Signal Standard (IOSTANDARD)	V_{CCO} For Outputs	V_{CCO} For Inputs	V_{REF} for Inputs[1]	Board Termination Voltage (V_{TT})
GTL	Note 2	Note 2	0.8	1.2
GTLP	Note 2	Note 2	1	1.5
HSTL_I	1.5	-	0.75	0.75
HSTL_III	1.5	-	0.9	1.5
HSTL_I_18	1.8	-	0.9	0.9
HSTL_II_18	1.8	-	0.9	0.9
HSTL_III_18	1.8	-	1.1	1.8
LVCMOS12	1.2	1.2	-	-
LVCMOS15	1.5	1.5	-	-
LVCMOS18	1.8	1.8	-	-
LVCMOS25	2.5	2.5	-	-
LVCMOS33	3.3	3.3	-	-
LVTTL	3.3	3.3	-	-
PCI33_3	3.0	3.0	-	-
SSTL18_I	1.8	-	0.9	0.9
SSTL18_II	1.8	-	0.9	0.9
SSTL2_I	2.5	-	1.25	1.25
SSTL2_II	2.5	-	1.25	1.25

Table 8: **Differential I/O Standards**

Signal Standard (IOSTANDARD)	V_{CCO} (Volts) For Outputs	V_{CCO} (Volts) For Inputs	V_{REF} for Inputs (Volts)
LDT_25 (ULVDS_25)	2.5	-	-
LVDS_25	2.5	-	-
BLVDS_25	2.5	-	-
LVDSEXT_25	2.5	-	-
LVPECL_25	2.5	-	-
RSDS_25	2.5	-	-
DIFF_HSTL_II_18	1.8	-	-
DIFF_SSTL2_II	2.5	-	-

Logic Block Organization

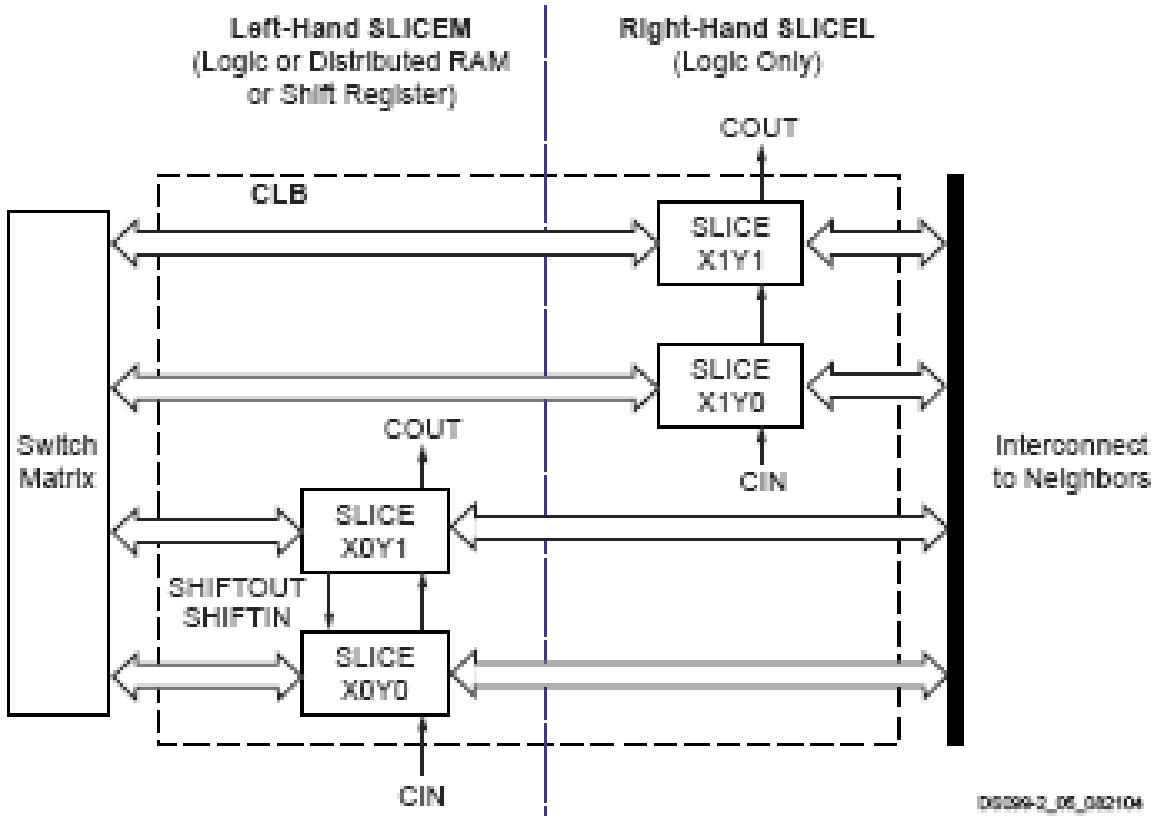
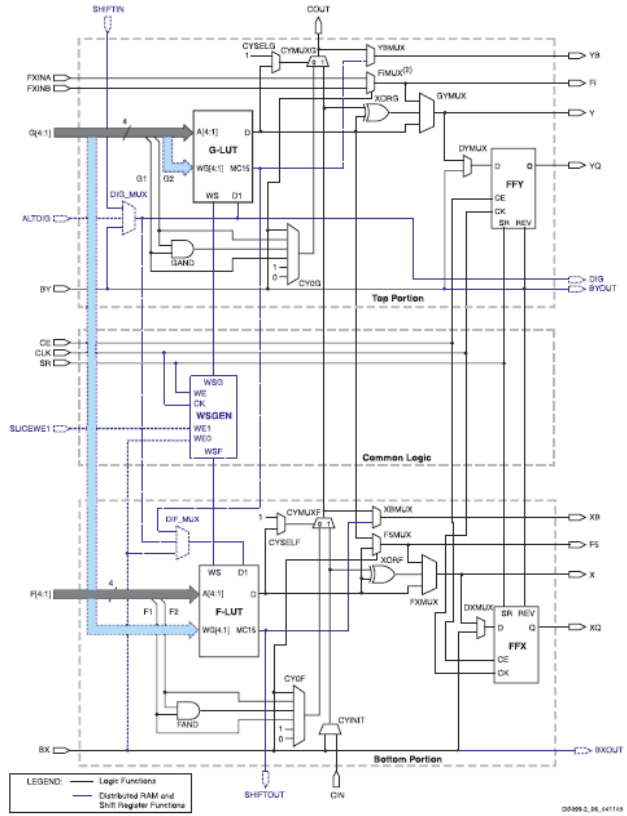
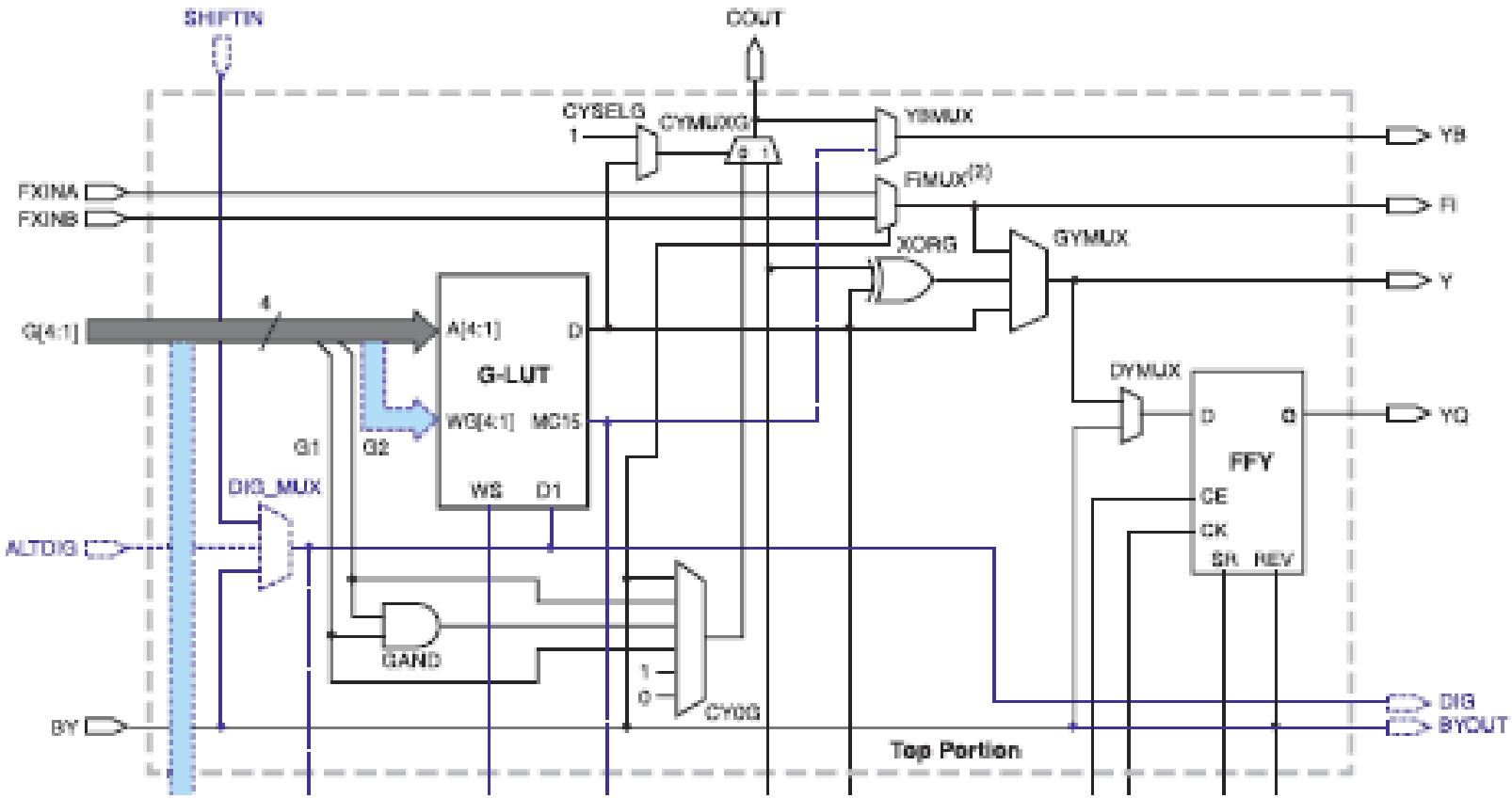


Figure 9: **Arrangement of Slices within the CLB**

Inside a Logic Block



Logic Block Closeup



FPGA Configuration