EE3810 – Lecture 23

Advanced Features of Xilinx FPGAs

FPGA Clock Distribution



Digital Clock Manager

- The Spartan 3 has 8 internal global clock buses, and 4 Digital Clock Managers.
- The Digital Clock Managers allow:
 - multiplying or dividing an external clock
 - eliminating clock skew
 - phase shifting

The DCM Has Four Main Blocks

- Delay Lock Loop
 - uses feedback to deskew clock.
- Digital Freq Synth
 - Generates clocks
- Phase Shifter
 - Adjusts phase relationships of output clocks
- Status Logic



Delay Locked Loop

- CLKIN is used as a reference signal.
- CLKFB is a feedback signal from the end of the clock distribution network.
- Clock skew is compensated by correcting phase differences.



Example Clock Feedback

- CLK0 (or CLK2X) is used as a reference signal.
- A correction is applied to the other clocks.
- The clock network may extend off-chip.



⁽c) Off-Chip with CLK0 Feedback

Digital Frequency Synthesizer



Xilinx Architecture Wizard

- From the start menue for ISE, go to "Accessories" and pick "Architecture Wizard"
- Note that there are several other tools available as well.



Architecture Wizard

- The initial screen prompts for a file name.
- Enter a file name and select the part type you're targeting.

💱 Xilinx Architecture Wiza	rd - Setup	×
XAW File:		
Enter a name for a new or exi	Browse	
Output File Type		
VHDL	C Verilog	
Synthesis Tool XST		
Part		_
Use Select button to choose	part	Select
	OK Cancel	

🔅 Xilinx Architecture Wiza	rd - Setup		×
XAW File:			
Clock ManagerExample			Browse
Output File Type			
 VHDL 	C Verilog		
Synthesis Tool			
XST		•	
Part			
xc3s200-ft256-4			Select
		-	
	ОК	Cancel	

Creating a Single DCM

- For this example, we'll invoke a single DCM for our design.
- Select the appropriate configuration in the Wizard.

Xilinx Architecture Wizard - Selection	×
Select the wizard:	
Architecture Wizards for spartan3	
⊡ Clocking Wizard Board Deskew with an Internal Deskew Cascading in Series with Two DCMs Clock Forwarding / Board Deskew Clock Switching with Two DCMs Single DCM	
ок	Cancel

Options in Wizard

 In this example we'll enable the DFS to provide a divide by 16 clock and we'll use both clock multiplier phases.

Anno-clocking Wizere acticital Scorp	
	CLKO ——
CLKFB	CLK90
	CLK180
	CLKFX180
RST	
PSEN	STATUS
PSINCDEC	LOCKED
PSCLK	PSDONE
Input Clock Frequency	Phase Shift
50 • MHz C ns	Type: NONE
	Value: 0 🚖 -255 to 255
	0.000 ns 0.000 Degrees
CLKIN Source	Feedback Source
© External C Internal	C External C None
 Single 	Single
 Single Differential 	 Gingle Cifferential
Single Differential Divide By Value	G Single C Differential Feedback Value
Single Differential Divide By Value	G Single C Differential Feedback Value C 1X C 2X
Single Differential Divide By Value 16 X 7.5	G Single O Differential Feedback Value G 1X C 2X
Single Differential Divide By Value 16 2 Correction Correction	G Single O Differential Feedback Value C 1X C 2X
Single Differential Divide By Value 16	G Single C Differential Feedback Value G 1X C 2X
Single Differential Divide By Value	© Single © Differential © TX © 2X
Single Differential Divide By Value	© Single © Differential © 1X © 2X

Multipliers and Dividers

- To generate a clock, the input may be
 - multiplied by 1-32
 - divided by 1-32
- For this example I want to create a 75 MHz clock from a 50MHz clock.

🏶 Xilinx Clocking Wizard - Clock Freq	uency Synt	hesizer				_ 🗆 🗙
-Valid Ranges for Speed Grade -4						
Dfs Mode		Fin	[MHz)	Fout (MHz)		
Low		1.000 - 302.000 18.000 - 210.000		000 - 210.000		
High		1.000 - 302.000		210.000 - 302.000		
Inputs for Jitter Calculations Input Clock Frequency: 50.000 MHz C Use output frequency C Use Multiply (M) and Divide (D) value M 3 1 D 2 Calculate	C ns s					
-Generated Output						
Jitter Type	м і	D	Output Frequency (MHz)	Period Jitter (unit interval)	Period Jitter (pk-to-pk ns)	
Jitter With Noise	3 :	2	75	0.06	0.76	
	Alinix Clocking Wizard - Clock Freq -Valid Ranges for Speed Grade -4 Dfs Mode Low High -Inputs for Jitter Calculations Input Clock Frequency: 50.000 MHz (*) Use output frequency (*) Use output frequency (*) Use Multiply (M) and Divide (D) value M 3 2 D 2 Calculate -Generated Output Jitter Type Jitter With Noise		Wilnix Clocking Wizard - Clock Frequency Synthesizer -Vaild Ranges for Speed Grade -4 Dfs Mode Fin I Low 1.000 - High 1.000 - -Inputs for Jitter Calculations Input Clock Frequency: 50.000 MHz C Use output frequency Image: C ris Image: C Use Multiply (M) and Divide (D) values M 3 2 D 2 2 Calculate Calculate	Stinux Clocking Wizard - Clock Frequency Synthesizer -Valid Ranges for Speed Grade -4 Dfs Mode Fin (MHz) Low 1.000 - 302.000 High 1.000 - 302.000 -Inputs for Jiter Calculations	Sylinix Clocking Wizard - Clock Frequency Synthesizer -Valid Ranges for Speed Grade -4 Dfs Mode Fin (MHz) Low 1.000 - 302.000 High 1.000 - 302.000 -Inputs for Jiter Calculations Input Clock Frequency: 50.000 MHz C Use output frequency: G Use Multiply (M) and Divide (D) values M 3 Calculate	Syllinix Clocking Wizard - Clock Frequency Synthesizer Valid Ranges for Speed Grade -4 Dfs Mode Fin (MHz) Fout (MHz) Low 1.000 - 302.000 18.000 - 210.000 High 1.000 - 302.000 210.000 - 302.000 Inputs for Jitter Calculations Input Clock Frequency: 50.000 MHz Imput Clock Frequency: 50.000 MHz C Use output frequency Imput Clock Frequency Imput Clock Frequency C Use Multiply (M) and Divide (D) values Imput Clock Frequency Imput Clock Instructions M 3 Imput Clock Imput Clock Instructions Imput Clock Instructions Generated Output Imput Clock Instructions Imput Clock Instructions Imput Clock Instructions Jitter Type M D Output Frequency (MHz) Period Jitter (pkto-pk ns) Jitter With Noise 3 2 75 0.06 0.76

Wizard Output Files

- The Wizard creates three files:
 - .vhd contains the component definitions for the clock manager.
 - .xaw contains architecture wizard settings
 - .ucf user constraints file.



Add the .XAW File

- Adding the .xaw file to the design is done through the "add source" menu.
- The .xaw file can also be created from within project manager.



VHDL Source

```
entity ClockManager is
    Port ( clk_50mhz : in std_logic;
        clk_75mhz : out std_logic;
        clk_75mhz_180 : out std_logic);
end ClockManager;
```

```
architecture Behavioral of ClockManager is
  component clkgen 75mhz
  port ( CLKIN IN
                         : in
                                std logic;
                         : in
                                std_logic;
         RST_IN
         CLKFX OUT
                         : out std_logic;
         CLKFX180 OUT : out std logic;
         CLKIN_IBUFG_OUT : out std_logic;
         LOCKED OUT
                                std_logic );
                         : out
         end component;
begin
  gen_75mhz: clkgen_75mhz
  port map( CLKIN IN
                            => clk 50mhz,
                           => '0',
            RST IN
                          => clk_75mhz,
            CLKFX_OUT
                           => clk_75mhz_180,
            CLKFX180_OUT
            CLKIN_IBUFG_OUT => open,
            LOCKED OUT
                            => open );
end Behavioral;
```

DCM Output



Xilinx FPGA Organization



IO Buffer Details



Example IO Buffer Configurations

Table 7: Single-Ended I/O Standards (Values in Volts)

Vcco		0		Board
Signal Standard (IOSTANDARD)	For Outputs	For Inputs	V _{REF} for Inputs ⁽¹⁾	Voltage (Vπ)
GTL	Note 2	Note 2	0.8	1.2
GTLP	Note 2	Note 2	1	1.5
HSTL_I	1.5	-	0.75	0.75
HSTL_III	1.5	-	0.9	1.5
HSTL_I_18	1.8	•	0.9	0.9
HSTL_II_18	1.8	-	0.9	0.9
HSTL_III_18	1.8		1.1	1.8
LVCMOS12	1.2	1.2	-	-
LVCMOS15	1.5	1.5	-	-
LVCMOS18	1.8	1.8	-	-
LVCMOS25	2.5	2.5	-	-
LVCMOS33	3.3	3.3	-	-
LVTTL	3.3	3.3	-	-
PCI33_3	3.0	3.0	-	-
SSTL18_I	1.8	-	0.9	0.9
SSTL18_II	1.8	-	0.9	0.9
SSTL2_I	2.5	-	1.25	1.25
SSTL2_II	2.5	-	1.25	1.25

Table 8: Differential I/O Standards

	V _{CCO} (Volts)		V _{REF} for	
Signal Standard (IOSTANDARD)	For Outputs	For Inputs	Inputs (Volts)	
LDT_25 (ULVDS_25)	2.5	-	-	
LVDS_25	2.5	-	-	
BLVDS_25	2.5	-	-	
LVDSEXT_25	2.5	-		
LVPECL_25	2.5	-	-	
RSDS_25	2.5	-	-	
DIFF_HSTL_II_18	1.8	-	-	
DIFF_SSTL2_II	2.5	-	-	

Logic Block Organization



Figure 9: Arrangement of Slices within the CLB

Inside a Logic Block



Logic Block Closeup



FPGA Configuration

