LPFFIR FPGA Characterization

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Revision History

Rev.	Date	Author	Description
1.0	03/25/19	Vladimir Armstrong	First Draft

Contents

1

Introduction

The LPFFIR [1] FPGA implementation Device Under Test (DUT) is characterized by magnitude and phase response. The magnitude and phase measurement results [4] is obtained by running scripts [Appendix A] on measurement equipment setup [2]. The magnitude and phase measurement results analysis [5] is done by comparing expected behavior [3] versus measurement results [4].

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Measurement Equipment

The Measurement Equipment consist of PC, Mixed Signal Oscilloscope [5], FPGA prototyping board [2] , ADC [3] and DAC [4] peripheral modules. The Waveform Generator is connected to ADC peripheral module and Oscilloscope channel 1 (CH1). The Oscilloscope channel 2 (CH2) is connected to DAC peripheral module as shown below.

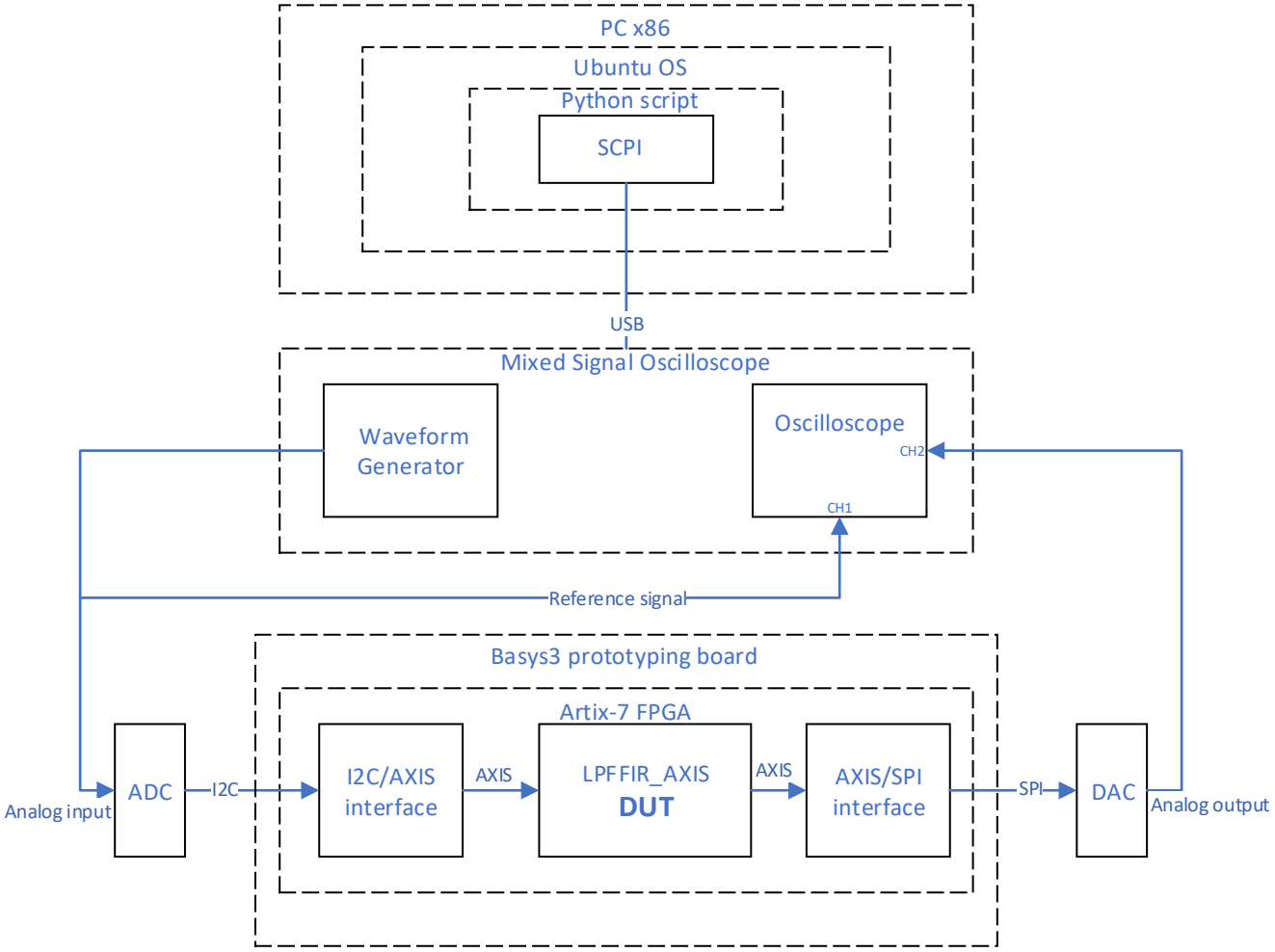

Figure 1 Measurement equipment block diagram

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Expected Behavior

Expected Magnitude Response Equation

$$\left|H\left(z=e^{i\omega}\right)\right| = 2\left|\cos\frac{5}{2}\omega + \cos\frac{3}{2}\omega + \cos\frac{1}{2}\omega)\right|$$

Expected Phase Response Equation

$$\measuredangle H\left(z=e^{i\omega}\right) = -\frac{5}{2}\omega$$

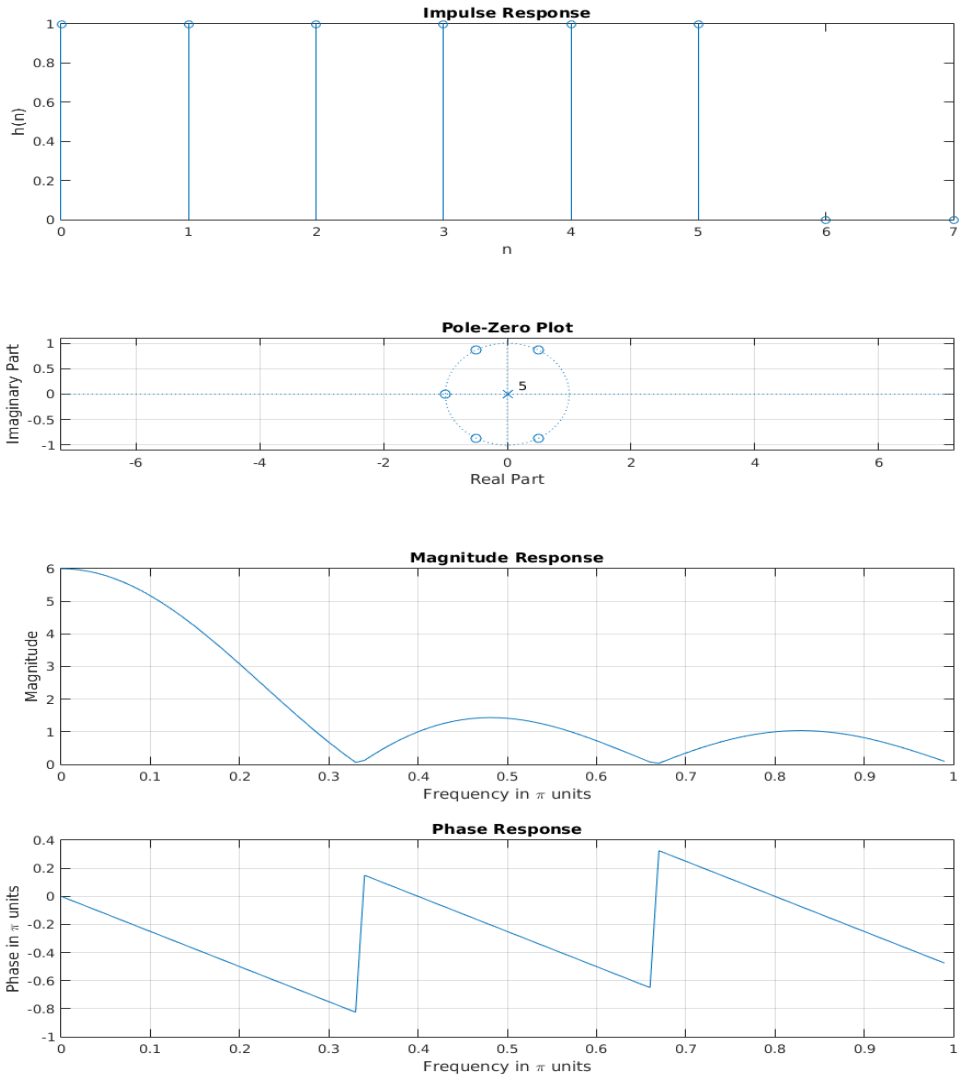

Figure 2 Expected magnitude and phase response plots

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Measurement Results

TBD

5

Measurement Analysis

TBD

Appendix A

Measurement Scripts

The Measurement Scripts consist of SCPI [7] with Python wrapper [6] and is used to controlling the measurement equipment [2] to generate a magnitude and phase response of LPFFIR FPGA implementation.

Magnitude Response Script Requirements

1. The script shall control the Waveform Generator to output a 1 V amplitude sinusoidal signal in 1 Hz to 25 MHz frequency range with 1 Hz frequency increment step.
2. The script shall control Oscilloscope to sample the output of DAC.
3. The script shall generate a magnitude response array by comparing the amplitude of sinusoidal signal from Waveform Generator with DAC output.

Phase Response Script Requirements

1. The script shall control the Waveform Generator to output a 1 V amplitude sinusoidal signal in 1 Hz to 25 MHz frequency range with 1 Hz frequency increment step.
2. The script shall control Oscilloscope to sample the output of DAC.
3. The script shall generate a phase response array by comparing the phase of sinusoidal signal from Waveform Generator with DAC output.

Appendix B

Peripheral Modules

The Analog-to-Digital Converter (ADC) [3] and Digital-to-Analog Converter (DAC) [4] peripheral modules are used for LPFFIR FPGA implementation characterization. The summary of key features of ADC and DCA are listed below:

ADC Key Features

- TBD sample period
- 12-bit analog to digital converter
- I2C interface

DAC Key Features

- TBD sample period
- 12-bit analog to digital converter
- SPI interface

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1. LPFFIR IP Core Specification: https://opencores.org/projects/lpffir
2. FPGA prototyping board: https://reference.digilentinc.com/reference/programmable-logic/basys-3/reference-manual
3. ADC peripheral module: https://reference.digilentinc.com/reference/pmod/pmodad2/reference-manual
4. DAC peripheral module: https://reference.digilentinc.com/reference/pmod/pmodda4/reference-manual
5. Mixed Signal Oscilloscope: https://www.rigolna.com/products/digital-oscilloscopes/mso5000
6. Python wrapper: https://pypi.org/project/scpi
7. Standard Commands for Programmable Instruments (SCPI): https://en.wikipedia.org/wiki/Standard_Commands_for_Programmable_Instruments