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LPFFIR IP Core Specification

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Rev. 1.0
January 27, 2019

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Revision History

Rev.	Date	Author	Description
1.0	01/27/19	Vladimir Armstrong	First Draft

Contents

1 Introduction

Lowpass filter with finite impulse response (LPFFIR) IP core is characterized by one passband and one stopband, each specified by passband ω_p edge frequency and stopband ω_s edge frequency. The LPFFIR ideal filter $H_i(e^{j\omega})$ gain is 6 in the passband and ideal attenuation in the stopband is zero, the filter design specifications include tolerance limits by which the ideal gains in the passband can be attenuated by δ_p value and ideal stopband can be gained by δ_s value. The LPFFIR tolerance scheme with edge frequencies and tolerance limits is shown in Figure 1.

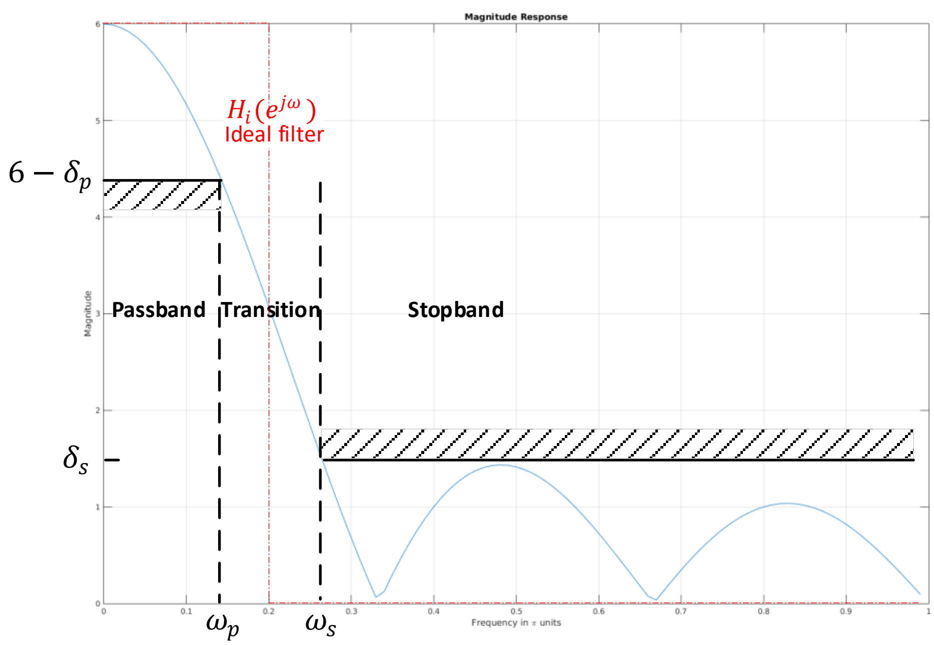

Figure 1 LPFFIR tolerance scheme.

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Specifications

The LPFFIR Figure 1 specifications are shown in Table 1

Table 1 LPFFIR specifications.

	Passband	Stopband
Ideal filter	6 gain	0 attenuation
Edge frequencies	$\omega_p = 0.14$	$\omega_s = 0.26$
Tolerance	$\delta_p = 1.56$	$\delta_s = 1.605$

Features

- LPFFIR IP core RTL is fully synthesizable into logic gates targeting ASIC devices i.e. FPGA devices CLB slices or DSP units are not required for synthesis.
- High precision 16-bit fixed-point arithmetic is used for DSP RTL implementation.

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Architecture

The Figure 2 architecture is a realization of Figure 8 DSP structure which is made up of addition (+) and delay (Z^{-1}) elements. The addition (+) element function is implemented by Full Adder (FA) module and Ripple Carry Adder (RCA) module with hierarchy of Figure 3. The delay (Z^{-1}) element is implemented by Flip Flops (FF) in a series.

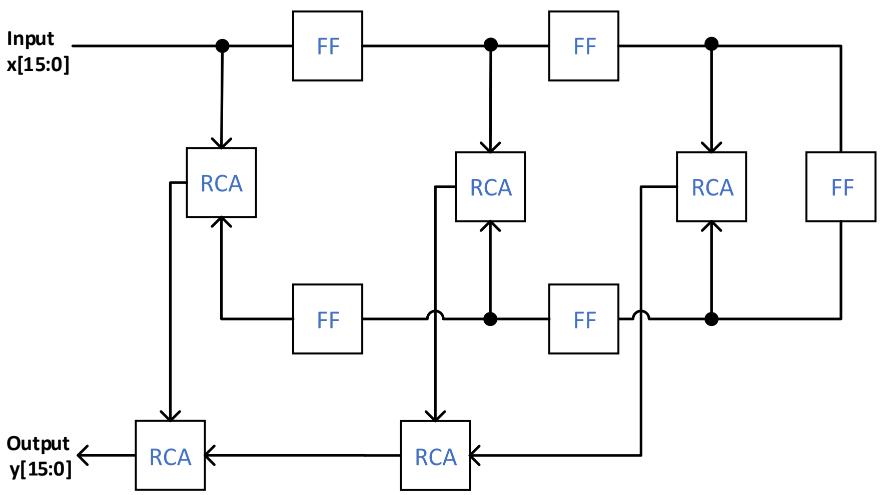

Figure 2 LPFFIR module block diagram.

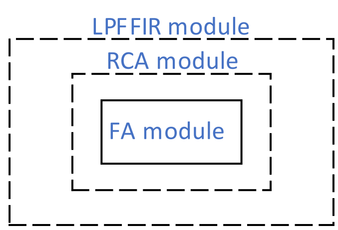

Figure 3 Module hierarchy block diagram.

The RCA module adds two 16-bit and one 1-bit binary number inputs A, B, and C_{in}(CI) respectively and outputs one 16-bit and one 1-bit binary numbers S and C_{out}(CO) respectively. The Figure 4 shows how multiple 1-bit add function FA modules are used to create 16-bit add function of RCA module.

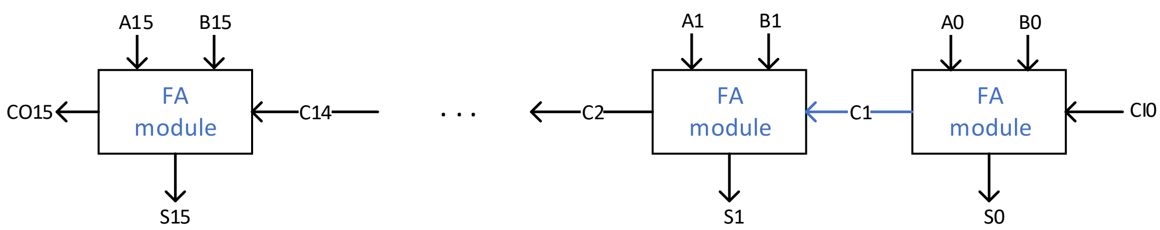

Figure 4 RCA module block diagram.

The FA module adds three 1-bit binary number inputs A, B, and C_{in}(CI) and outputs two 1-bit binary numbers S and C_{out}(CO) as gate diagram shown in Figure 5 which is an implementation of [Full adder simplified Boolean algebra expressions].

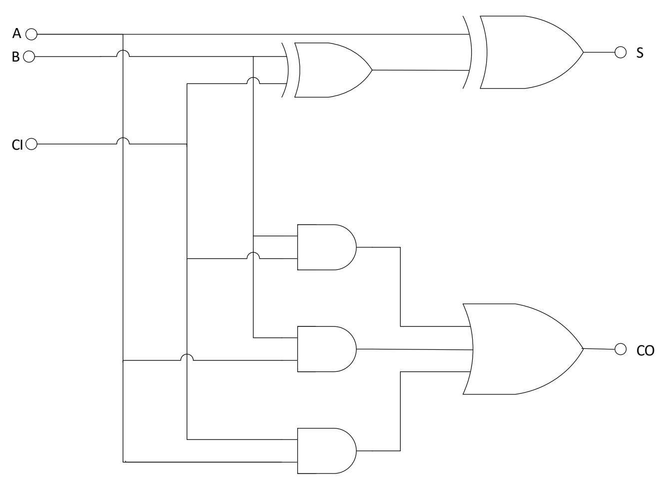

Figure 5 FA module gate diagram.

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Application

Application example of LPFFIR IP core is Discrete-Time Processing of Continuous-Time Signals[1] with block diagram of Figure 6 and frequency-domain illustration of Figure 7, if the input is bandlimited and the sampling frequency is high enough to avoid aliasing, then the overall system behaves as an LTI continuous-time system with the output is related to the input through an equation of the form

$$Y_r(j\Omega) = H_{eff}(j\Omega)X_c(j\Omega)$$

where effective continuous-time frequency responds

$$H_{eff}(j\Omega) = \begin{cases} H\left(e^{j\Omega T}\right), & |\Omega| < \pi/T \\ 0, & |\Omega| \geq \pi/T \end{cases}$$

Using $\omega = \Omega T$ relation to convert from effective continuous-time filter specification to the discrete-time filter specification results an equation of the form

$$H\left(e^{j\omega}\right) = H_{eff}\left(j\frac{\omega}{T}\right), \qquad |\omega| < \pi.$$

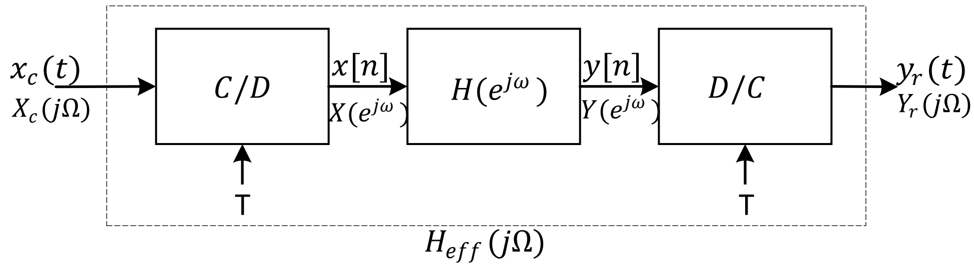

Figure 6 Discrete-time filtering of continuous-time signals system application.

The $|H_{eff}(j\Omega)|$ continuous-time overall system of Figure 6 with following requirements

1. Sample period shall be $T = 10^{-4}s$
2. The passband gain shall be 6.
3. The attenuated tolerance at the passband shall be 1.56 in the frequency band $0 \leq \Omega \leq 2\pi(1400)$.
4. The gain tolerance at the stopband shall be 1.605 in the frequency band $2\pi(2600) \leq \Omega$.

The mapping between the continuous-time and discrete-time frequencies only affects the passband and stopband edge frequencies and not the tolerance limits on frequency response magnitude [2].

The $|H(e^{j\omega})|$ discrete-time block of Figure 6 with following requirements

1. The passband gain shall be shall be 6.
2. The attenuated tolerance at the passband shall be 1.56 in the frequency band $0 \leq \omega \leq 0.14\pi$.
3. The gain tolerance at the stopband shall be 1.605 in the frequency band $0.26\pi \leq \omega$.

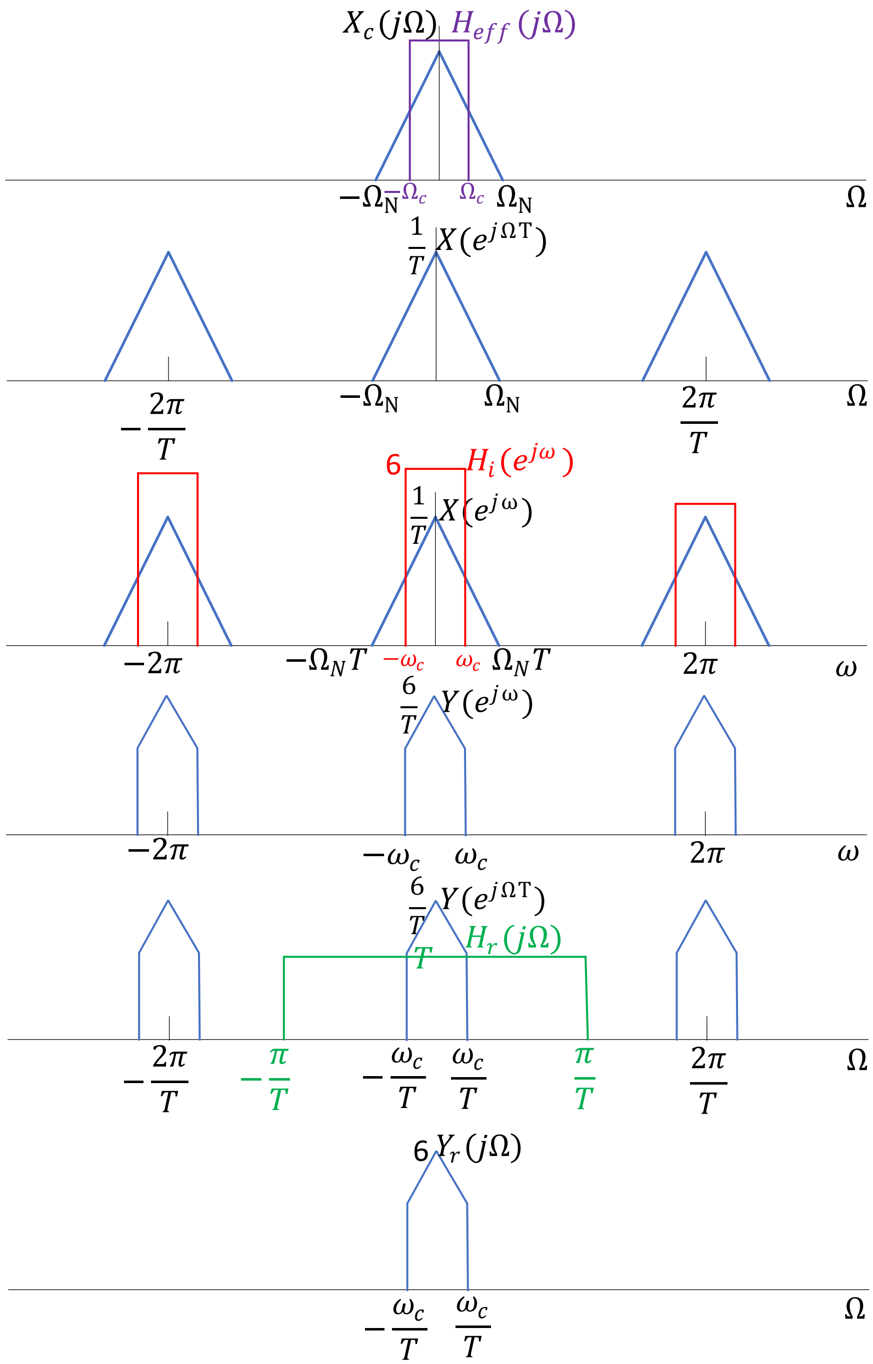

Figure 7 Frequency-domain illustration of discrete-time filtering of continuous-time signals.

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IO Ports

Port	Width	Direction	Description
clk_i	1	Input	Clock Input
x_i	16	Input	Low-pass filter Input
y_o	16	Output	Low-pass filter Output

Table 2: List of IO ports.

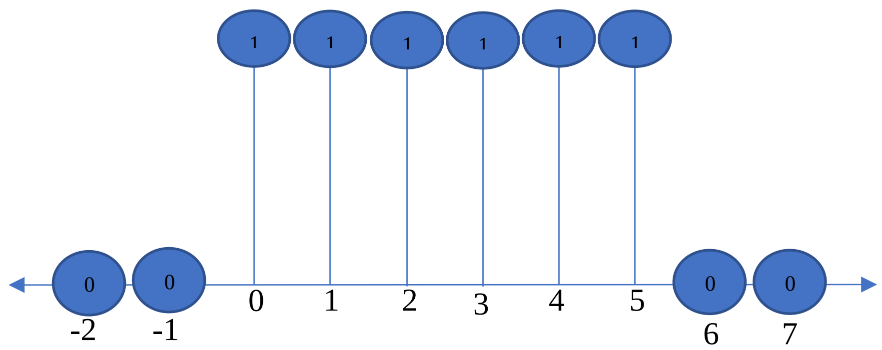
Appendix A

Structure

The LPFFIR uses a direct form structure for a FIR linear-phase system. The DSP theory [3] is used for derivation and structure is shown in Figure 8.

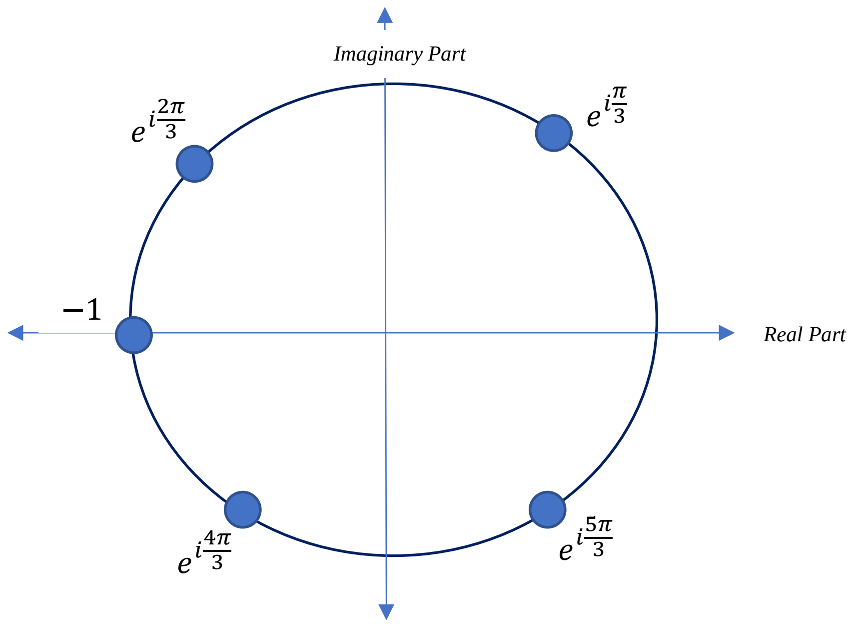
Impulse Response

$$h[n] = \begin{cases} 1, 0 \leq n \leq 5 \\ 0, otherwise \end{cases}$$



Pole Zero Plot

$$H(z) = 1 + z^{-1} + z^{-2} + z^{-3} + z^{-4} + z^{-5}$$
$$= (1 - e^{i\frac{\pi}{3}}z^{-1})(1 - e^{i\frac{2\pi}{3}}z^{-1})(1 - e^{i\pi}z^{-1})(1 - e^{i\frac{4\pi}{3}}z^{-1})(1 - e^{i\frac{5\pi}{3}}z^{-1})$$



Magnitude and Phase Response

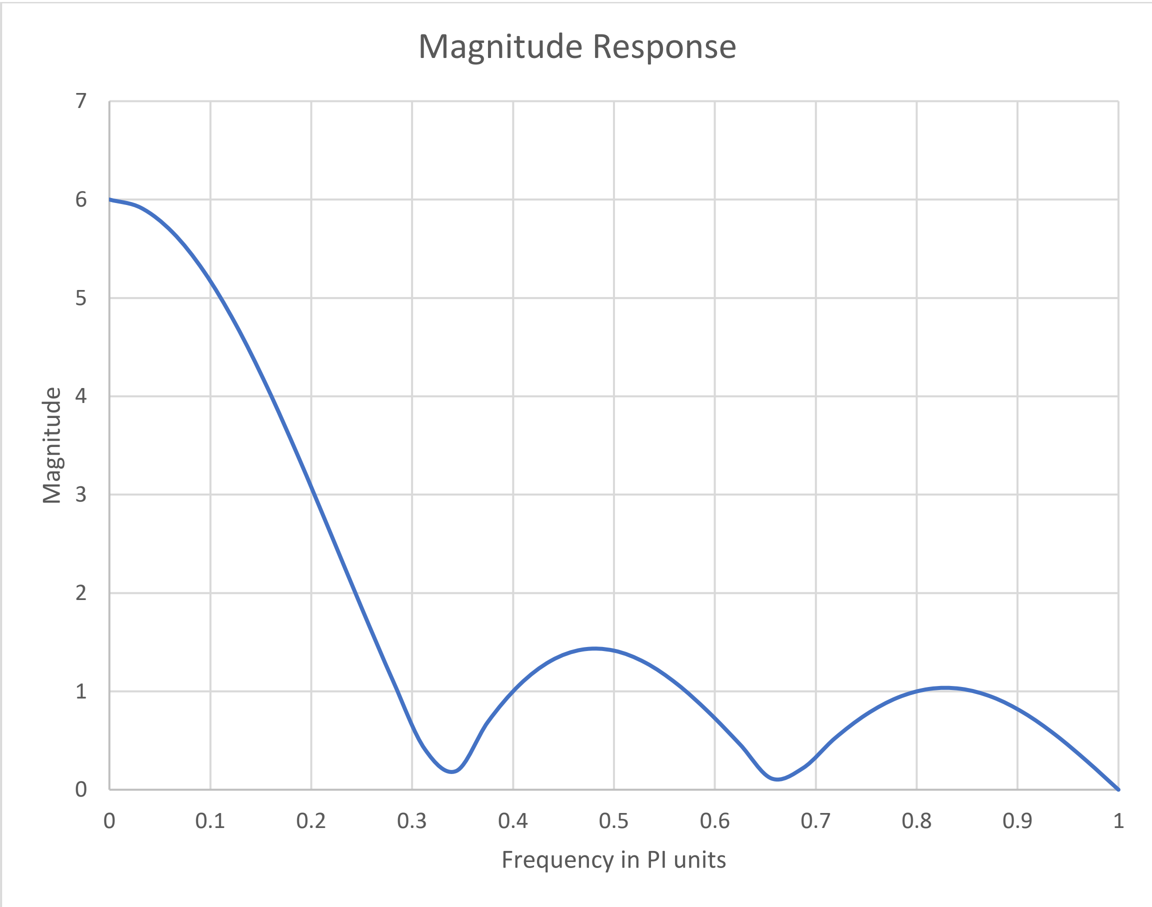
$$H\left(z=e^{i\omega}\right)=1+z^{-1}+z^{-2}+z^{-3}+z^{-4}+z^{-5}$$

$$=1+e^{-i\omega}+e^{-2i\omega}+e^{-3i\omega}+e^{-4i\omega}+e^{-5i\omega}$$

$$=\ e^{-i\omega\frac{5}{2}}(e^{i\omega\frac{5}{2}}+e^{i\omega\frac{3}{2}}+e^{i\omega\frac{1}{2}}+e^{-i\omega\frac{1}{2}}+e^{-i\omega\frac{3}{2}}+e^{-i\omega\frac{5}{2}})$$

$$=e^{-i\omega\frac{5}{2}}(2\cos\tfrac{5}{2}\omega+2\cos\tfrac{3}{2}\omega+\ 2\cos\tfrac{1}{2}\omega)$$

$$\therefore\left|H\left(z=e^{i\omega}\right)\right|=2\left|\cos\frac{5}{2}\omega+\cos\frac{3}{2}\omega+\ \cos\frac{1}{2}\omega)\right|\ and\ \measuredangle H\left(z=e^{i\omega}\right)=-\frac{5}{2}\omega$$



Structure

$$y[n] = h[n] * x[n]$$

$$= \sum_{k=0}^{M} h[k]x[n-k]$$

$$= \sum_{k=0}^{\frac{M-1}{2}-1} h[k]x[n-k] + \sum_{k=\frac{M-1}{2}+1}^{M} h[k]x[n-k]$$

$$= \sum_{k=0}^{\frac{M-1}{2}-1} h[k]x[n-k] + \sum_{k=0}^{\frac{M-1}{2}+1} h[M-k]x[n-M+k]$$

$$= \sum_{k=0}^{\frac{M-1}{2}} h[k](x[n-k] + x[n-M+k])$$

$Let: h[n] = \begin{cases} 1, 0 \le n \le 5 \\ 0, otherwise \end{cases} \Rightarrow M = 5$ Note: M is an odd integer.

$$= \sum_{k=0}^{2} h[k](x[n-k] + x[n-5+k])$$

$$= h[0](x[n] + x[n-5]) + h[1](x[n-1] + x[n-4]) + h[2](x[n-2] + x[n-3])$$

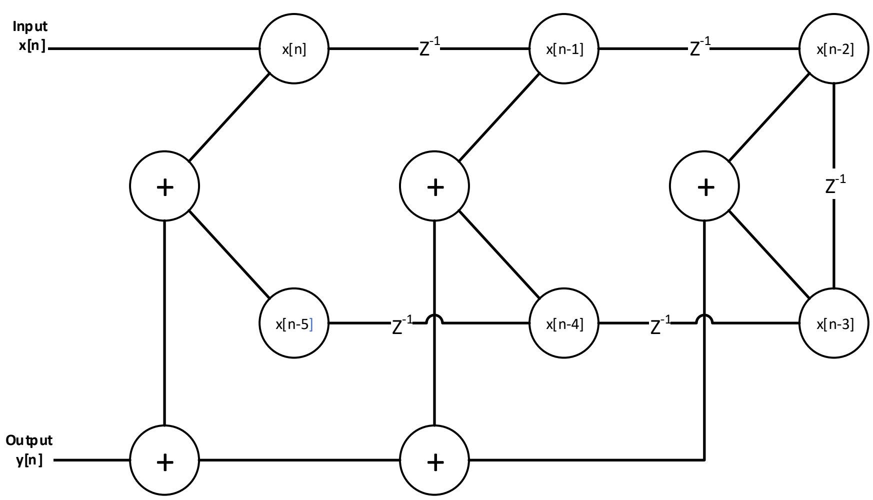


Figure 8 Direct form structure for a FIR linear-phase system.

Appendix B

Expected Behavior

The LPFFIR expected behavior is generated from MATLAB simulation. The simulation source code and result plot are shown in Figure 9 and Figure 10 respectively.

```
% FIR difference equation of lowpass filter
b = [1, 1, 1, 1, 1, 1]; a = [1];

% Response
n = [0:7];
h = impz(b,a,8);
[H,w] = freqz(b,a,100);
magH = abs(H); phaH = angle(H);

% Plot
subplot(4,1,1); stem(n,h);
title('Impulse Response'); xlabel('n'); ylabel('h(n)')

subplot(4,1,2);zplane(b,a);grid
title('Pole-Zero Plot')

subplot(4,1,3);plot(w/pi,magH);grid
xlabel('Frequency in \pi units'); ylabel('Magnitude');
title('Magnitude Response')

subplot(4,1,4);plot(w/pi,phaH/pi);grid
xlabel('Frequency in \pi units'); ylabel('Phase in \pi units');
title('Phase Response')
```

Figure 9 MATLAB simulation source code.

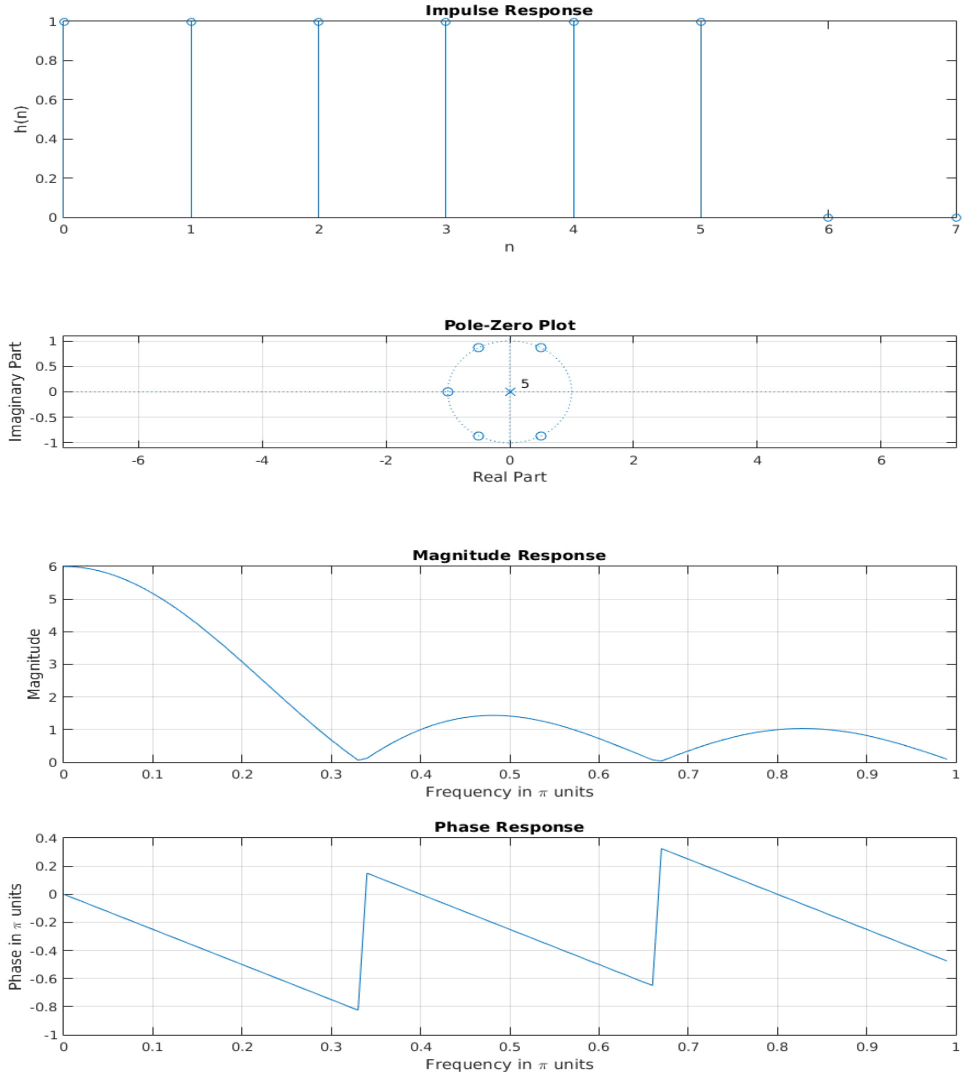
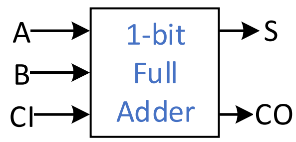


Figure 10 MATLAB simulation result plot.

Appendix C

Full adder Boolean algebra expressions



- $CO = B \cdot CI + A \cdot CI + A \cdot B + A \cdot B \cdot CI$
- $S = \bar{A} \cdot \bar{B} \cdot CI + \bar{A} \cdot B \cdot \overline{CI} + A \cdot \bar{B} \cdot \overline{CI} + A \cdot B \cdot CI$

The full adder Boolean expressions are derived from truth Table 3.

Table 3 Full adder truth table.

Input			Output	
A	**B**	**CI**	**CO**	**S**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Full adder simplified Boolean algebra expressions

- $CO = B \cdot CI + A \cdot CI + A \cdot B$
- $S = A \oplus B \oplus CI$

The K-map of Table 4 and Table 5 are used for simplifying Boolean algebra expressions of full adder.

Table 4 Full adder K-map of CO.

	$\overline{A} \cdot \overline{B}$	$\overline{A} \cdot B$	$A \cdot B$	$A \cdot \overline{B}$
$\overline{CI}$	0	0	1	0
C	0	1	1	1

Table 5 Full adder K-map of S.

	$\overline{A} \cdot \overline{B}$	$\overline{A} \cdot B$	$A \cdot B$	$A \cdot \overline{B}$
$\overline{CI}$	0	1	0	1
C	1	0	1	0

Index

1. Oppenheim, A. V., & Ronald, W. S. (2009). Discrete-Time Processing of Continuous-Time Signals. In *Discrete-Time Signal Processing 3rd Edition* (pp. 197-172). Upper Saddle River, NJ: Pearson
2. Oppenheim, A. V., & Ronald, W. S. (2009). Filter Specifications. In *Discrete-Time Signal Processing 3rd Edition* (pp. 494-496). Upper Saddle River, NJ: Pearson
3. Oppenheim, A. V., & Ronald, W. S. (2009). Structures for Linear-Phase FIR Systems. In *Discrete-Time Signal Processing 3rd Edition* (pp. 403-405). Upper Saddle River, NJ: Pearson.