

TRIPUTER

V0.1

User Manual

25.11.2018

# Introduction

TRIPUTER V0.1 is a small computer based on the Cyclone V GX Starter Kit. The main purpose is to test the capabilities of the M32632. The Series 32000 compatible CPU is running at 50 MHz. The FPGA contains all the logic functions and part of the memories. TRIPUTER V0.1 needs 6,803 of the 29,080 ALMs (23.4%) in the FPGA. (ALM = adaptive logic module)

First the FPGA has to be configured. This is done by the software Quartus Web Edition. Preferable is version 13.1 or higher. The configuration needs no project definition. All information is contained in the SOF file or POF file. SOF files configure the SRAM cells in the FPGA directly. This is useful for testing a new hardware. POF is written to a flash device which configures the FPGA at power-up.

TRIPUTER V0.1 uses a terminal for user I/O. The connection is based on USB. My host is a PC running Windows XP. To enable the USB interface on the FPGA board a driver is needed. Maybe modern OS have this capability already build in. The driver is for the FT232R chip and can be downloaded from the website of FTDI ([www.ftdichip.com](http://www.ftdichip.com)).

I use HyperTerminal on my PC. The parameters of the transmission are 57,600 baud, 8 data bits, one stop bit and no parity. The software is easy to use. It has a function for downloading a text file without handshaking. This is used to download a program or data to TRIPUTER V0.1 . Upload is currently not available and must be programmed by the user.

## Hardware

### Definitions:

0 : read as "0"

x : read value is unknown

RAM : Read/Write Memory

ROM : Read Only Memory

Reg : Register , always 4 Bytes wide

All addresses are in hexadecimal notation if not otherwise defined.

### Reset behaviour:

After RESET the CPU starts program execution at address 00000000. To make a defined start the ROM is accessed instead of the internal DRAM (iDRAM).

This behaviour is changed to normal mode by an instruction fetch to an address  $\geq 20000000$ . The JUMP instruction can be used for this:

```
00000000      MOVD x'20000008,R0 ; first two opcodes in ROM
00000006      JUMP R0
```

Coding the target address as a displacement is not possible.

The RESET button is KEY4 = CPU\_RESET.

### Memory Map:

<u>Address range</u>	<u>Type</u>	<u>Description</u>
00000000..0001FFFF	RAM	128KB internal DRAM Emulator. See <u>Reset behaviour.</u>
20000000..200007FF	ROM	2KB internal MONITOR program
20100000..2017FFFF	RAM	512KB external 16-bit SRAM
20200000	Reg	UART : Serial Interface
20300000	Reg	SSW : Slide Switches
20400000	Reg	LERG : Red and Green LEDs
20400004	Reg	LESS : Seven Segment LEDs
20500000	Reg	COUNT : NMI Counter
20500004	Reg	NECO : NMIE + NMI Counter

### **Register UART**

Address : x'2020\_0000

131	24!23	16!15	8 !7	0 !
+	+	!	+	!
!	!	!	T T T R R R !	!
! 0 0 0 0 0 0 0 0 0	! 0 0 0 0 0 0 0 0 0	! 0 0 0 I E B I E B	! D D D D D D D D D !	
+	+	!	+	!

<u>ID</u>	<u>Name</u>	<u>Bits</u>	<u>Access</u>	<u>Description</u>
TI	TXI	13	R/W	TX Interrupt: set to "1" if transmission finished
TE	TXIE	12	R/W	TX Interrupt Enable: enables interrupt if TXI="1"
TB	TXB	11	R	TX Busy: "1" if transmitter is busy
RI	RXI	10	R/W	RX Interrupt: set to "1" if new data is available
RE	RXIE	9	R/W	RX Interrupt Enable: enables interrupt if RXI="1"
RB	RXB	8	R	RX Busy: "1" if receiver is busy
D	DATA	7:0	R/W	DATA[7:0]: 8-bit data to send or to read. A write starts a transmission and clears TXI. If the TX is busy a write to data has no effect. Read data clears the RXI.

Reset

TXI = TXIE = TXB = RXI = RXIE = RXB = 0

Remark

Both interrupts use the same interrupt input of the CPU. If both interrupts are enabled the software must find the active source. Maybe both are active at the same time.

No options are available. The baudrate is fixed at 57,600 baud. The transmission format is fixed to 8-N-1. The BREAK condition is neither detected nor generated.

### Register SSW

Address : x'2030\_0000

```

|31          24|23          16|15          8 |7          0 |
+            +            !            +            !            +            !            +            !
!0 0 0 0 0 0 0 0 0 !0 0 0 0 0 0 0 0 0 !0 0 0 0 0 0 0 0 0 S S !S S S S S S S S S S !
+            +            !            +            !            +            !            +            !

```

ID	Name	Bits	Access	Description
S	SWITCH	9:0	R	SWITCH[9:0]: the 10 slide switches named from SS0 to SS9 of the Cyclone V GX Starter Kit.

Reset  
no action

### Register LERG

Address : x'2040\_0000

```

|31          24|23          16|15          8 |7          0 |
+            +            !            +            !            +            !            +            !
!x x x x x x x x x !G G G G G G G G G !x x x x x x x R R !R R R R R R R R R R !
+            +            !            +            !            +            !            +            !

```

ID	Name	Bits	Access	Description
G	LEDG	23:16	W	LEDG[7:0]: the 8 green LEDs named LEDG0 to LEDG7 of the Cyclone V GX Starter Kit.
R	LEDR	9:0	W	LEDR[9:0]: the 10 red LEDs named LEDR0 to LEDR9 of the Cyclone V GX Starter Kit.

Reset  
no action

### Register LESS

Address : x'2040\_0004

```

|31          24|23          16|15          8 |7          0 |
+            +            !            +            !            +            !            +            !
!x x x x x x x x x !x x x x x x x x x !x M M M M M M M M !x L L L L L L L L !
+            +            !            +            !            +            !            +            !

```

ID	Name	Bits	Access	Description
M	LESSM	14:8	W	LESSM[6:0]: the seven segment LED named HEX1 of the Cyclone V GX Starter Kit.
L	LESSL	6:0	W	LESSL[6:0]: the seven segment LED named HEX0 of the Cyclone V GX Starter Kit.

Reset  
no action

Remark  
The segment 0 is LESSx[0] at the top clockwise up to segment 6 which is LESSx[6]. DP is not available.

### Register COUNT

Address : x'2050\_0000

```
!31          24!23          16!15          8 !7          0 !
+            +            !            +            !            +            !
!0 0 0 0 0 0 0 C C !C C C C C C C C C C !C C C C C C C C C C !C C C C C C C C C C !
+            +            !            +            !            +            !
```

<u>ID</u>	<u>Name</u>	<u>Bits</u>	<u>Access</u>	<u>Description</u>
C	COUNTER	25:0	R	COUNTER[25:0]: counts upward starting at 0 to 49,999,999 . This counter is not stopable, except in Reset. The NMI occurs if the counter is >49,999,983.

#### Reset

COUNTER = 26'd0

### Register NECO

Address : x'2050\_0004

```
!31          24!23          16!15          8 !7          0 !
+            +            !            +            !            +            !
!N 0 0 0 0 0 0 0 C C !C C C C C C C C C C !C C C C C C C C C C !C C C C C C C C C C !
+            +            !            +            !            +            !
```

<u>ID</u>	<u>Name</u>	<u>Bits</u>	<u>Access</u>	<u>Description</u>
N	NMIE	31	R/W	NMI Enable: enable NMI if set to "1"
C	COUNTER	25:0	R	COUNTER[25:0]: same as register COUNT

#### Reset

NMIE = 0 , COUNTER same as in COUNT

# Software

TRIPUTER V0.1 has a simple monitor program called MONITOR. It provides five commands: LOAD, RUN, DUMP, + and - . Only the first letter of LOAD, RUN and DUMP is necessary. Commands and adresse are not case sensitive. Addresses are entered as hexadecimal numbers.

MONITOR displays a second clock on the seven segment LEDs. If a character is received by the UART the value is shown on the red LEDs and the index in the buffer on the green LEDs. Heavy flashing occurs during a download.

The content of the ROM can be replaced by any other software on request.

## Register Definitions:

SP0	Stack Pointer	00000300
INTBASE	Interrupt Base	00000300
SB	Static Base	00000400

All other registers are not used.

Memory Map: MONITOR uses iDRAM for its own data.

00000200..000002FF	Stack Area
00000300..0000037F	Interrupt Vector Area
00000380..000004FF	Static Base Area
00000500..000005FF	Serial Interface Input Area

<u>Commands</u>	<u>&lt;CR&gt;</u>	<u>Description</u>
L(OAD) address	YES	LOAD downloads bytes from the host system. The format is Intel Hex without any flow control. LOAD shows after each line received the total number of bytes received.
R(UN) address	YES	RUN executes a program. It uses the instruction "BSR addr" to start the program. The instruction "RET 0" is used at the end of the program to return to MONITOR.
D(UMP) address	YES	DUMP displays 16 lines of 16 bytes each. Each line shows the address, the bytes in hexadecimal form and a alphanumerical interpretation.
+	NO	performs a DUMP with the last DUMP address + 256.
-	NO	performs a DUMP with the last DUMP address - 256.

## Remark

First and last line of a file in Intel Hex format:

```
:080000000102030405060708D4  
:00000001FF
```