PC calculation

This document is the reference one about the pps_pf module included in the miniMIPS core. The goal of this module is the calculation of the PC calculation at each core clock cycle.

Typically, at each step, the PC is incremented by four as each instruction is 32 bits long. In other cases, the module take care of the following signals by order of priority :

- The *reset* signal initializes the PC to the boot address which is defined in the pack_mips.
- The *stop_all* signal freezes the PC. This command appears when the pipeline must be locked to wait for a memory data.
- The *exch_cmd* loads the PC with the *exch_adr*. This command appears when an exception or an interruption occured in the pipeline.
- The *bra_cmd_pr* loads the PC with the *bra_adr*. This command appears when a bad prediction has occured.
- The *stop_pf* locked the PC. It appears when a data hazard is in the pipeline in order to wait the data.
- The *bra_cmd* loads the PC with the *bra_adr*. This command appears when a prediction is possible. Two different commands loads the PC with *bra_adr*. The first one is prioritary on the *stop_pf* signal as the data hazard is here only because of a bad prediction. The second one must wait for the data hazard resolution before predicting a new address.
- Of course if none of those signals have appeared the PC is incremented by four to point to the next instruction.