

# Minimal OpenRISC System on Chip

## How To

### 1 Download IP cores

1. download minsoc
2. download further necessary IP cores
  - a) `cd minsoc/rtl/verilog`
  - b) `svn co http://opencores.org/ocsvn/adv_debug_sys/adv_debug_sys/trunk adv_debug_sys`
  - c) `svn co http://opencores.org/ocsvn/ethmac/ethmac/trunk ethmac`
  - d) `svn co http://opencores.org/ocsvn/openrisc/openrisc/trunk/or1200 or1200`
  - e) `svn co http://opencores.org/ocsvn/uart16550/uart16550/trunk uart16550`

### 2 Install GNU toolchain and adv\_jtag\_bridge

1. Follow: [http://www.opencores.org/openrisc.gnu\\_toolchain](http://www.opencores.org/openrisc.gnu_toolchain) (to install binutils, gcc, gdb)
2. To debug and load the firmware you have to use the new advanced\_debug\_system. This project is included in the minsoc files inside of minsoc/rtl/verilog/adv\_debug\_sys. There you can find the software in Software and the documentation, which shall help you to go under Doc.
  - a) change the Makefile in Software/adv\_jtag\_bridge and compile the software using make.
  - b) `sudo make install`
  - c) Copy the description file of your FPGA to your home directory `“cp /opt/Xilinx/10.1/ISE/spartan3e/data/xc3s500e_fg320.bsd ~/”`
3. With the adv\_jtag\_bridge you can also debug your simulation. To do so, the simulation has to include a vpi module. This has to be compiled by your system. The sources are found under “minsoc/adv\_debug\_sys/Software/adv\_jtag\_bridge/sim\_lib/icarus”.
  - a) `cd minsoc/adv_debug_sys/Software/adv_jtag_bridge/sim_lib/icarus`
  - b) `make`
  - c) `cp minsoc_adv_debug_sys/Software/adv_jtag_bridge/sim_lib/icarus/jp-io-vpi.vpi minsoc/bench/verilog/vpi`
4. The adv\_jtag\_bridge connect the debug system to gdb, the GNU debugger. But the actual version of gdb has some issues, which have to be corrected before use. To do so, the adv\_jtag\_bridge software includes a patch for gdb. Save the patch to the gdb source code directory installed by the toolchain installation script and patch it:
  - a) `cp minsoc/adv_debug_sys/Software/adv_jtag_bridge/gdb-6.8-bz436037-reg-no-longer-active.patch toolchain_build_directory/gdb-6.8`
  - b) `cd toolchain_build_directory/gdb-6.8`
  - c) `patch -p1 < gdb-6.8-bz436037-reg-no-longer-active.patch`

- d) make
- e) sudo make install

### 3 Compile Software

1. edit sw/support/orp.ld line 14 LENGTH = 0x00006E00 to
  - a) your memory amount in Bytes  $4 \cdot 2^{MEMORYADRWIDTH}$ , where MEMORYADRWIDTH is defined in `define MEMORY\_ADR\_WIDTH in “minsoc\_defines.v”  
 $4 \cdot 2^{MEMORYADRWIDTH}$  minus ORIGIN = 0x00001200  
(e.g.  $4 \cdot 2^{13} = 32,768$  Bytes = 0x8000 | LENGTH = 0x8000 – 0x1200 = 0x6E00)
2. select your STACK size on board.h line 16 #define STACK\_SIZE 0x01000
  - a) change your IN\_CLK if not using 25000000 (25MHz)
3. inside of sw/support make clean, make all
4. inside of sw/utills make clean, make all
5. inside of the target software (e.g. sw/uart) make clean, make all

### 4 Simulation

1. Install Icarus Verilog
  - a) You will need at least version 0.9.1 (<ftp://ftp.icarus.com/pub/eda/verilog/v0.9/>)
2. configure your system: minsoc\_defines.v (**not necessary**)
  - a) **Note: (since revision 17)** Ethernet functionality of testbench does not base on eth\_phy.v anymore. This means that you can uncomment ETHERNET on minsoc\_defines.v and simulate it without simulation speed decrease and without changing any file.
  - b) **Previous to revision 17:** if you uncomment “`define ETHERNET” you have to:
    - edit “minsoc/sim/run/generate\_bench”:
      - substitute “../bin/minsoc\_model\_fast.txt” for “../bin/minsoc\_model\_complete.txt”
    - THIS WILL SLOW DOWN YOUR SIMULATION BY FACTOR 300
3. configure minsoc\_bench\_defines.v (**not necessary**)
  - a) Your testbench will use a memory model, not actually the same memory controller the implementation uses. This enables the option “`define INITIALIZE\_MEMORY\_MODEL”, where the firmware is loaded to the memory before testbench start.
  - b) You may use the actual implementation memory:
    - comment “`define INITIALIZE\_MEMORY\_MODEL”
    - edit minsoc/sim/run/generate\_bench
      - substitute “../bin/minsoc\_model.txt” for “../bin/minsoc\_memory.txt”
    - You might want to uncomment “`define START\_UP”, it loads the firmware to a SPI memory. At start of testbench the system reads this memory and loads the firmware to

main memory. Takes +-3 min. This is possible to be used for a real system, all you have to do is uncomment “`define START\_UP” from minsoc/rtl/verilog/minsoc\_defines.v.

#### 4. Modify testbench (**not necessary**)

#### 5. command to start testbench and select firmware

a) from minsoc/sim/run/

➤ ./generate\_bench

➤ ./run\_bench <your\_firmware.hex>

- ./run\_bench ../../sw/uart/uart-nocache-twobyte-sizefirst.hex

#### 6. Debugging the testbench (3 terminals)

a) terminal 1: from minsoc/sim/run/

➤ ./generate\_bench

➤ ./run\_bench <your\_firmware.hex>

- ./run\_bench ../../sw/uart/uart-nocache-twobyte-sizefirst.hex

b) terminal 2: from minsoc/sim/run

➤ ./start\_server

c) terminal 3: at minsoc/sw/uart

➤ or32-elf-gdb uart-nocache.or32

➤ target remote :9999

➤ load

- if you have INITIALIZE\_MEMORY\_MODEL enabled you don't have to do this
- if you have START\_UP and waited for the message: “Memory start-up completed...” you also don't need this

➤ set \$pc=0x100

➤ c

## 5 Implementation

#### 1. configure minsoc\_defines.v (recommended values for different devices under 7. Examples)

a) Select your FPGA device by uncommenting its manufacturer and commenting all other manufacturers. Select then your FPGA model by uncommenting it in case you have a Xilinx FPGA, for Altera comment all out.

b) `define MEMORY\_ADR\_WIDTH 13 defines the amount of memory you get. The depth is defined by  $2^{MEMORYADRWIDTH}$ , since its data width is 32 bits, the amount in Bytes is 4 times its depth. (this is not allowed to be less than 12, 11 is the memory block address width)

c) choose a clock division for your global clock related to your design max speed by changing the definition: “`define CLOCK\_DIVISOR 5”. If you have an Altera device please use only even numbers for the division, odd numbers are going to be rounded down.

- d) Define your RESET polarity: uncomment `"`define POSITIVE_RESET"` for an active high reset or `"`define NEGATIVE_RESET"` for an active low reset and comment the other.
- 2. configure `or1200_defines.v` (optional -> reduce logic usage) (recommended values for different devices under 7. Examples)
  - a) Target FPGA memories (`OR1200_XILINX_RAMB16` for Xilinx, Spartan 3 and above, `OR1200_ALTERA_LPM` for all Altera)
  - b) Type of register file RAM (generic, twoport or dual port) (dual port is supported by Xilinx BRAM and Altera)(**select only one of the three**)
  - c) If not using Linux you can comment out `OR1200_QMEM_IMPLEMENTED`.
- 3. define user constraints for system pinout (edit `backend/yourboard.ucf` file)
- 4. create project in project manager (ISE, Quartus), include files
- 5. synthesize, P&R and upload bitfile
- 6. connect the cable to the selected JTAG TAP

## 6 Software Upload and Debugging

Upload software and debug for simulation and implementation using GDB

1. start `adv_jtag_bridge`
  - a) `cd ~/`
  - b) `sudo adv_jtag_bridge xpc3 (xess, usbbaster, xpc_usb, ft2232)`
  - c) Let the program running and open another terminal
2. Open a terminal program (e.g. `gtkterm`)
  - a) configure port to a serial port connected to your board
  - b) configure bitrate to 115200
3. start `gdb`, load firmware (example)
  - a) `cd minsoc/sw/uart`
  - b) `or32-elf-gdb uart-nocache.or32`
  - c) `target remote :9999`
  - d) `load`
  - e) `set $pc=0x100`
  - f) `c`
4. Inside of `gtkterm` "Hello World." should have appeared, if you press any key inside of `gtkterm` the processor will return the next alphabetical letter (press a, it returns b)

## 7 Examples

Note: different constraint files for different boards → inside of backend directory

1. Spartan 3A DSP 1800 (100%)

- a) minsoc\_defines.v
    - no definitions change, ready to go
  - b) or1200\_defines.v (optional, reduce logic use)
    - uncomment `define OR1200\_XILINX\_RAMB16
    - uncomment `define OR1200\_RFRAM\_DUALPORT
    - comment `define OR1200\_RFRAM\_GENERIC
2. Spartan 3E Starter Kit **no Ethernet** (100%)
- a) minsoc\_defines.v
    - comment `define SPARTAN3A
    - uncomment `define SPARTAN3E
    - change CLOCK\_DIVISOR from 5 to 2
    - comment `define ETHERNET
  - b) or1200\_defines.v
    - uncomment `define OR1200\_XILINX\_RAMB16
3. Spartan 3E Starter Kit **with Ethernet (not tested)**
- a) Synthesis properties:
    - Optimization Goal: Area
    - Optimization Effort: High
  - b) minsoc\_defines.v
    - comment `define SPARTAN3A
    - uncomment `define SPARTAN3E
    - let CLOCK\_DIVISOR at 5
    - change MEMORY\_ADR\_WIDTH from 13 to 12
    - uncomment `define ETHERNET
    - comment `define UART
      - this is not necessary, though you will get 99% device usage if not commenting, 89% otherwise.
  - c) or1200\_defines.v
    - uncomment `define OR1200\_XILINX\_RAMB16
    - comment `define OR1200\_MULT\_IMPLEMENTED
    - comment `define OR1200\_MAC\_IMPLEMENTED
    - uncomment `define OR1200\_RFRAM\_DUALPORT
    - comment `define OR1200\_RFRAM\_GENERIC

- comment `define OR1200\_PM\_IMPLEMENTED
- comment `define OR1200\_QMEM\_IMPLEMENTED
- comment `define OR1200\_CFGR\_IMPLEMENTED

d) eth\_defines.v

- uncomment `define ETH\_FIFO\_XILINX
- uncomment `define ETH\_XILINX\_RAMB4

e) Collateral effects:

- from sw/support/Makefile.inc line 7:
  - GCC\_OPT=-mhard-mul -g to GCC\_OPT=-msoft-mul -g
- change sw/support/orp.ld:
  - ram: LENGTH = from 0x00006E00 to 0x00002E00
  - this is not much memory, I recommend the inclusion of the wb\_ddr project to minsoc to use your DDR SRAM memory
- Further area optimization possibilities: **(not necessary, DON'T DO)**
  - Turn off: pic, tick timer or debug unit

#### 4. Altera Devices

a) minsoc\_defines.v

- uncomment `define ALTERA\_FPGA
- comment `define XILINX\_FPGA
- comment `define SPARTAN3A
- select your memory amount "`define MEMORY\_ADR\_WIDTH 13"
- choose a clock division for your global clock related to your design max speed by changing the definition: "`define CLOCK\_DIVISOR 5". Since you have an Altera device please use only even numbers for the division, odd numbers are going to be rounded down.
- Define your RESET polarity uncommenting "`define POSITIVE\_RESET" or "`define NEGATIVE\_RESET" and commenting the other.

b) or1200\_defines.v

- uncomment `define OR1200\_ALTERA\_LPM
- uncomment `define OR1200\_RFRAM\_DUALPORT
- comment `define OR1200\_RFRAM\_GENERIC
- comment `define OR1200\_QMEM\_IMPLEMENTED