Installation Instructions

Install Icarus Verilog

1. You will need at least version 0.9.1 (ftp://ftp.icarus.com/pub/eda/verilog/v0.9/)

Download IP cores

1. download minsoc
2. download further necessary IP cores
   a) cd minsoc/rtl/verilog
   b) svn co http://opencores.org/ocsvn/adv_debug_sys/adv_debug_sys/trunk adv_debug_sys
   c) svn co http://opencores.org/ocsvn/ethmac/ethmac/trunk ethmac
   d) svn co http://opencores.org/ocsvn/openrisc/openrisc/trunk/or1200 or1200
   e) svn co http://opencores.org/ocsvn/uart16550/uart16550/trunk uart16550

Install GNU toolchain and adv_jtag_bridge

1. Follow: http://www.opencores.org/openrisc,gnu_toolchain (to install binutils, gcc, gdb)
2. To debug and load the firmware you have to use the new advanced_debug_system. This project is included in the minsoc files inside of minsoc/rtl/verilog/adv_debug_sys. There you can find the software in Software and the documentation, which shall help you to go under Doc.
   a) change the Makefile in minsoc/rtl/verilog/adv_debug_sys/Software/adv_jtag_bridge and compile the software using make.
      - change Makefile line 34, “INCLUDE_JSP_SERVER=true” to “INCLUDE_JSP_SERVER=false”
      - make
      - sudo make install
   b) Copy the description file of your FPGA to your home directory “cp /opt/Xilinx/10.1/ISE/spartan3e/data/xc3s500e_fg320.bsd ~/”
3. With the adv_jtag_bridge you can also debug your simulation. To do so, the simulation has to include a vpi module. This has to be compiled by your system. The sources are found under “minsoc/rtl/verilog/adv_debug_sys/Software/adv_jtag_bridge/sim_lib/icarus”.
   a) cd minsoc/rtl/verilog/adv_debug_sys/Software/adv_jtag_bridge/sim_lib/icarus
   b) make
   c) cp jp-io-vpi.vpi minsoc/bench/verilog/vpi
4. The adv_jtag_bridge connect the debug system to gdb, the GNU debugger. But the actual version of gdb has some issues, which have to be corrected before use. To do so, the adv_jtag_bridge software includes a patch for gdb. Save the patch to the gdb source code directory installed by the toolchain installation script and patch it:

a) cp minsoc/rtl/verilog/adv_debug_sys/Software/adv_jtag_bridge/gdb-6.8-bz436037-reg-no-longer-active.patch toolchain_build_directory/gdb-6.8

b) cd toolchain_build_directory/gdb-6.8

c) patch -p1 < gdb-6.8-bz436037-reg-no-longer-active.patch

d) make

e) sudo make install