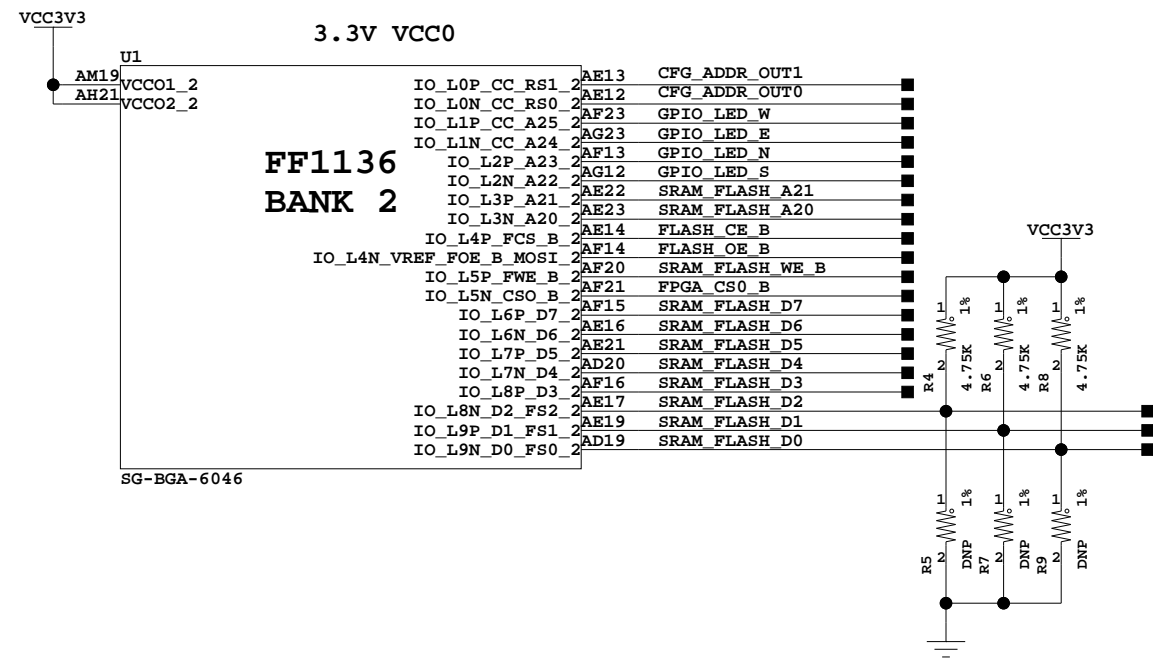
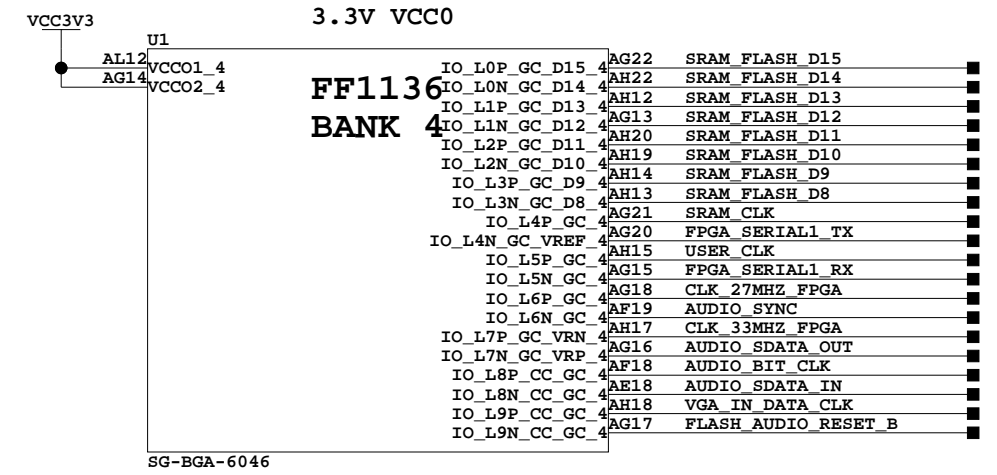
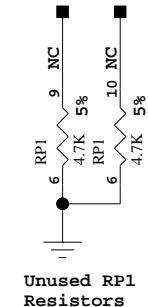
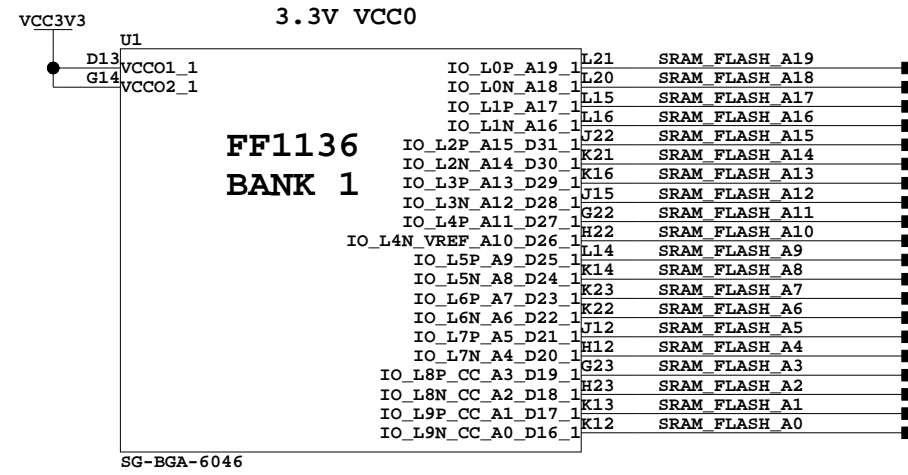
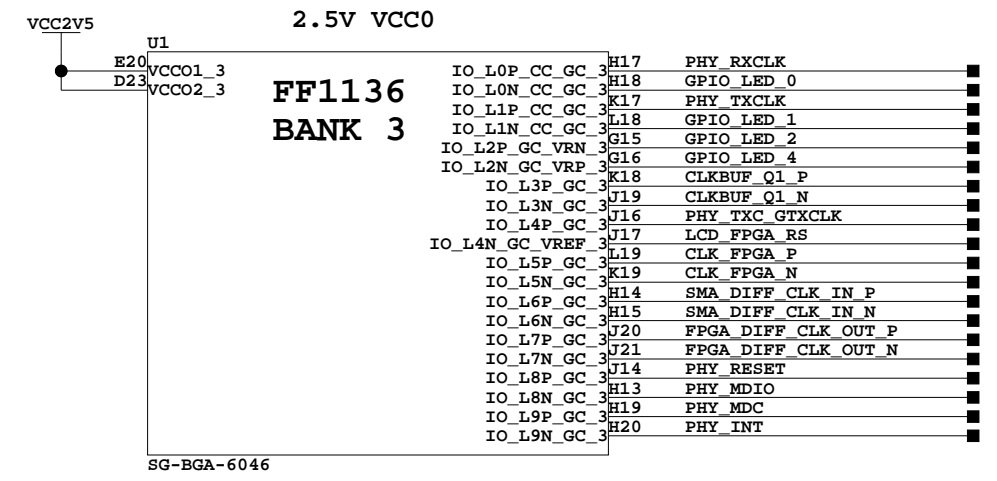
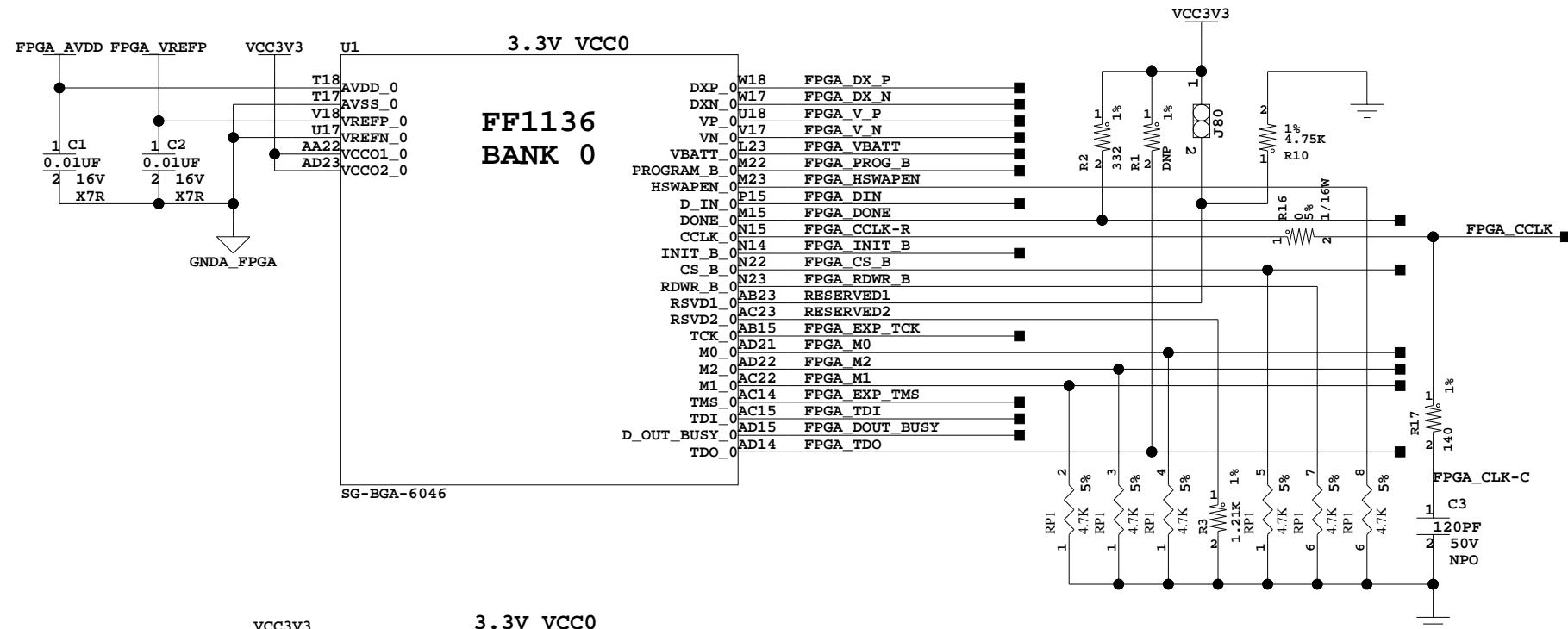


**XILINX**

Title: ML505/6/7 Block Diagram SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241

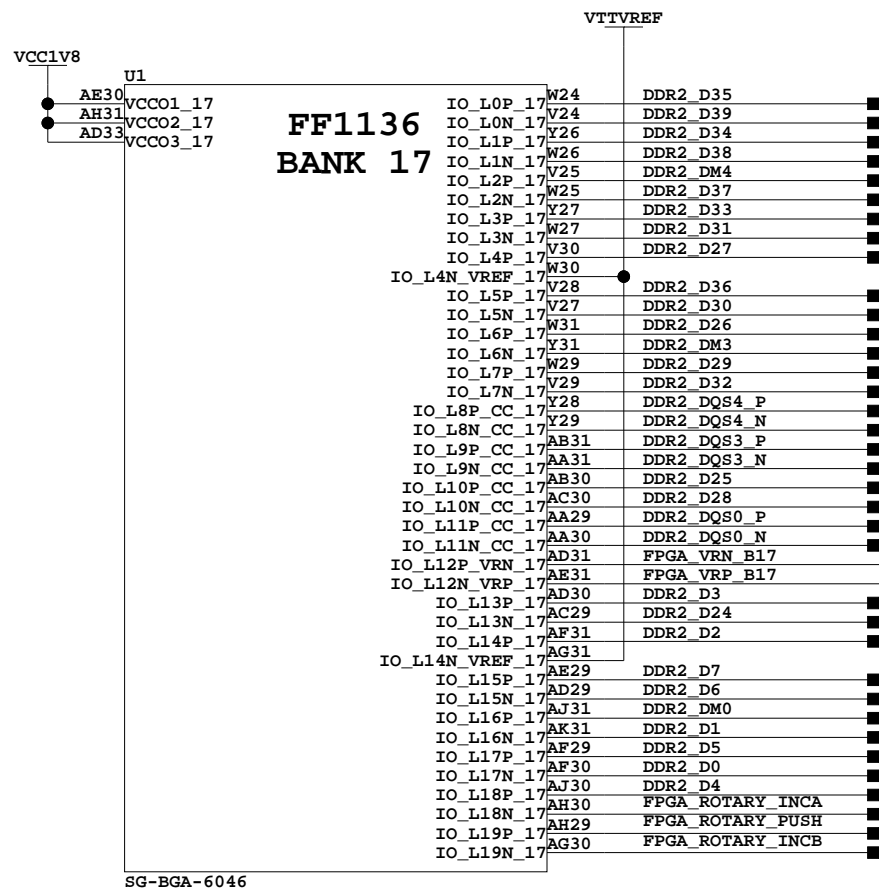
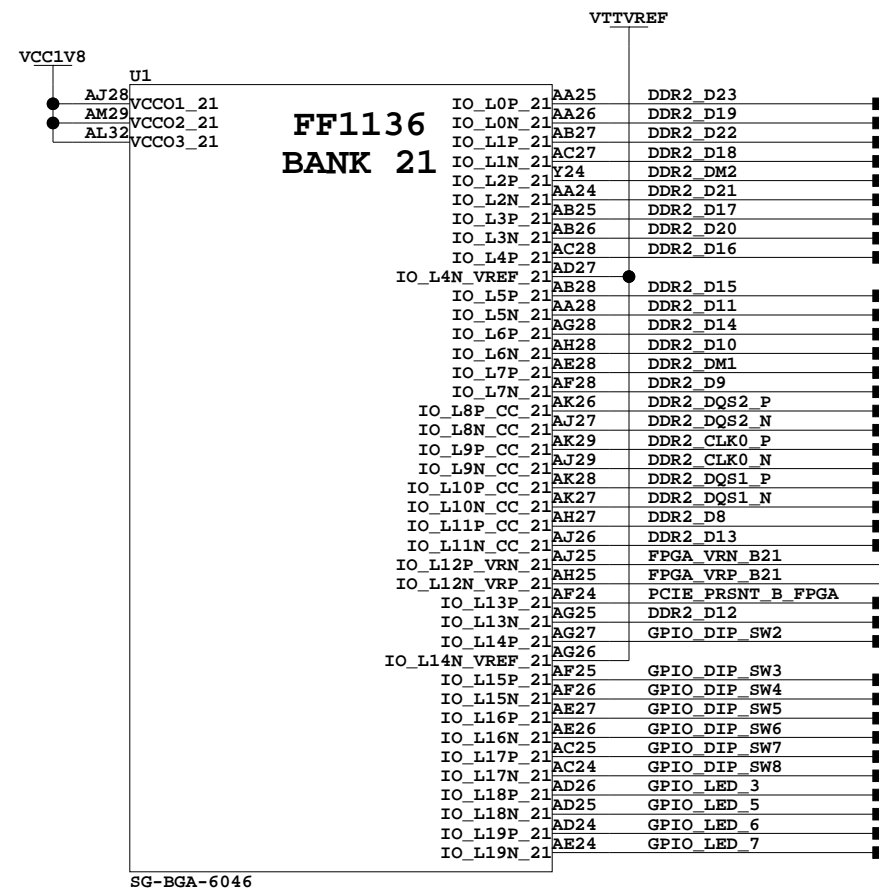
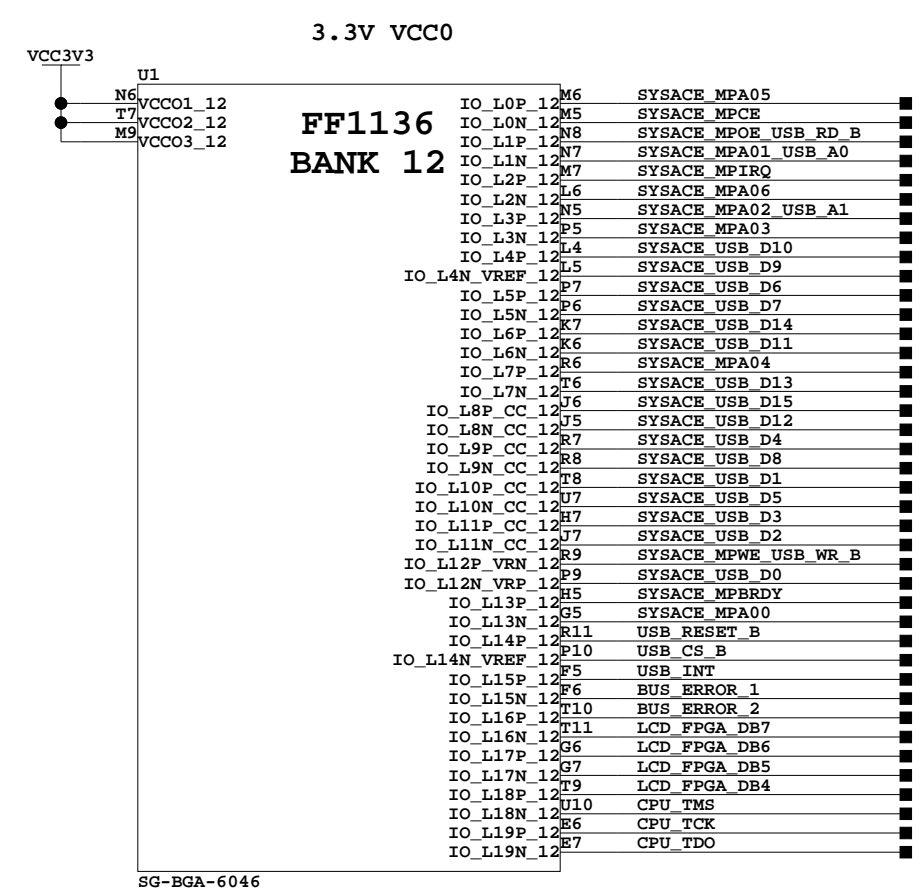
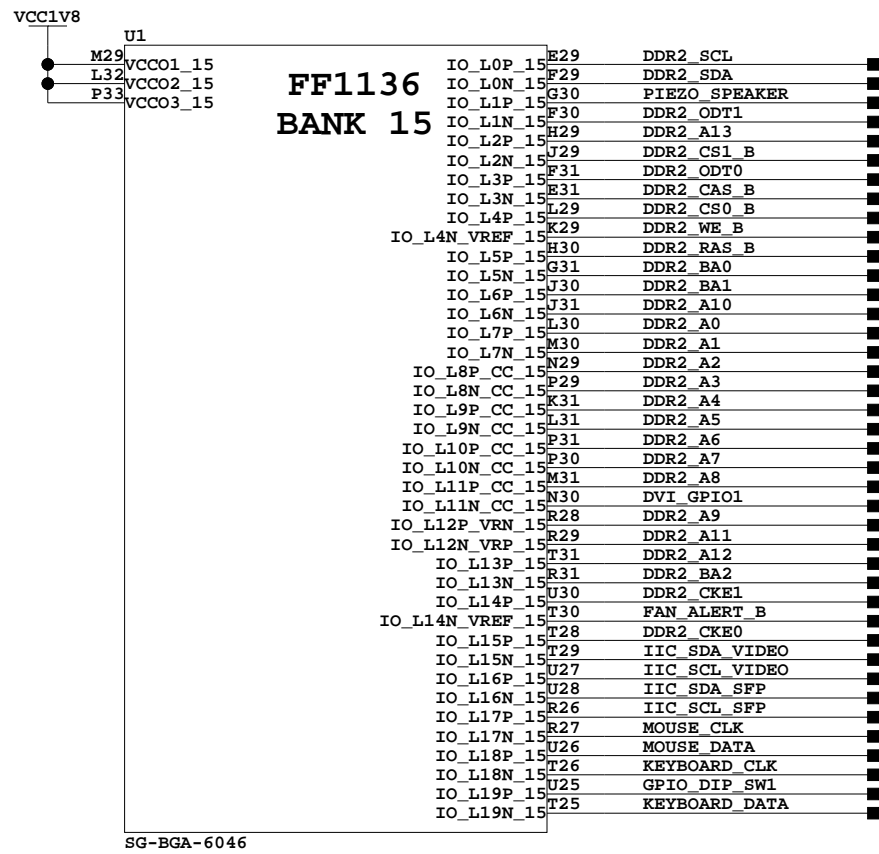
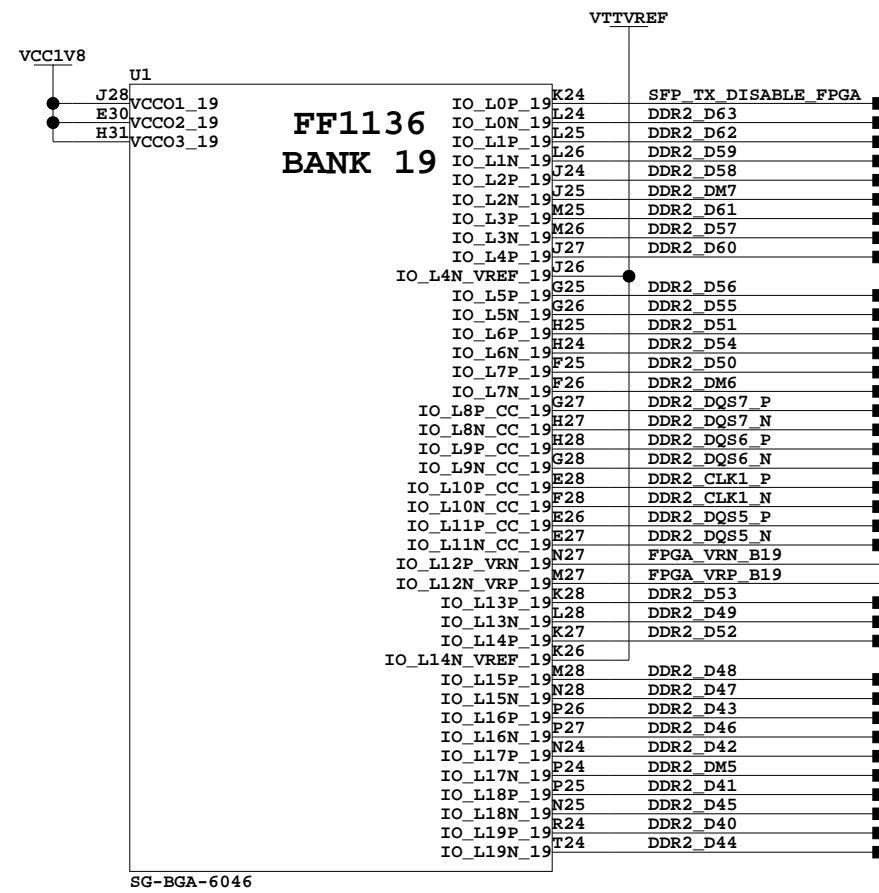
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet <b>1</b> of <b>27</b>	Drawn By BP



**Banks 0,1,2,3,4  
Config, FLASH, SRAM,  
GPIO, CLKs**



Title: FPGA Banks 0,1,2,3,4@config, FLASH, SRAM, GPIO, CLKs SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
Sheet 2 of 27	Drawn By BP	

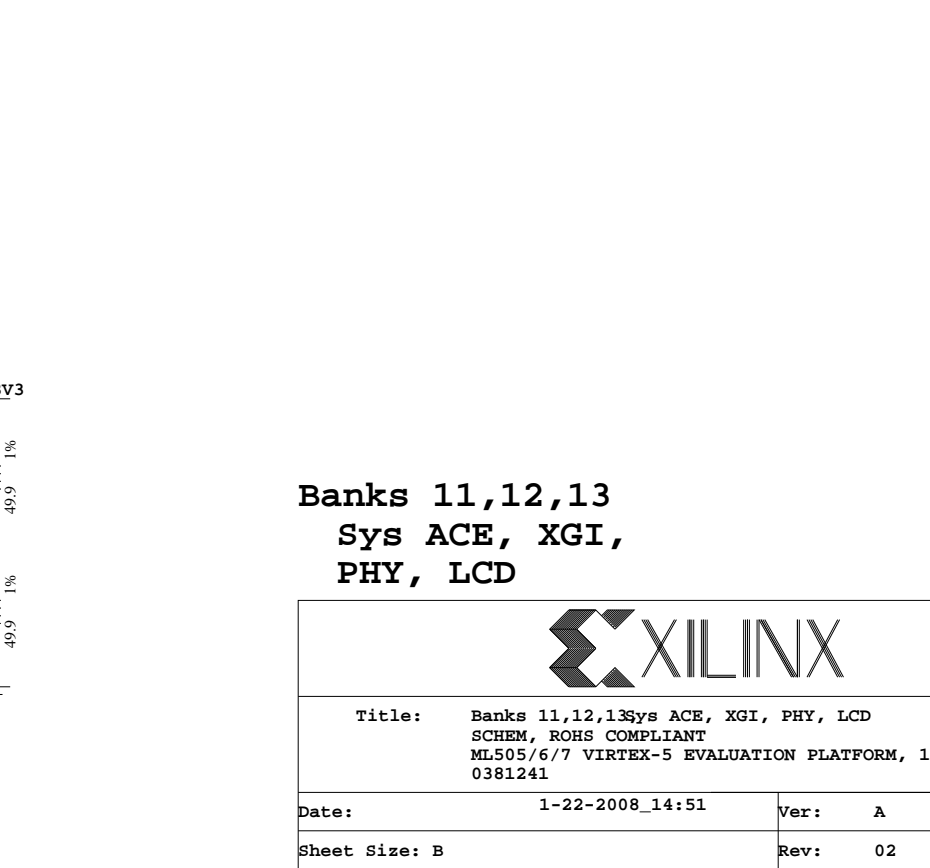
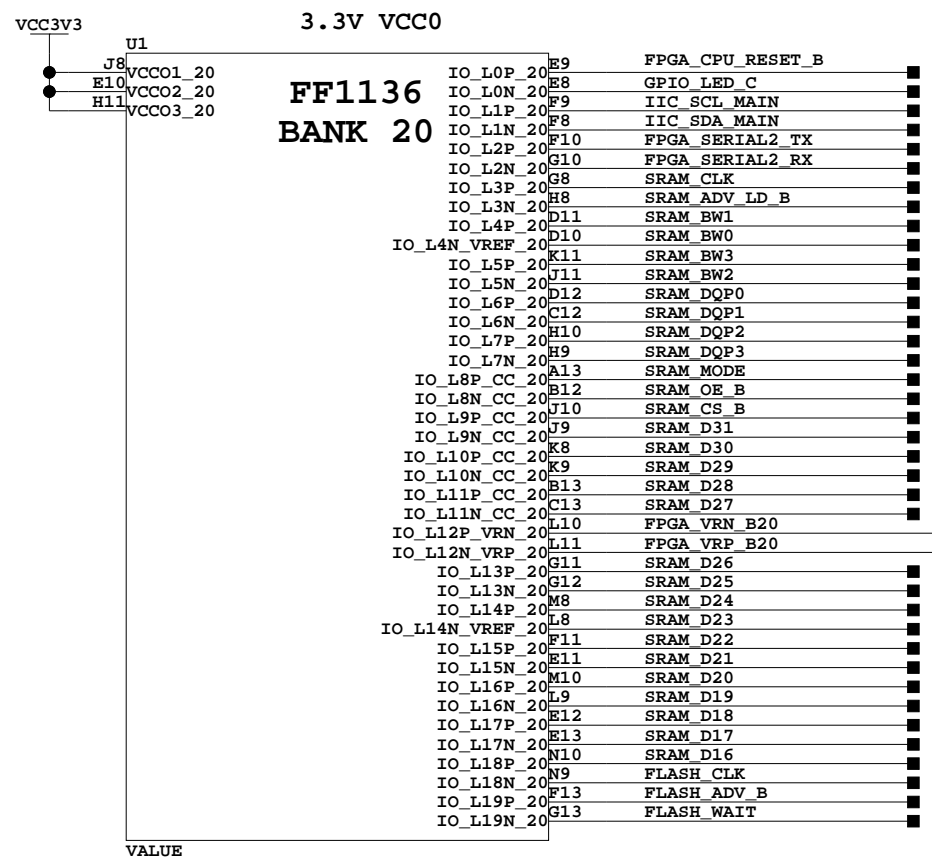
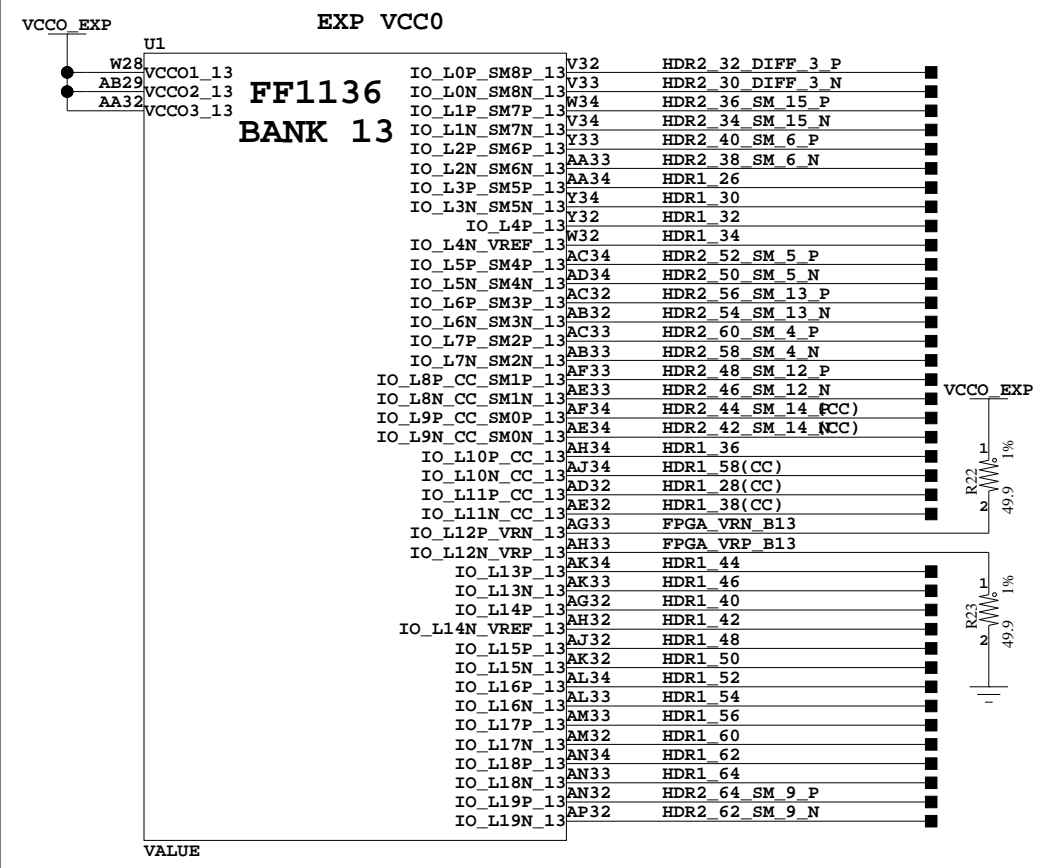
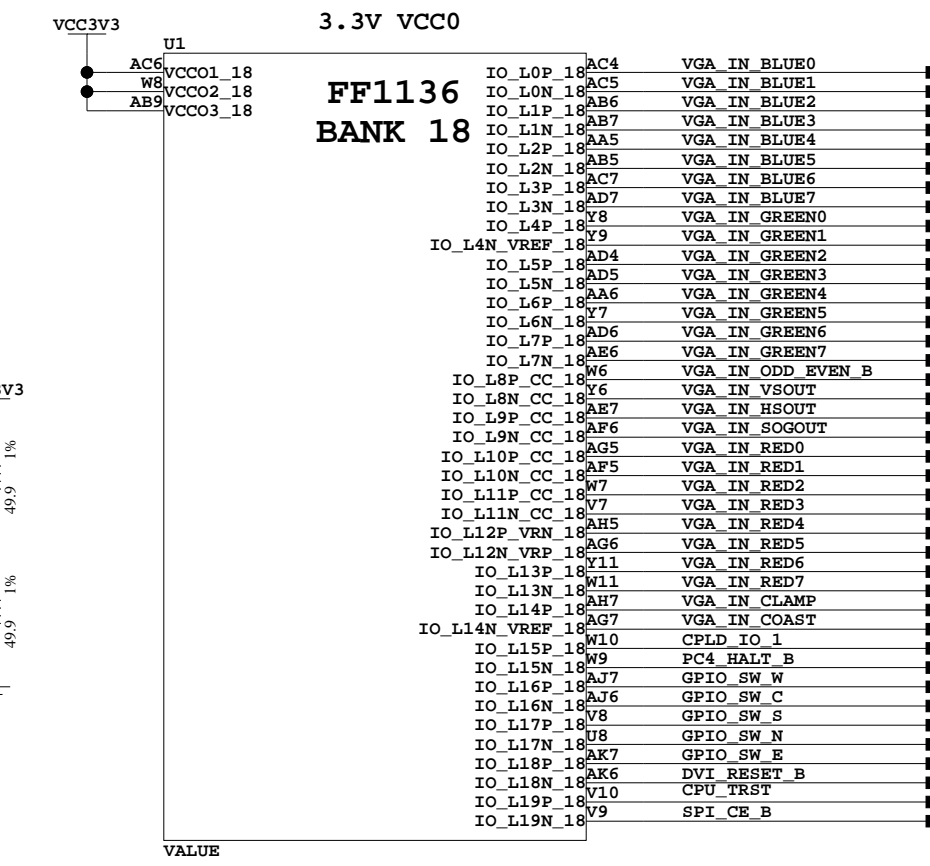
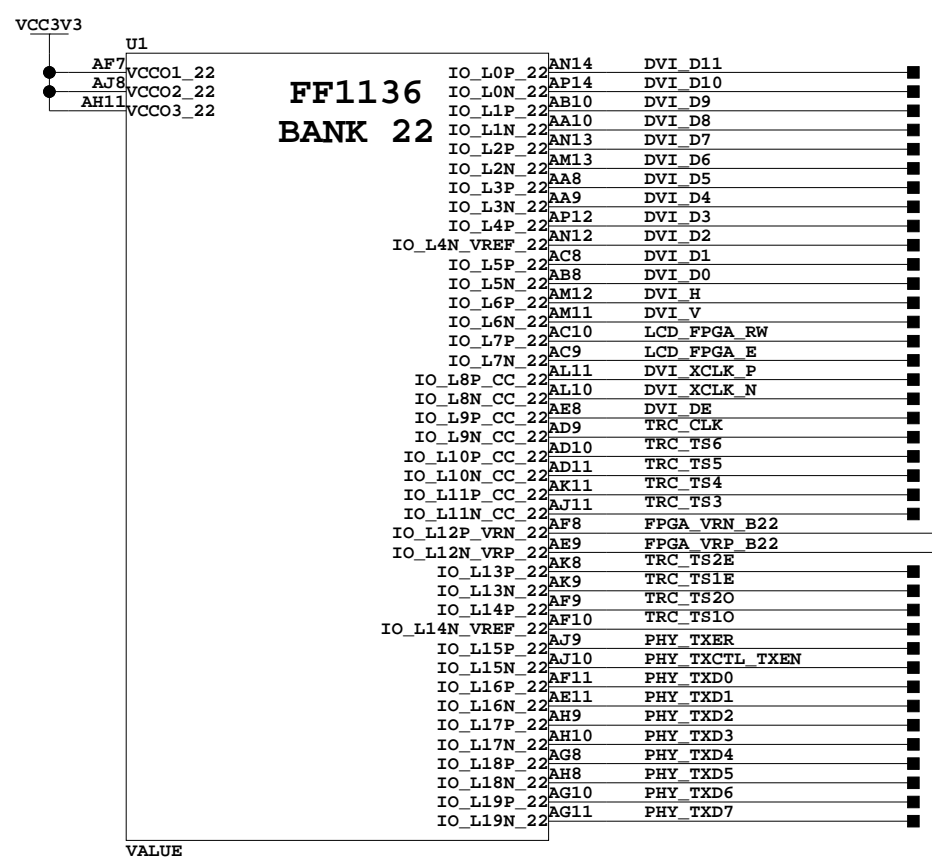
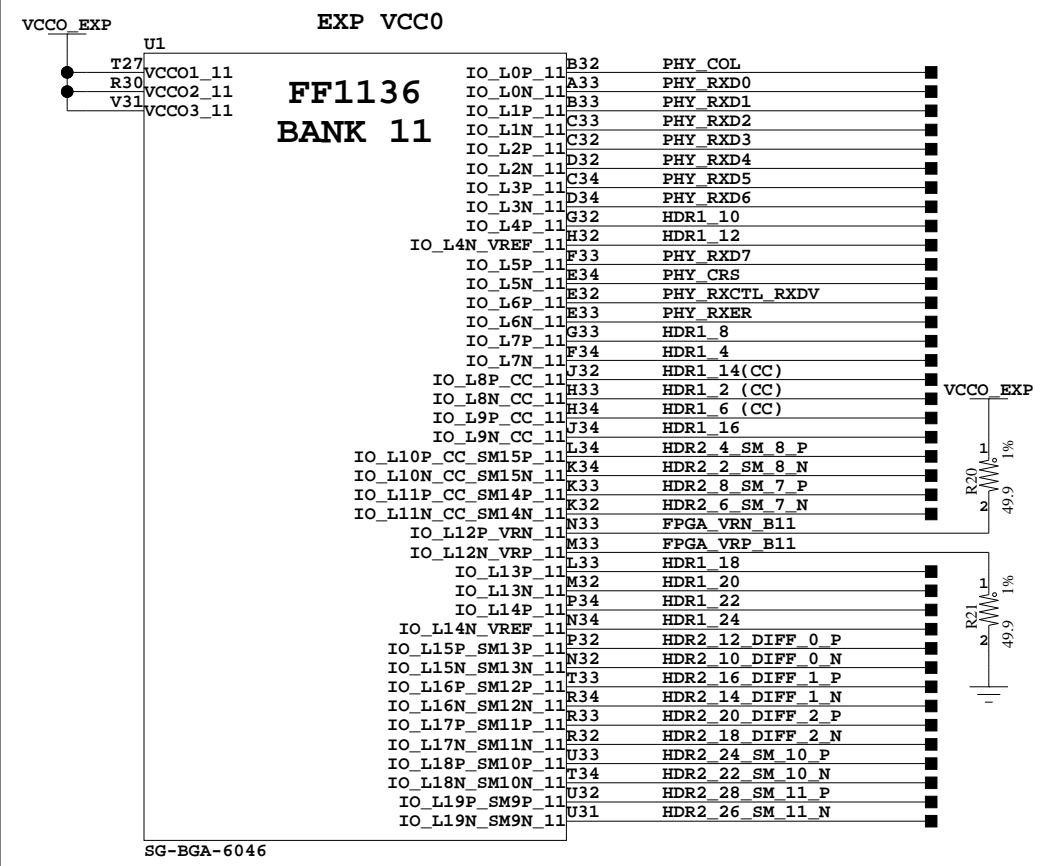


**Banks 14,16,18,21  
DDR2, PS2, GPIO**



Title: FPGA Bank 14, 16, 18, 21DDR2, PS2, GPIO  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
Sheet	3 of 27	Drawn By	BP



**Banks 11,12,13  
Sys ACE, XGI,  
PHY, LCD**

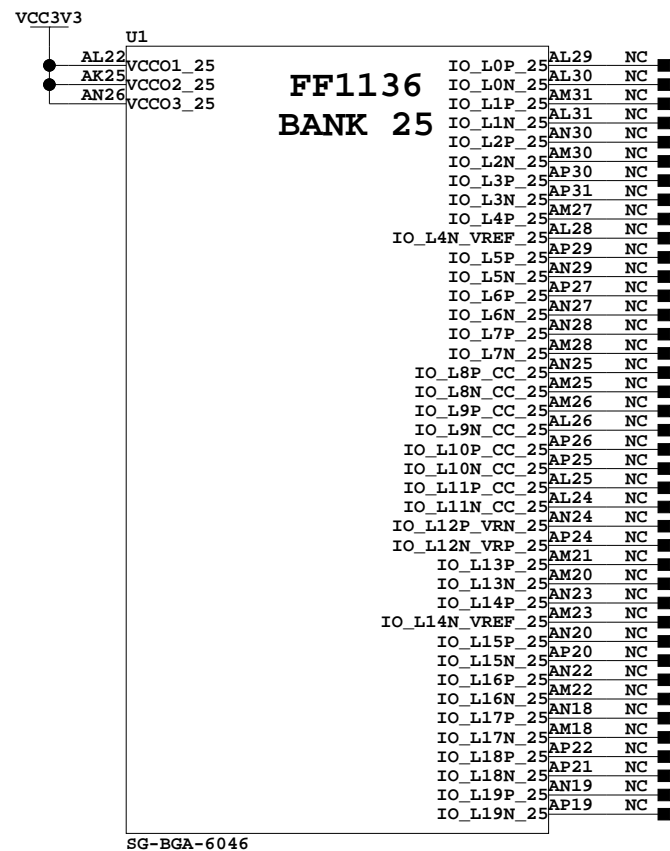
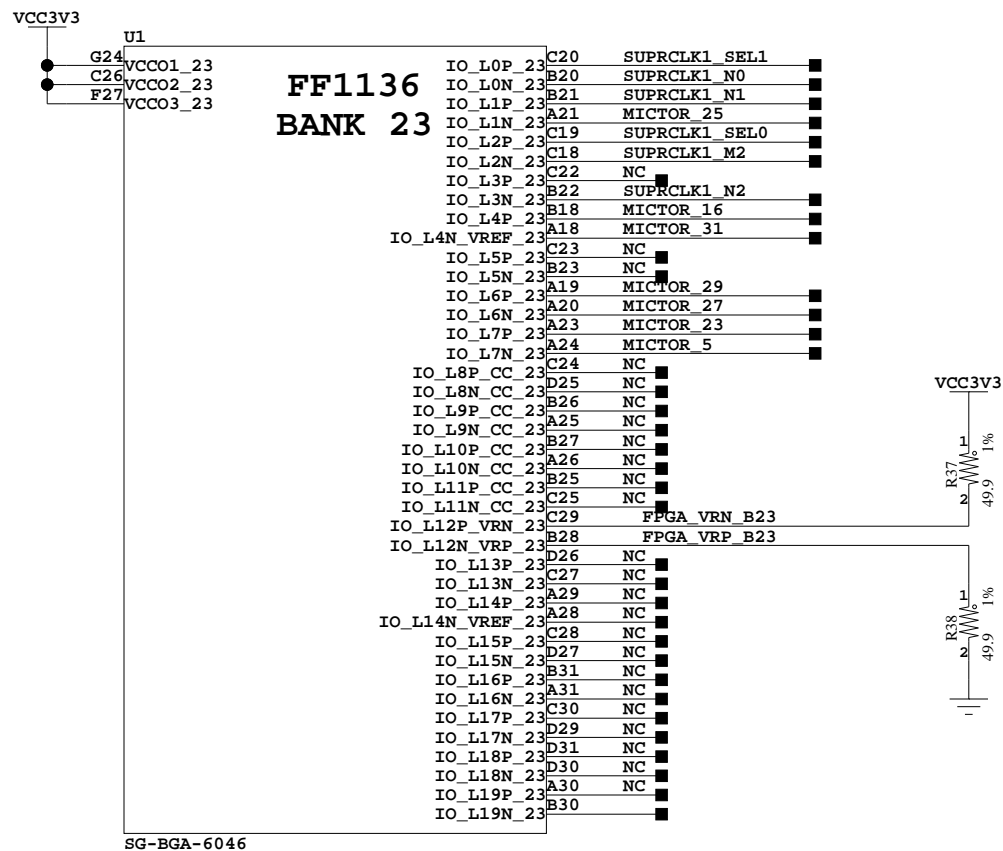
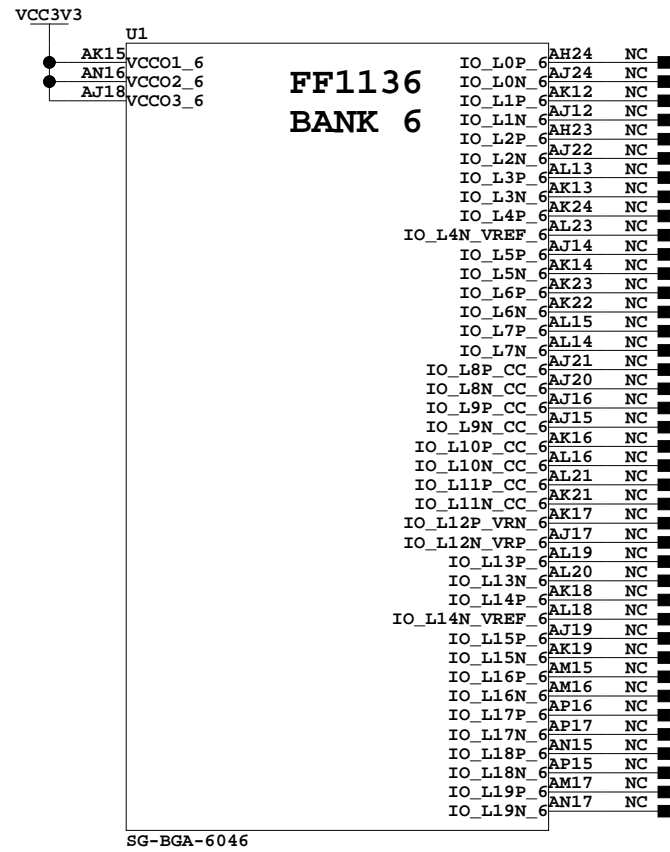
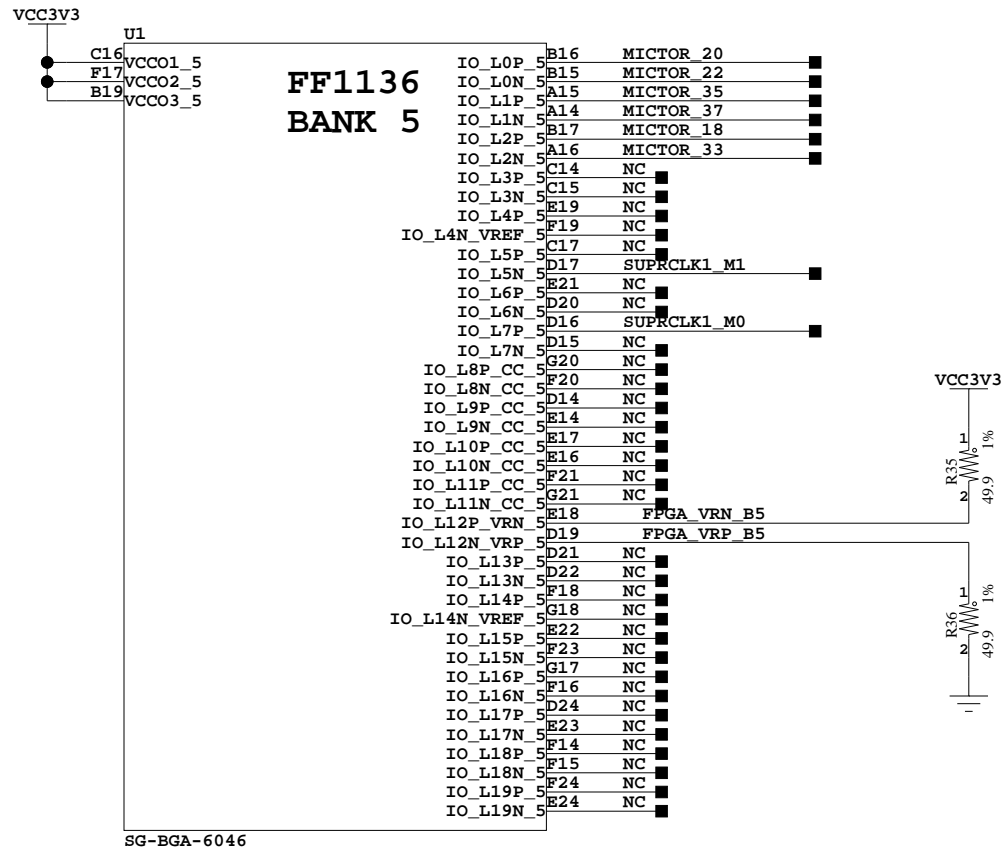
Title: Banks 11,12,13sys ACE, XGI, PHY, LCD  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

Date: 1-22-2008\_14:51 Ver: A

Sheet Size: B Rev: 02

Sheet **4** of **27** Drawn By BP

Unused banks on the LX50T and SX50T

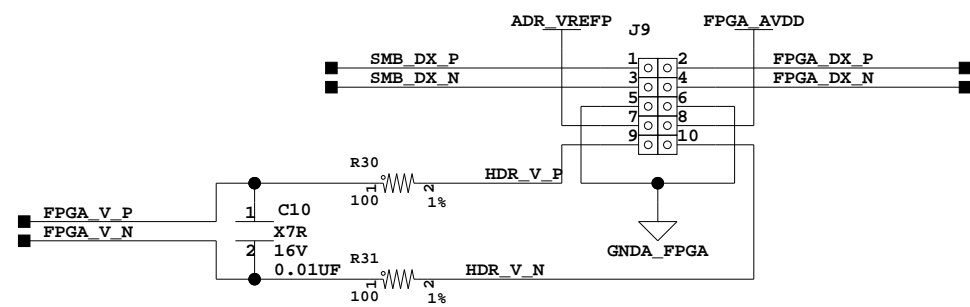


Banks 15, 17  
VGA, IIC, PHY  
SRAM, FLASH, GPIO

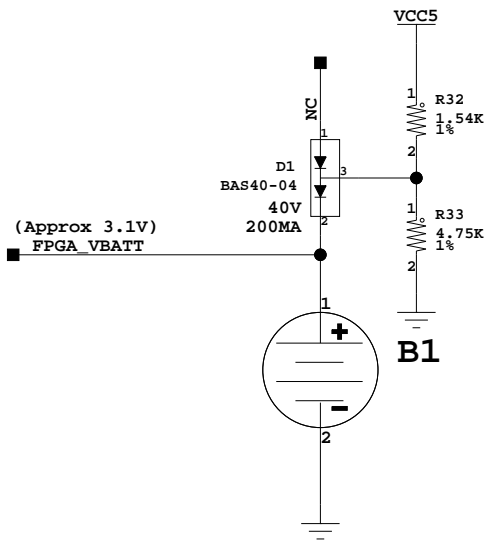


Title: Banks 11,12,13VGA, IIC, PHY, SRAM, GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 5 of 27	Drawn By BP

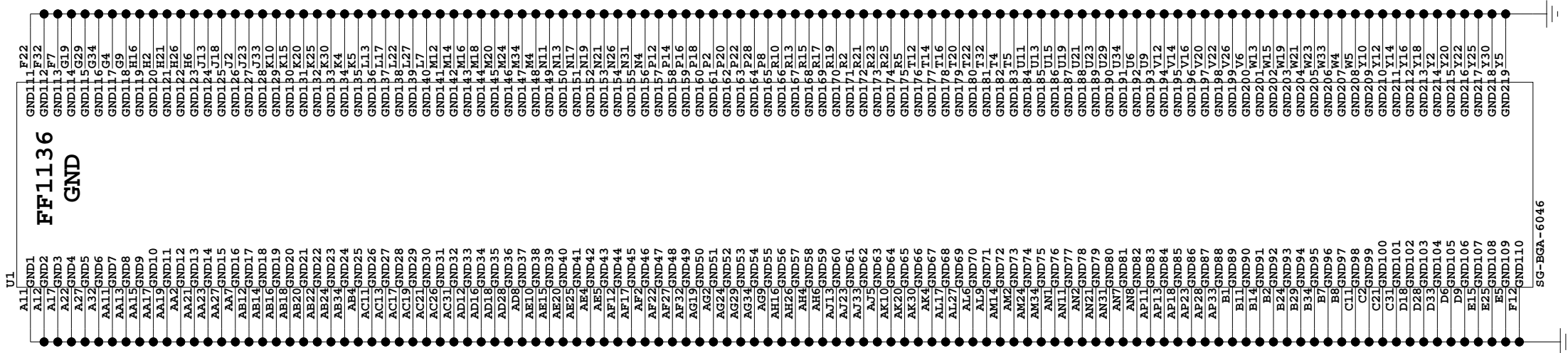
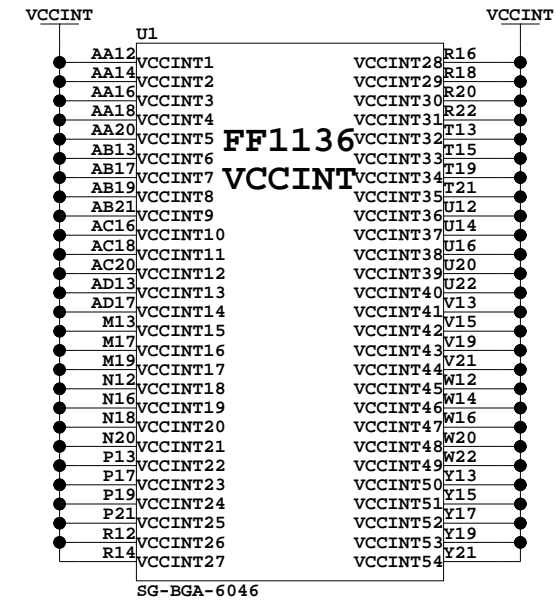
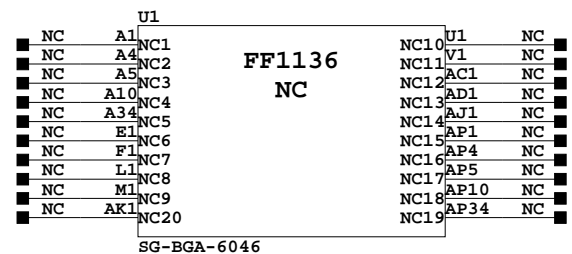
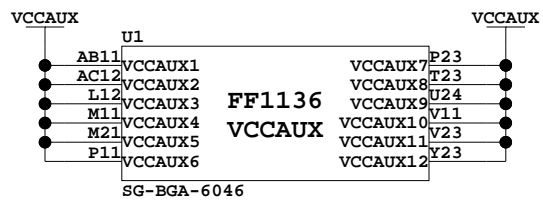
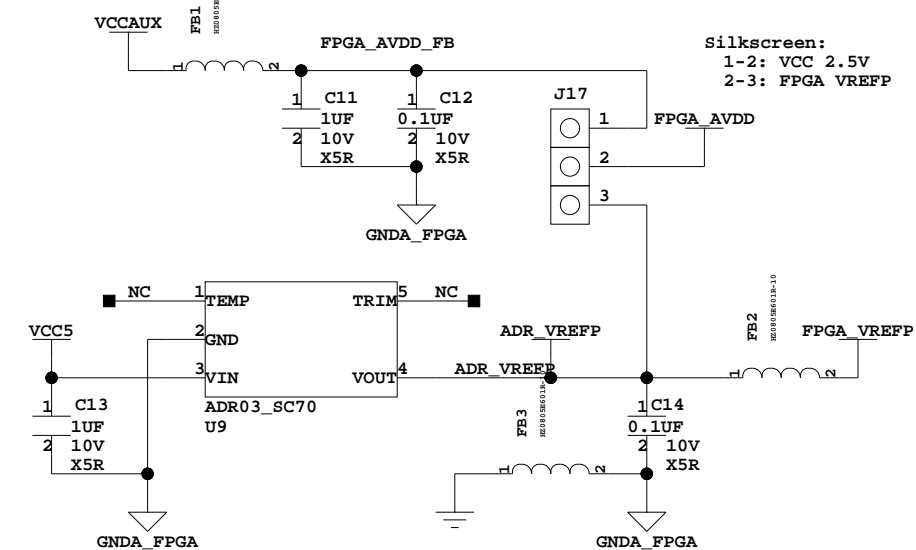
### System Monitor Header



### Rechargeable Battery



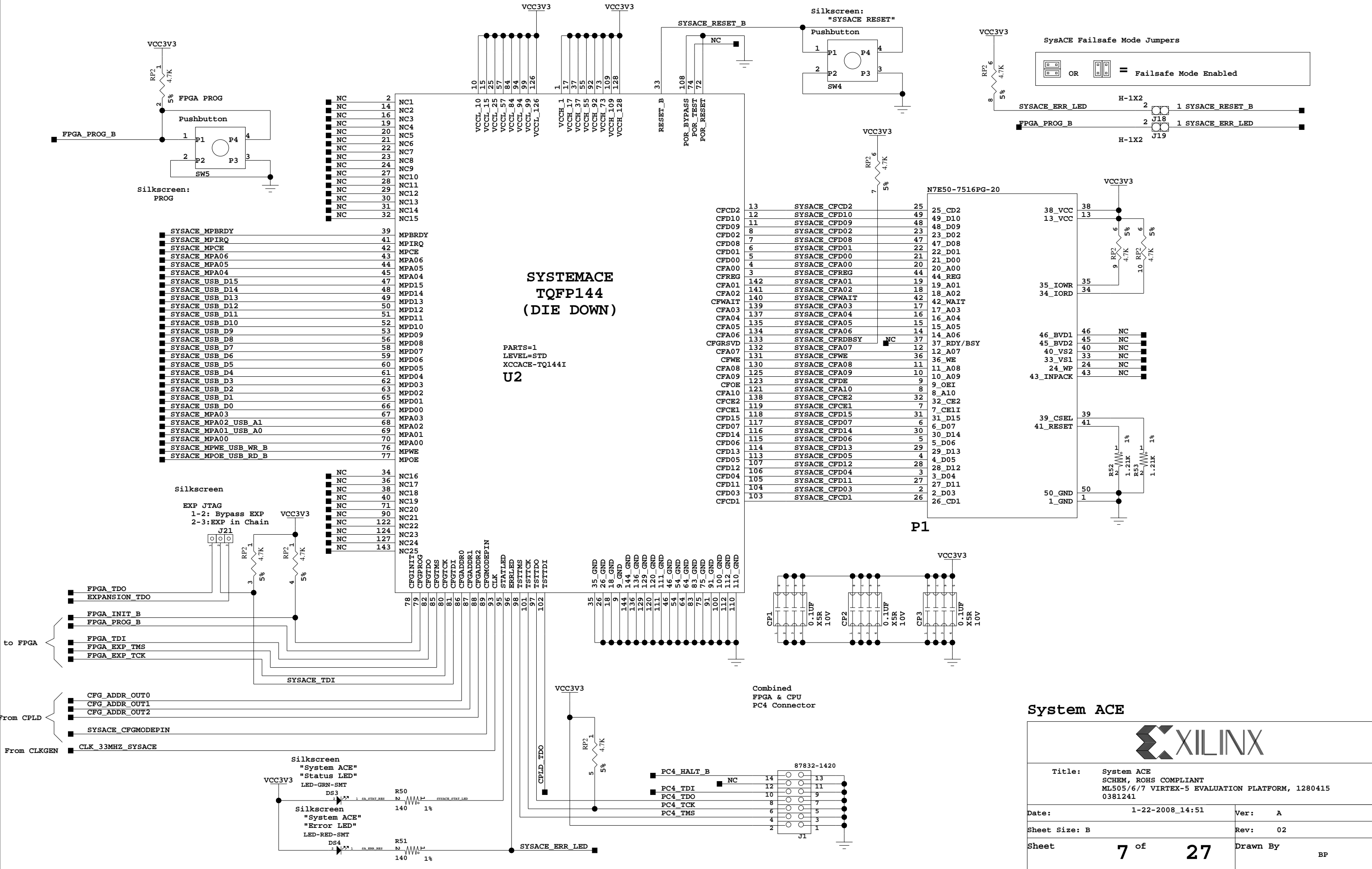
### FPGA AVDD Select



### Power and Misc FPGA Banks VCCINT, VCCAUX, NCs, GND Battery and System Monitor



Title: FPGA Misc, VCCINT, VCCAUX, GND, Sys Mon SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
Sheet 6 of 27	Drawn By	BP



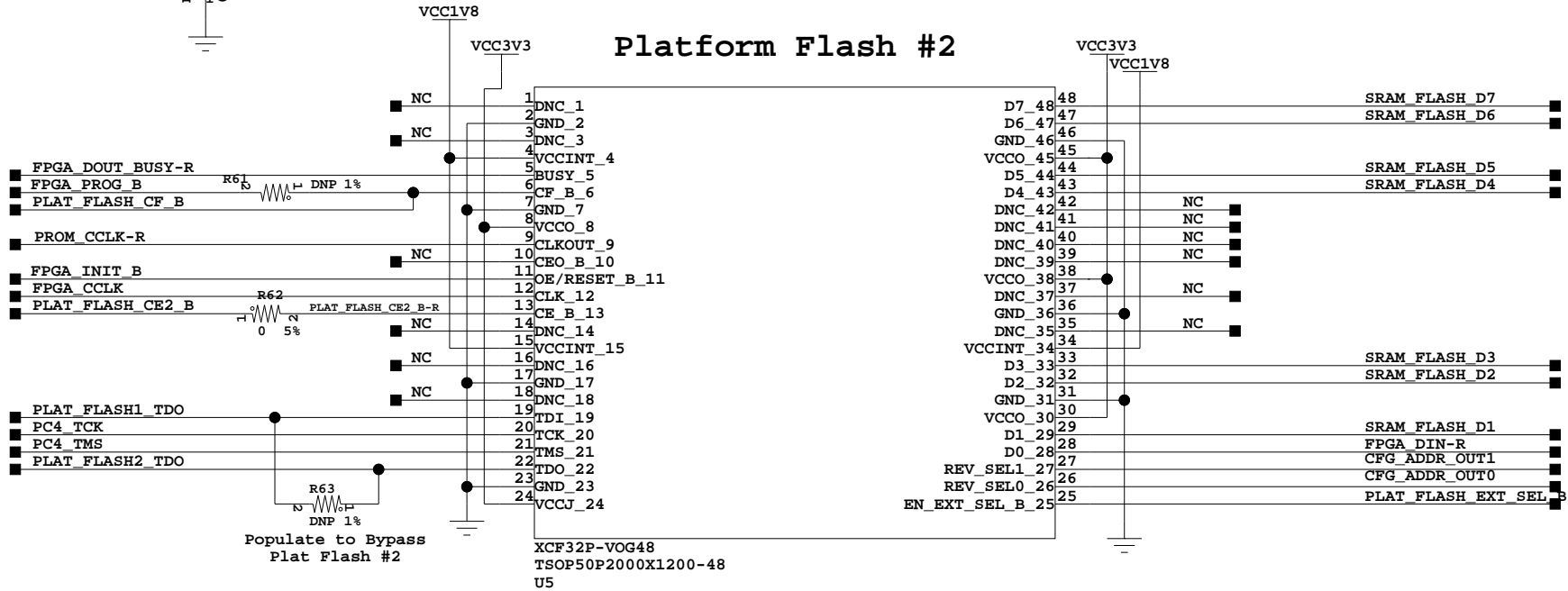
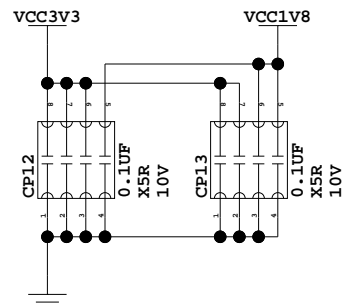
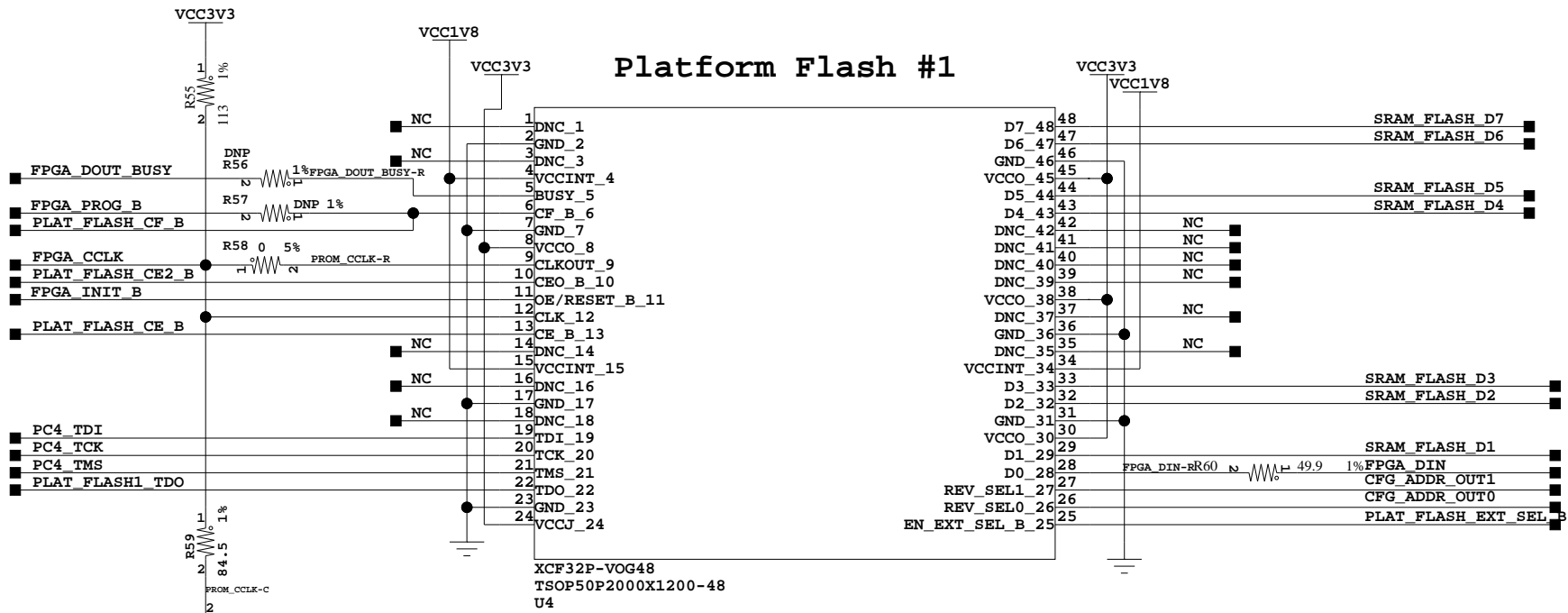
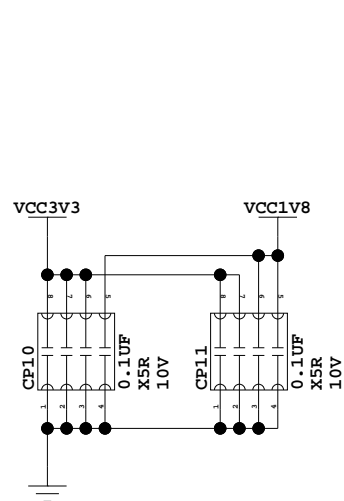
## System ACE

**Title:** System ACE  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

**Date:** 1-22-2008\_14:51     **Ver:** A

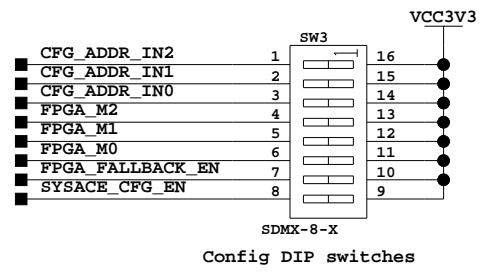
**Sheet Size:** B     **Rev:** 02

**Sheet** 7 of 27     **Drawn By** BP

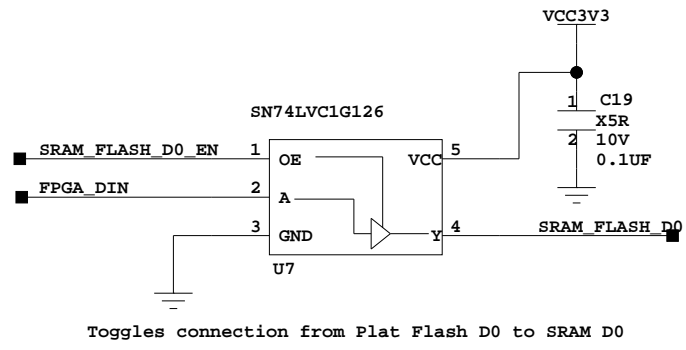


Populate to Bypass Plat Flash #2

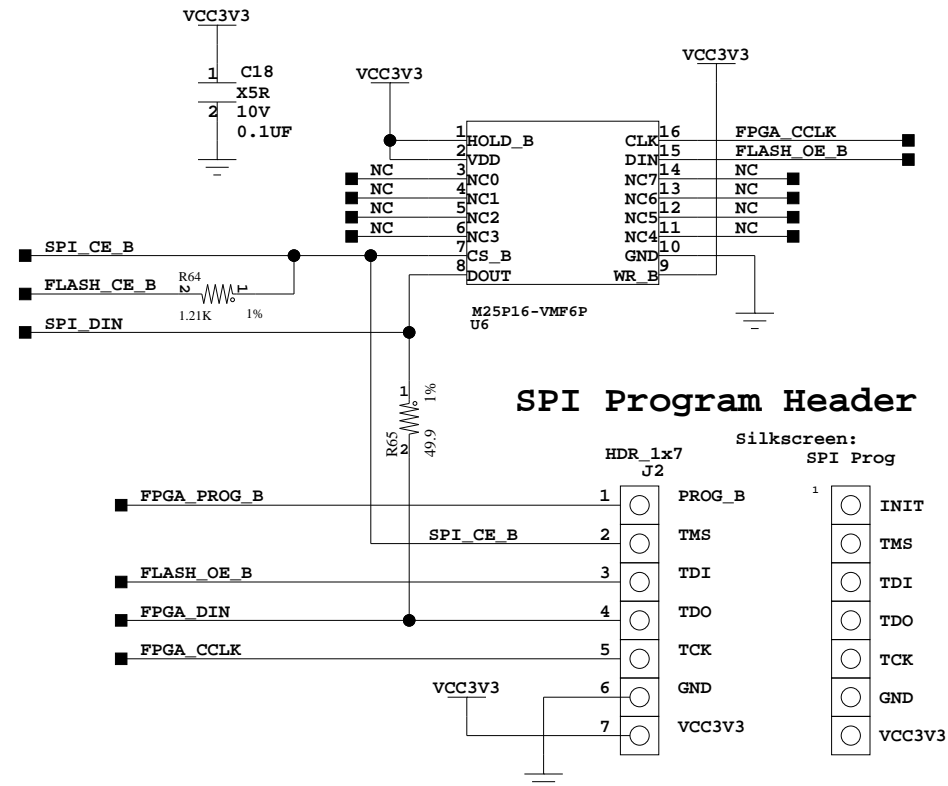
Silkscreen:  
SysACE Config, Mode pins



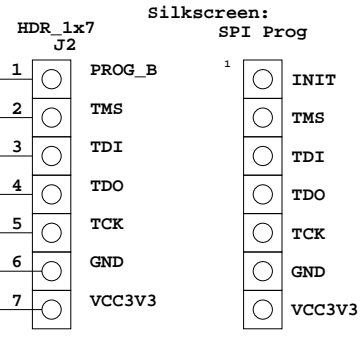
Config DIP switches



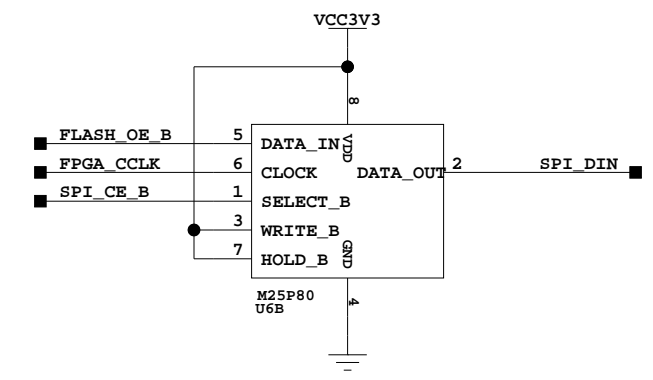
Toggles connection from Plat Flash D0 to SRAM D0



SPI Program Header



SPI Flash



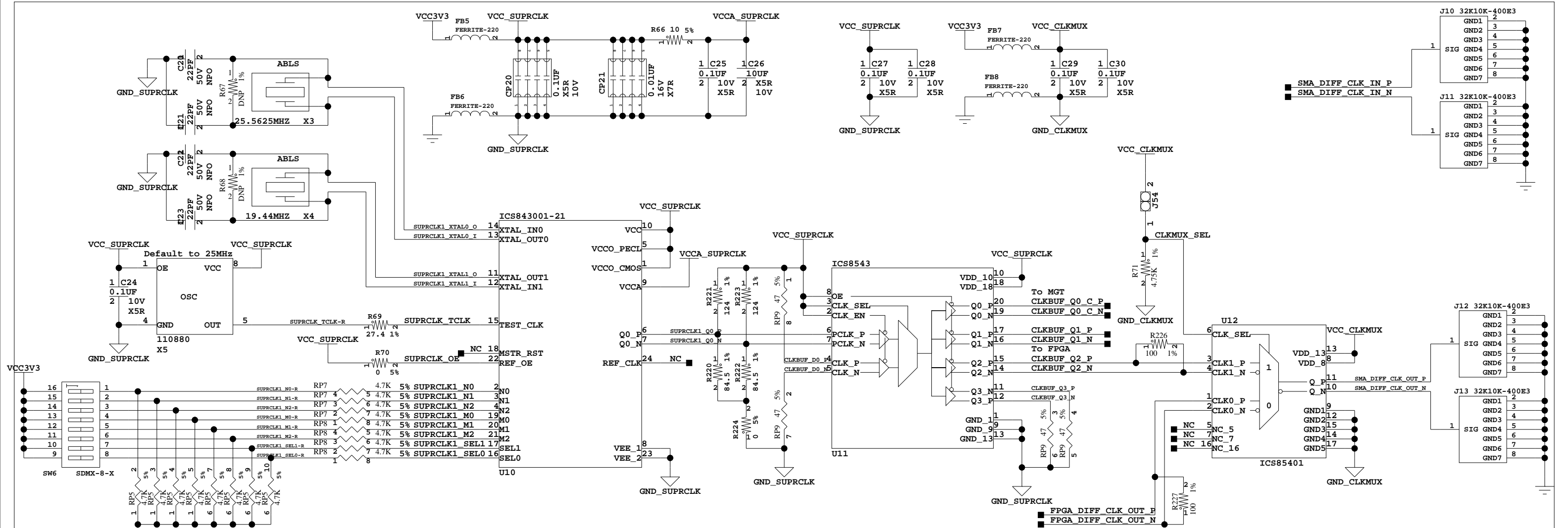
Misc Config  
Platform Flash,  
SPI Flash



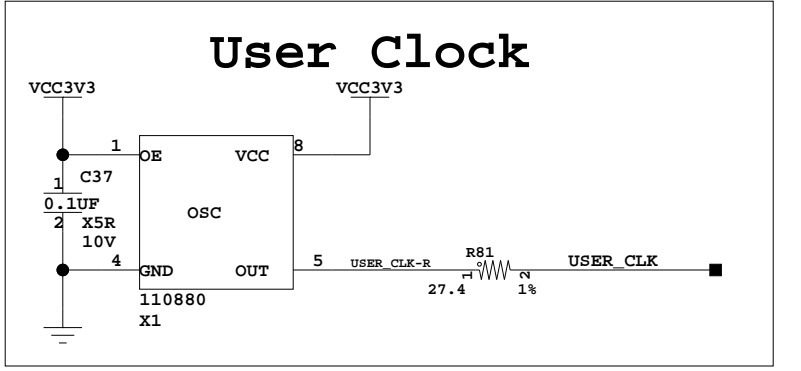
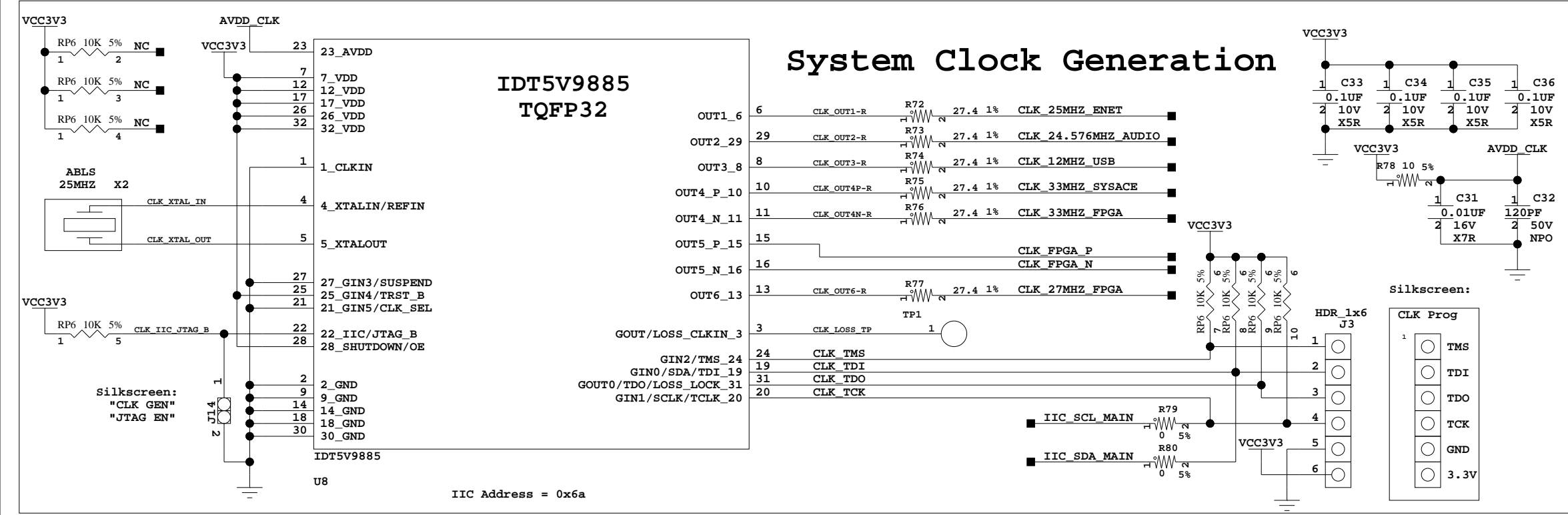
Title: Misc Config, Platform Flash, SPI Flash  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
Sheet	8 of 27	Drawn By	BP





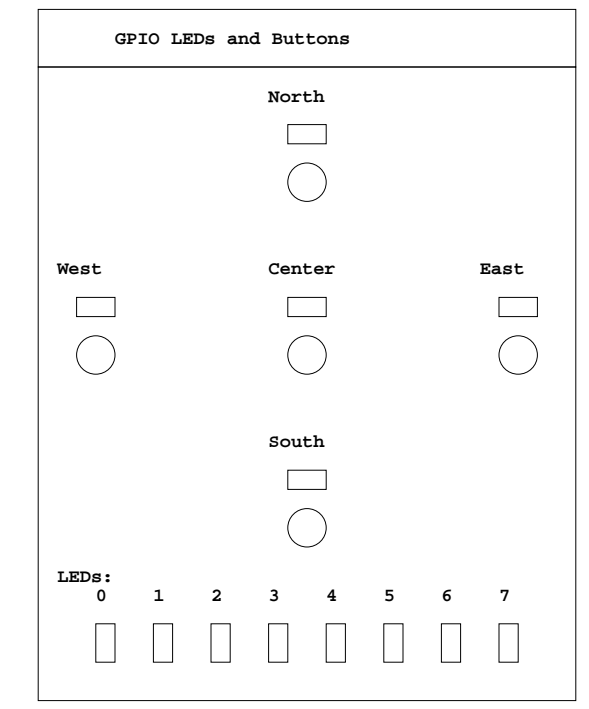
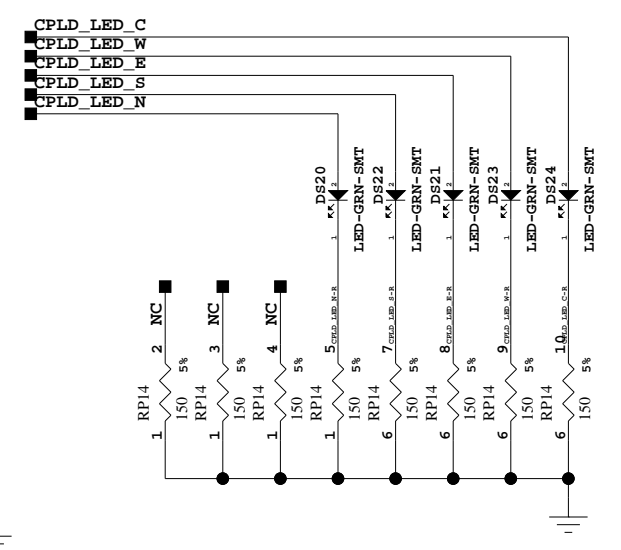
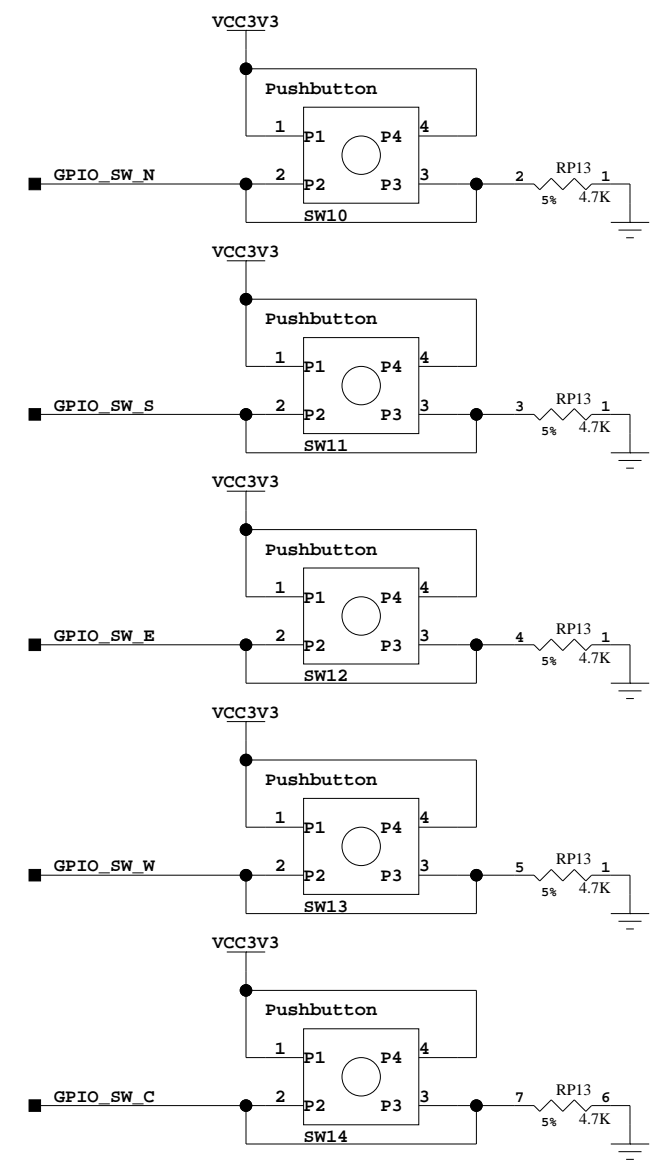
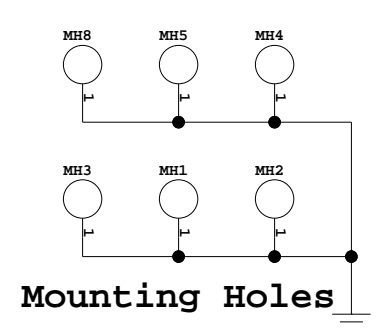
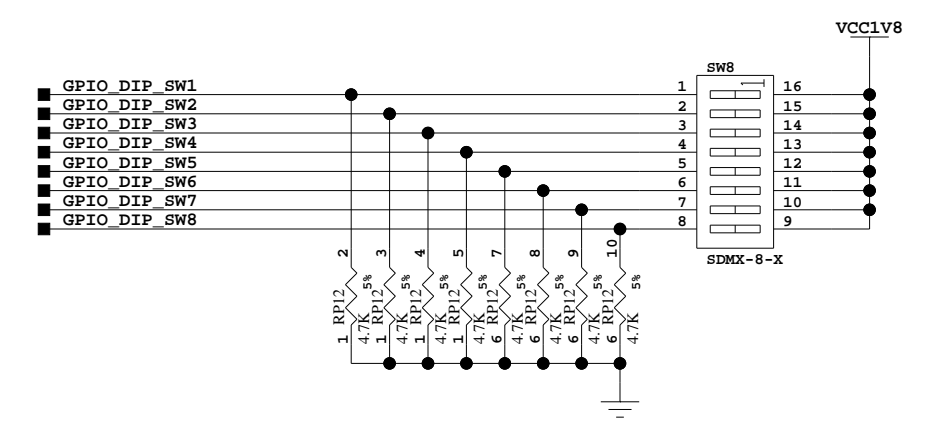
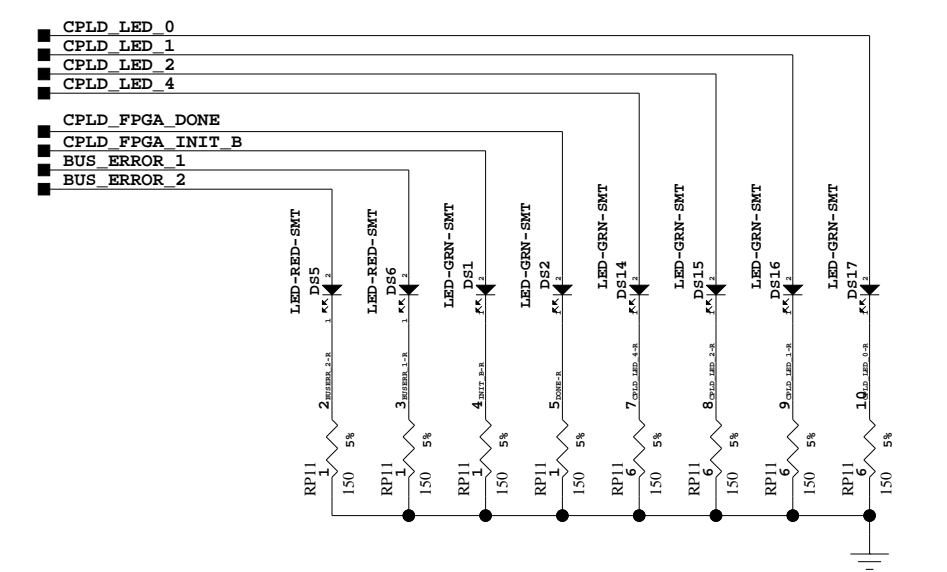
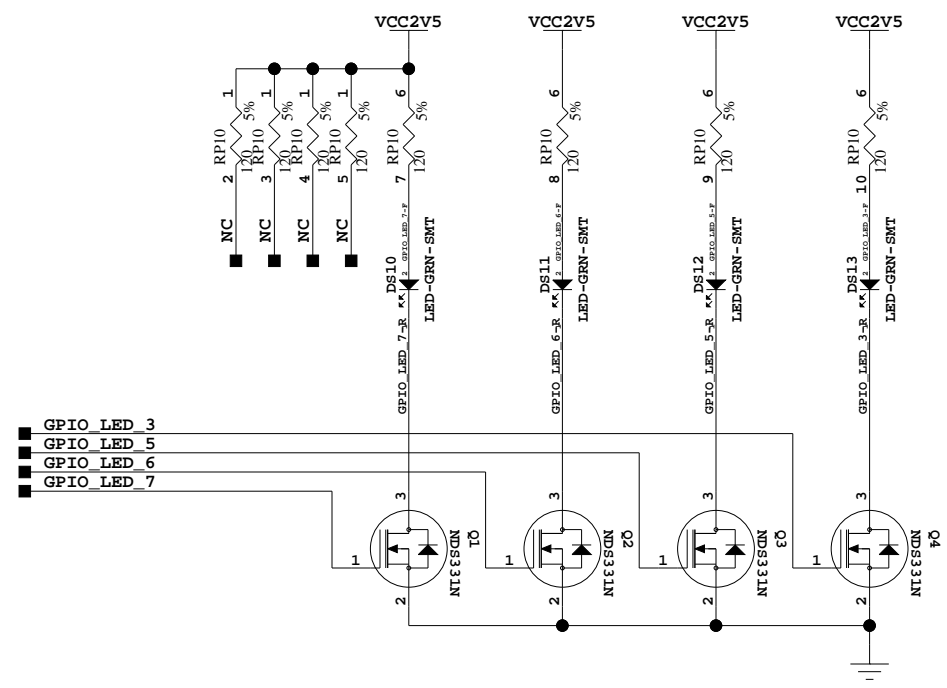
**Diff Clocks: SMAs, Generation, MUX and Buffer**



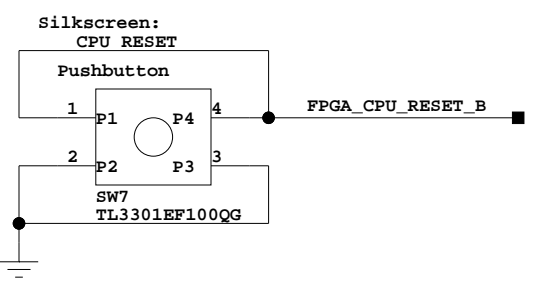
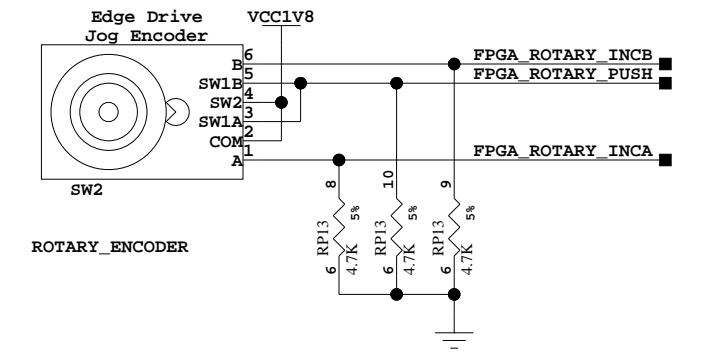
**Clocking - Differential Clock, System Clock & User Clock**



Title: Differential Clock, System Clock, User Clock SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 9 of 27	Drawn By BP



### Edge Drive Jog Encoder Switch

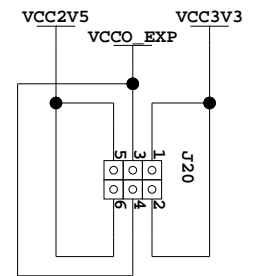
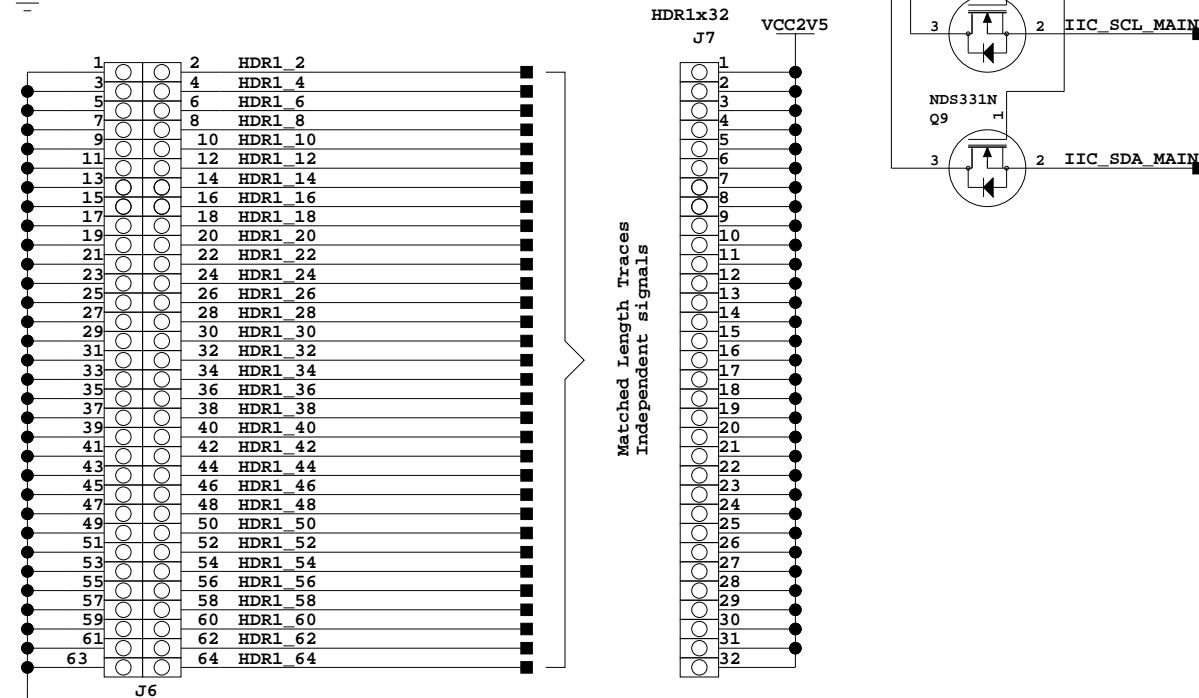
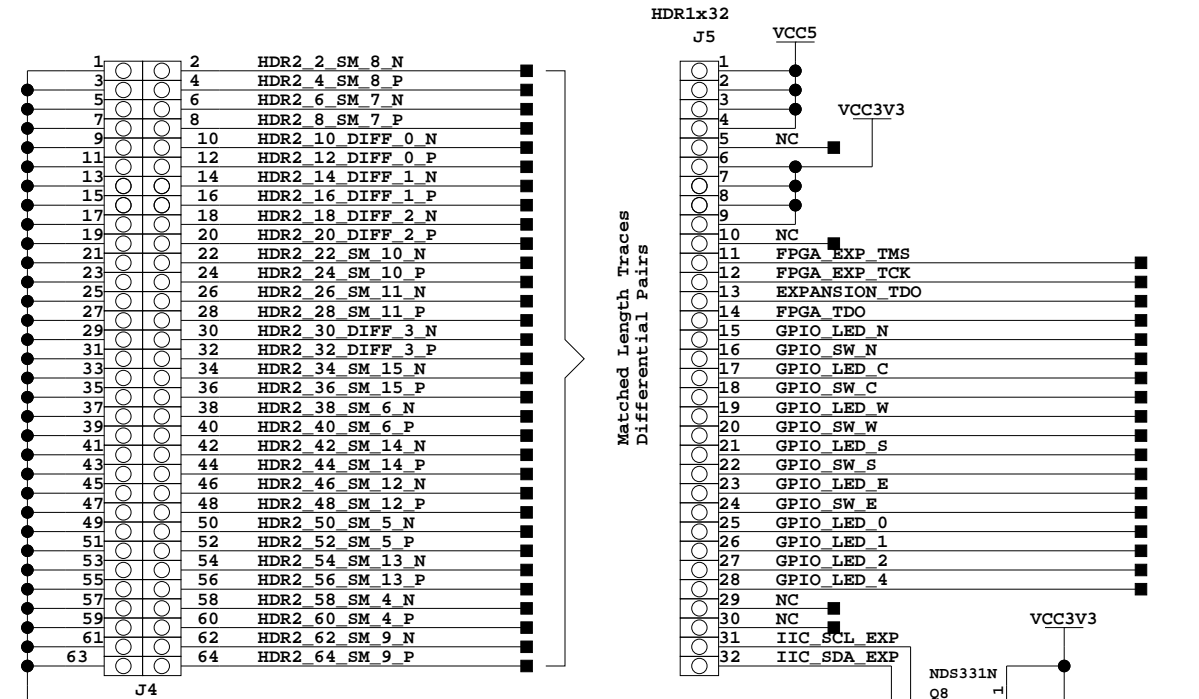


### GPIO - Buttons, LEDs, Switches



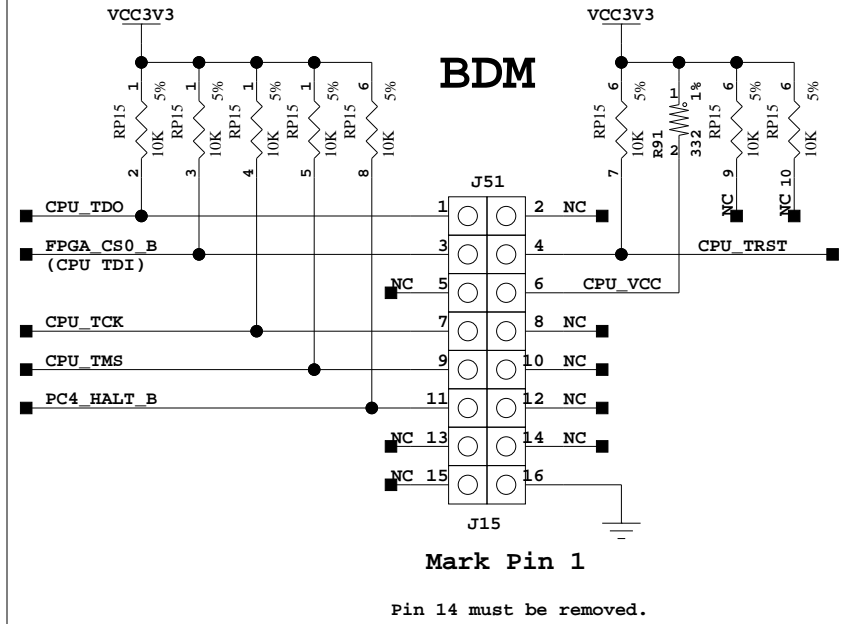
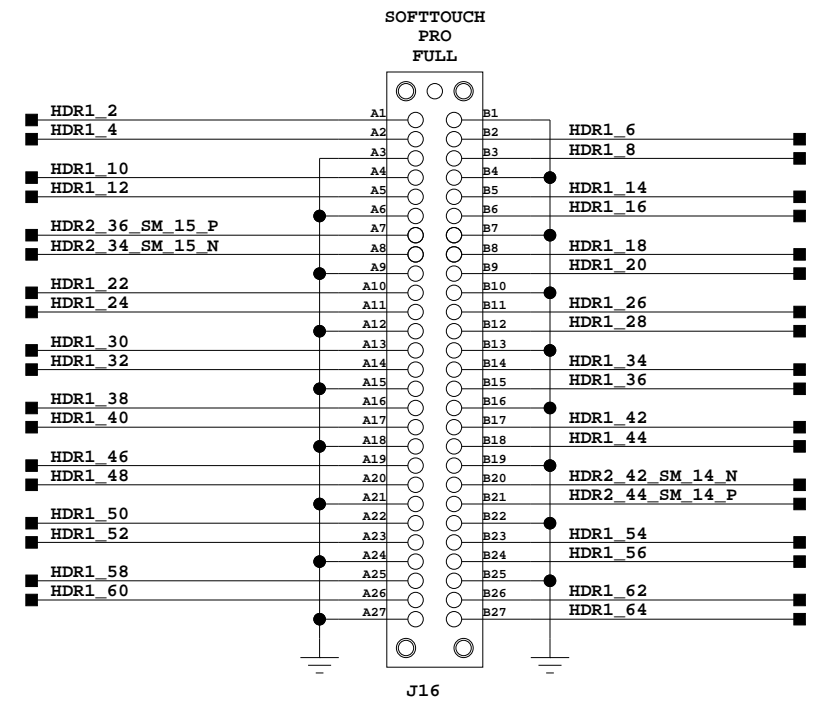
Title: GPIO Buttons, LEDs, Switches SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
Sheet 10 of 27	Drawn By	BP

# XGI Expansion Interface



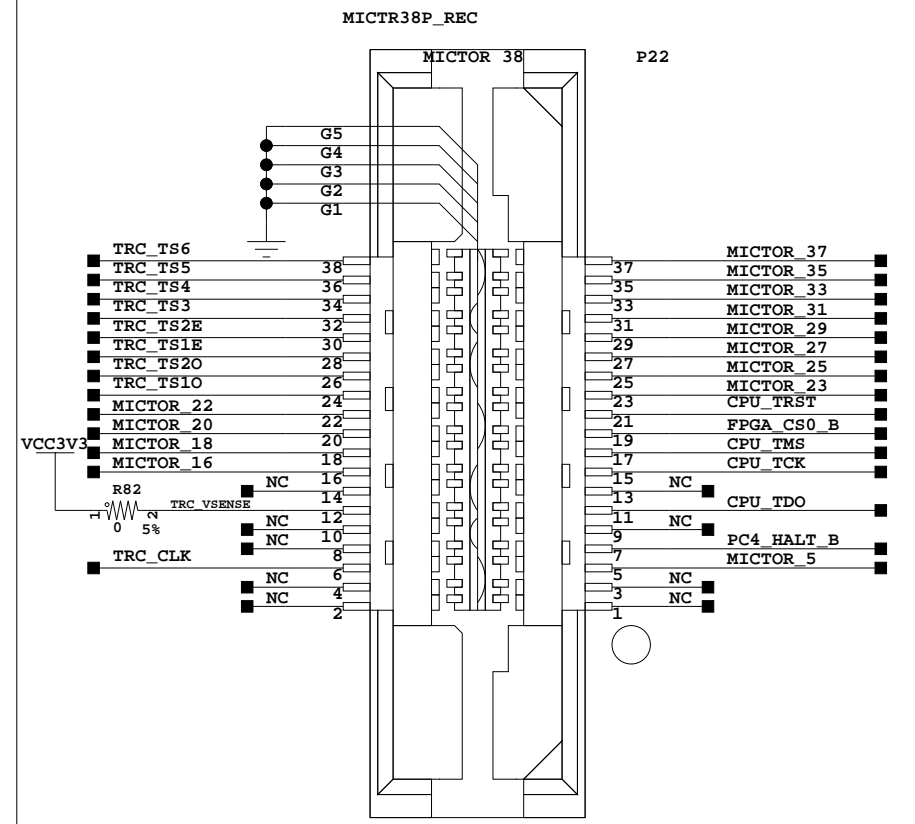
Bank 11/13 Expansion Connector Voltage  
 1-3 & 2-4 = 3.3V  
 3-5 & 4-6 = 2.5V

# SoftTouch Pro



Mark Pin 1  
 Pin 14 must be removed.

# Mictor

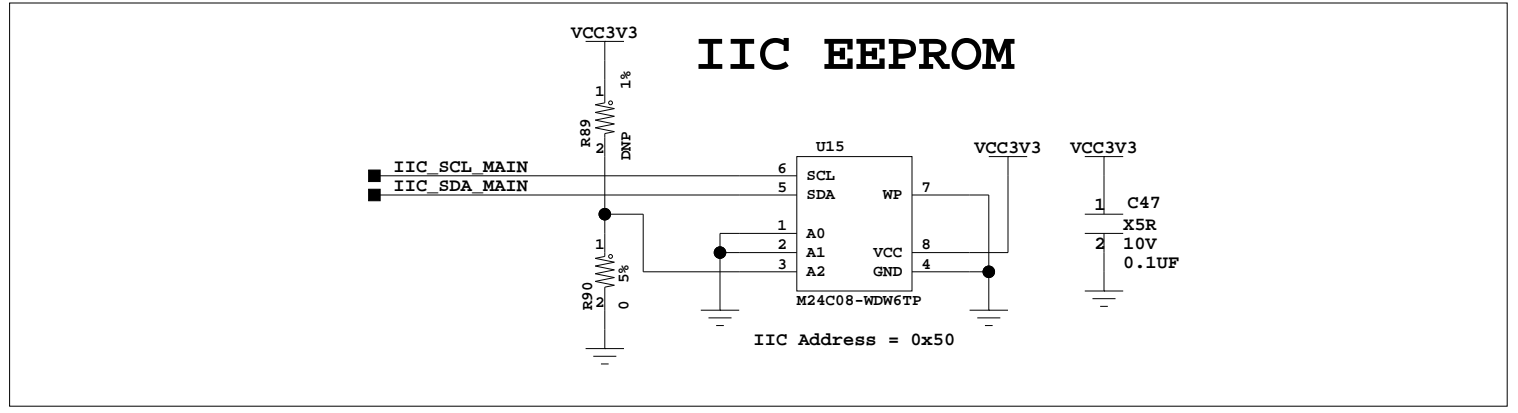
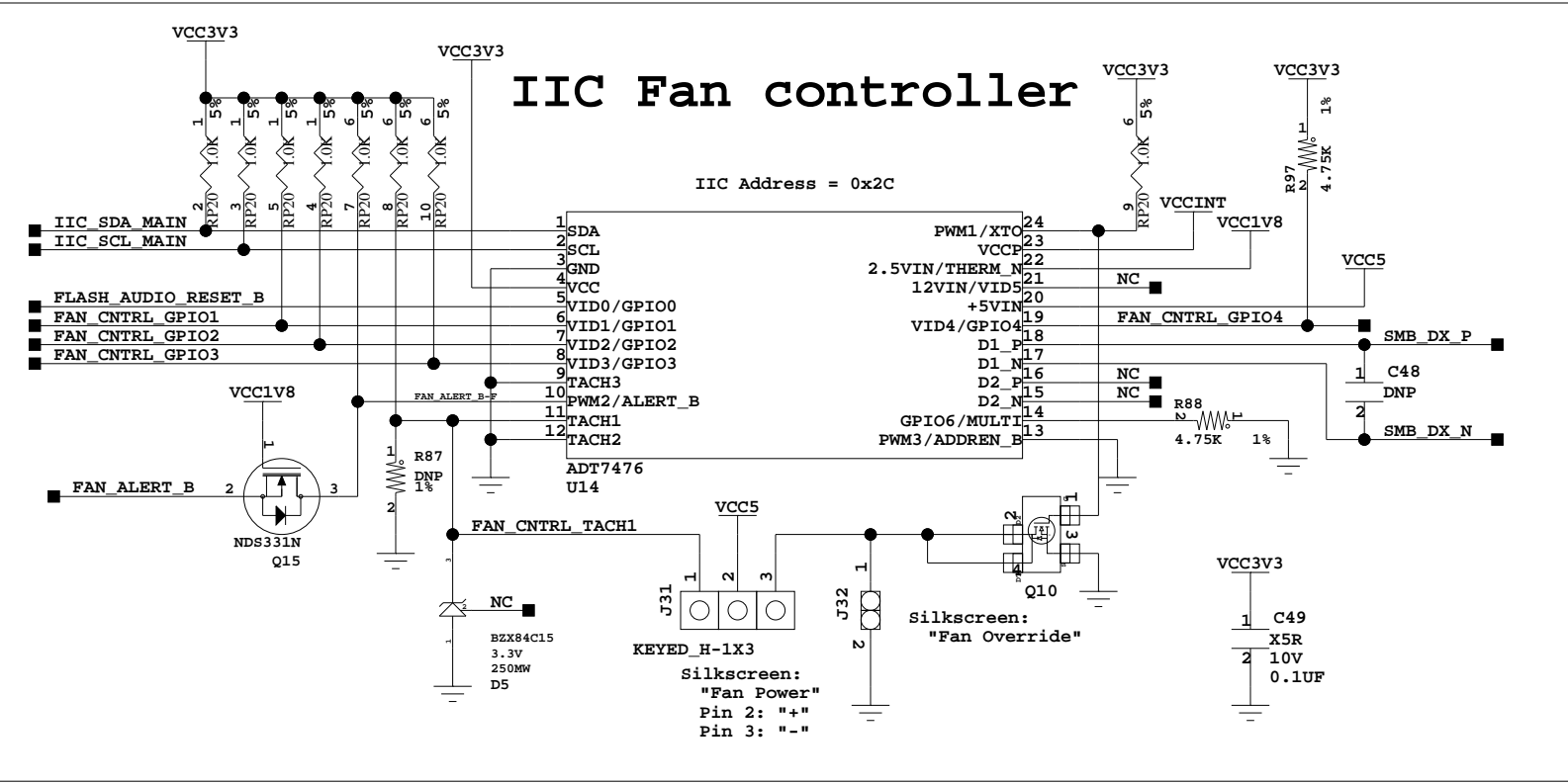
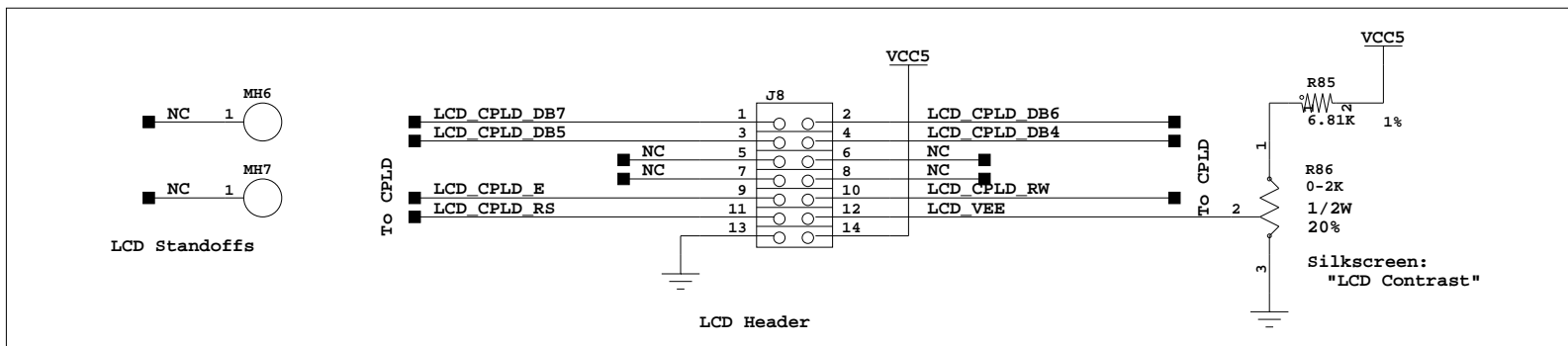
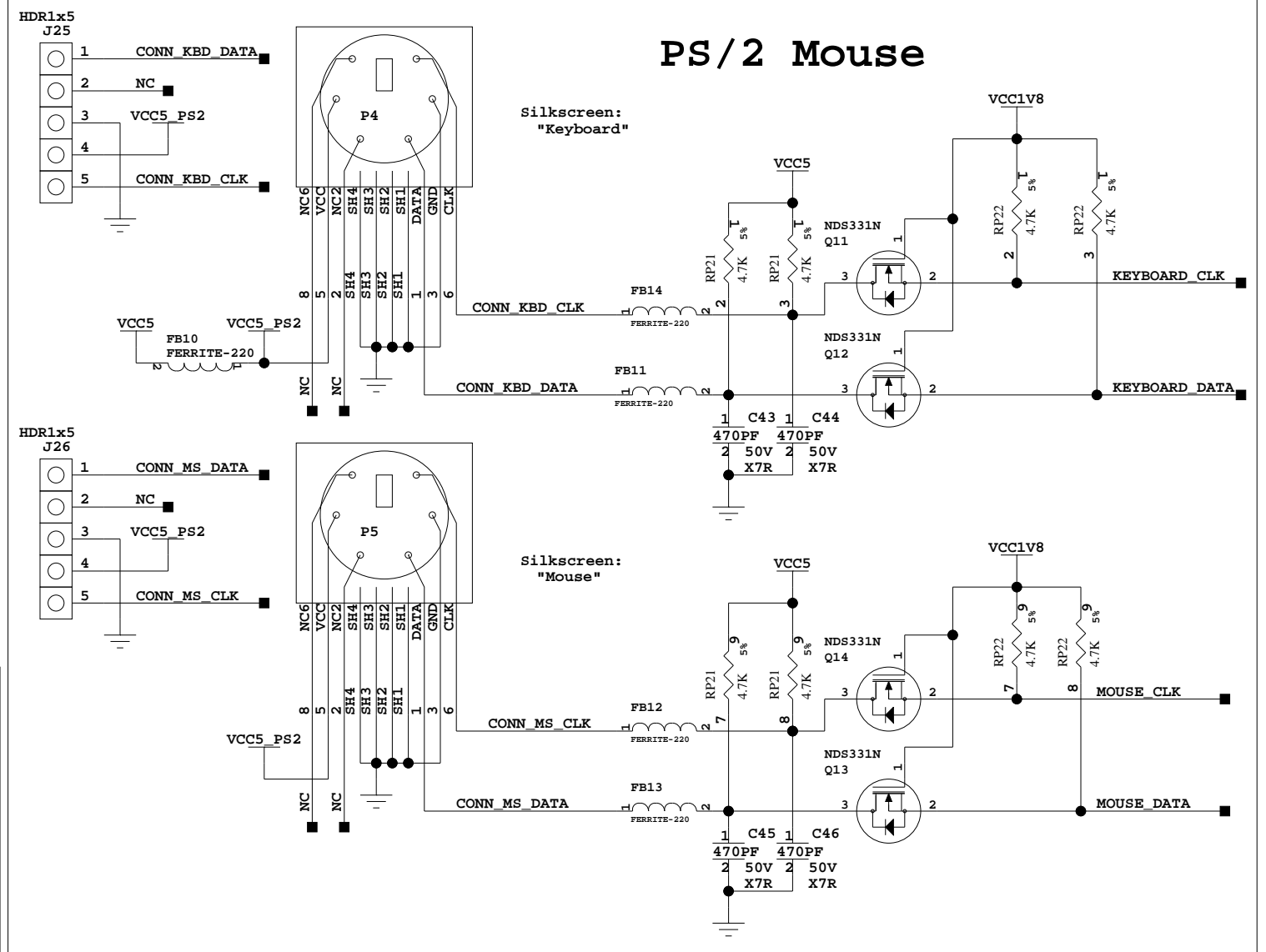
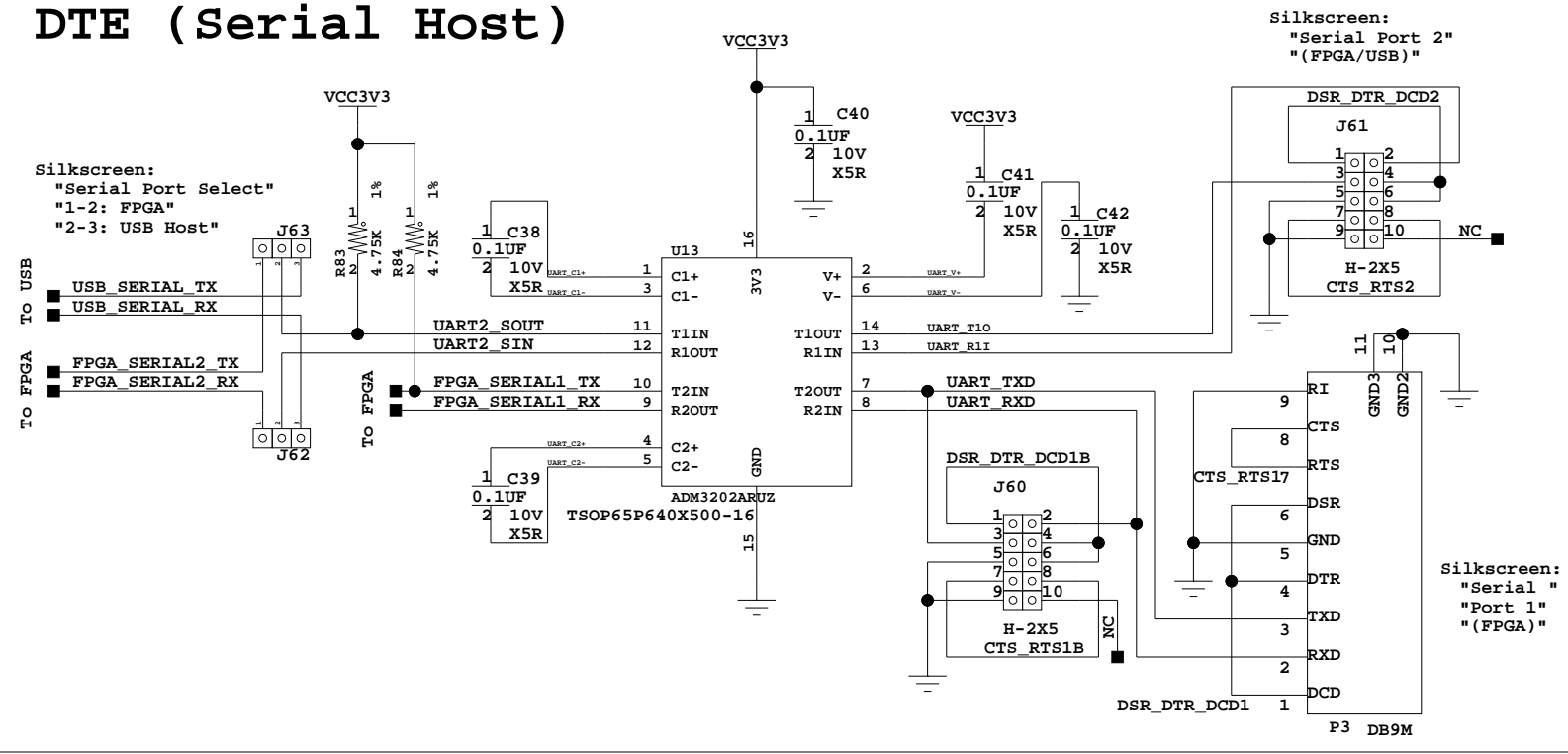


# XGI - Expansion Connector



Title: XGI - Expansion Headers SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 11 of 27	Drawn By BP

# DTE (Serial Host)



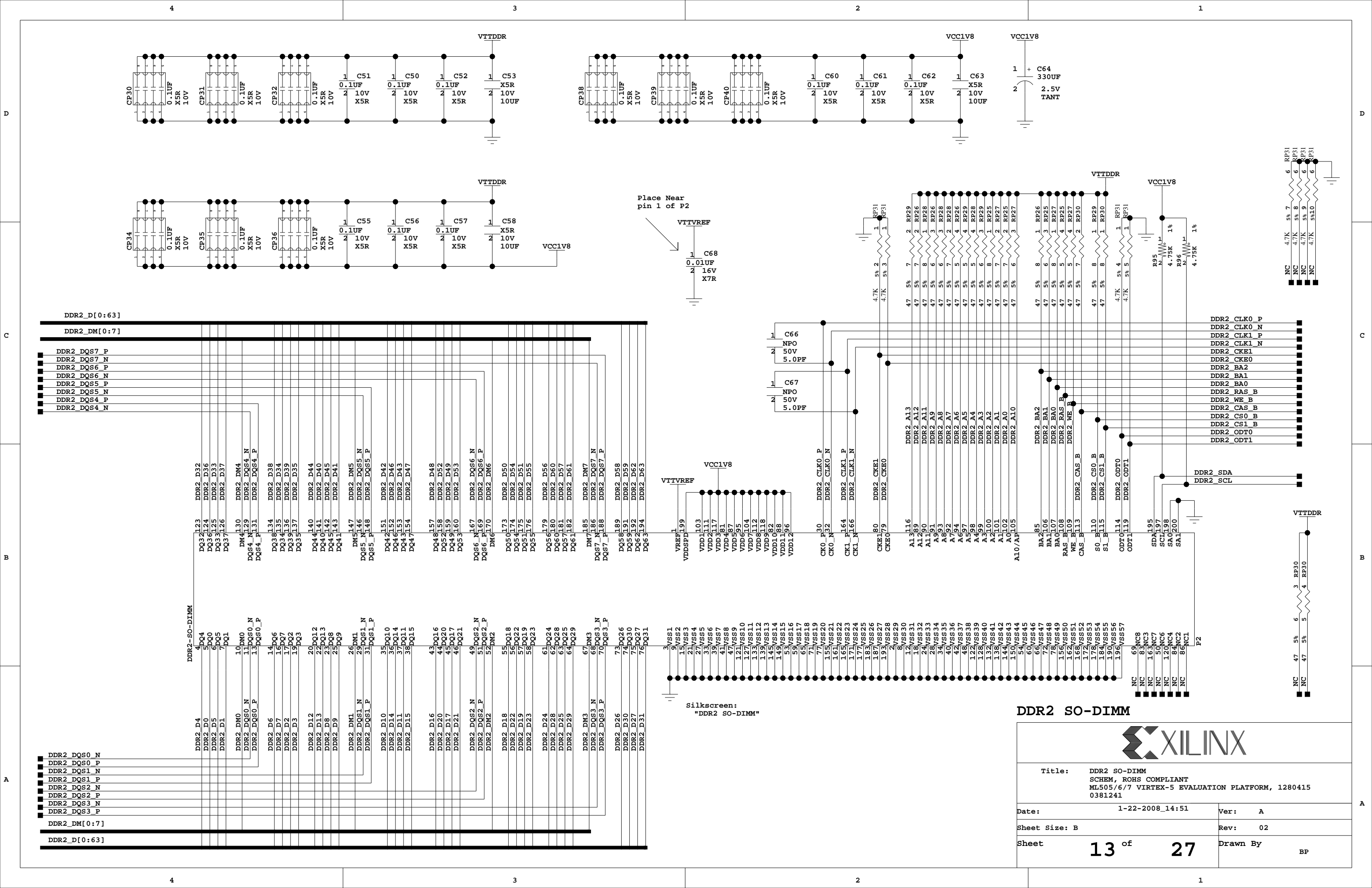
## Misc - LCD, PS2, UART, Fan Controller

**Title:** LCD, PS2, UART, IIC EEPROM, IIC Fan Controller SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241

**Date:** 1-22-2008\_14:55 **Ver:** A

**Sheet Size:** B **Rev:** 02

**Sheet** 12 **of** 27 **Drawn By** BP



**DDR2 SO-DIMM**



Title: DDR2 SO-DIMM  
 SCHEM, ROHS COMPLIANT  
 ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
 0381241

Date: 1-22-2008\_14:51 Ver: A

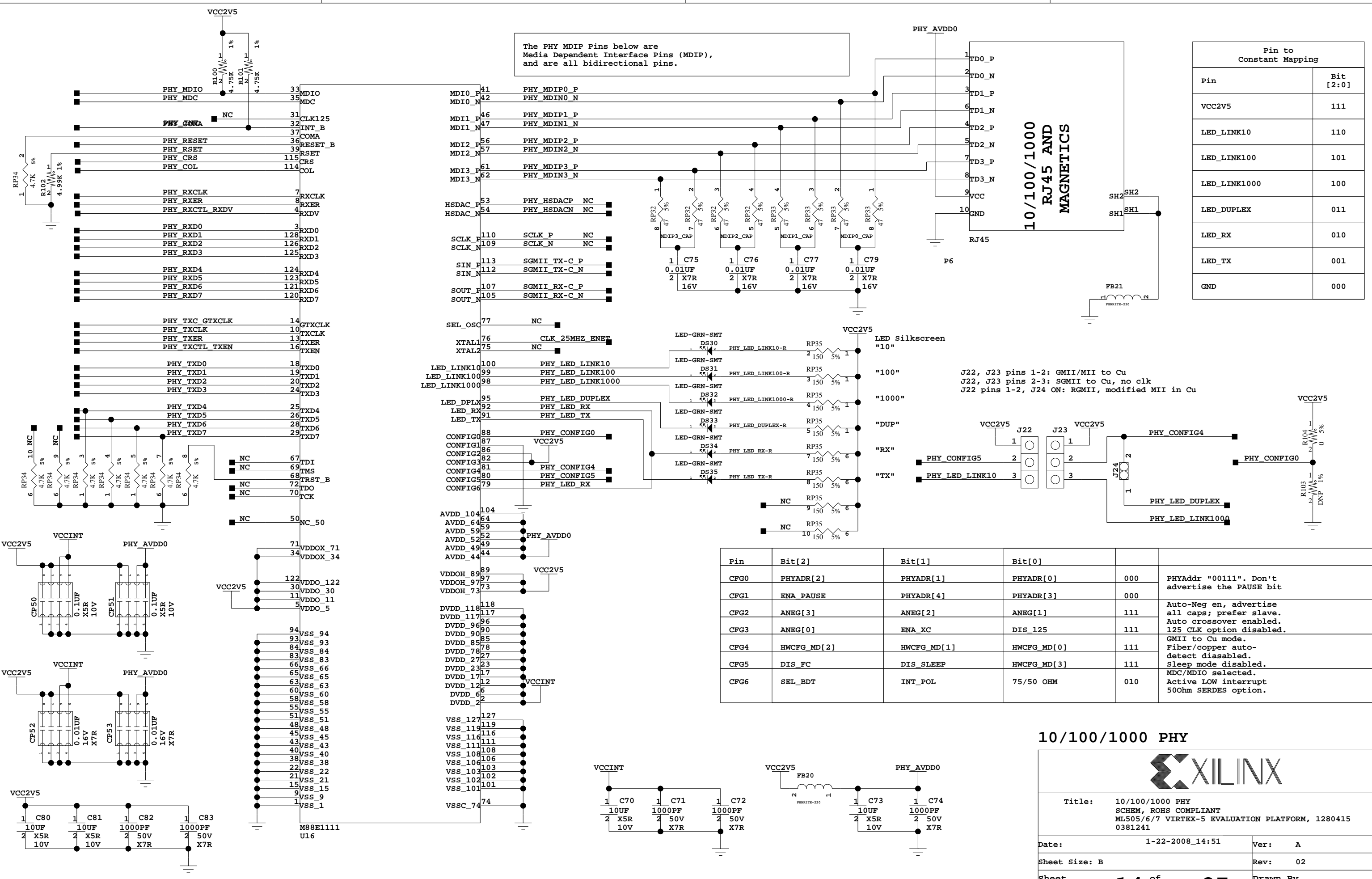
Sheet Size: B Rev: 02

Sheet 13 of 27 Drawn By BP

Silkscreen:  
 "DDR2 SO-DIMM"

Place Near  
 pin 1 of P2

The PHY MDIP Pins below are Media Dependent Interface Pins (MDIP), and are all bidirectional pins.



Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

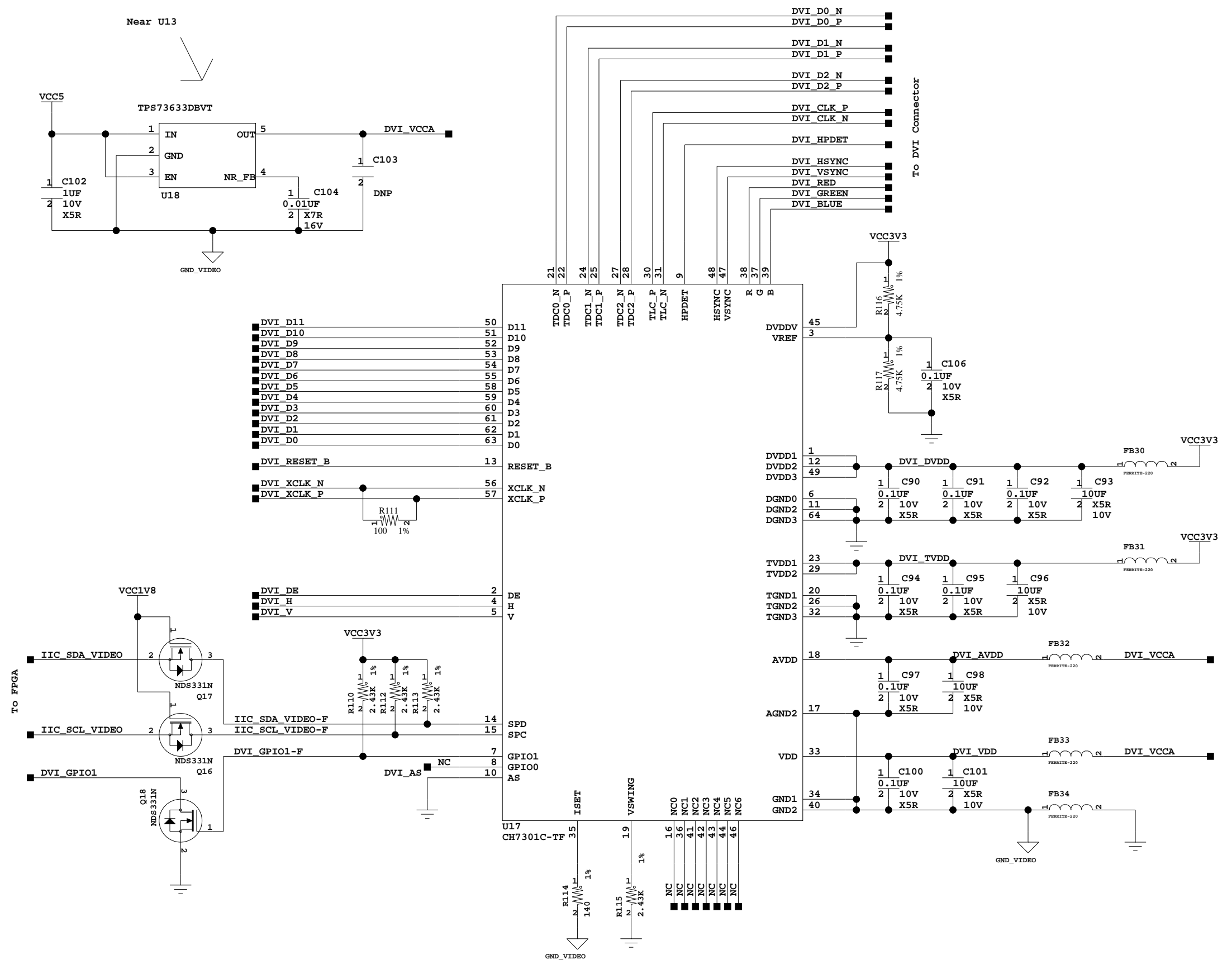
Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS 125	111	
CFG4	HWCFG MD[2]	HWCFG MD[1]	HWCFG MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect disabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG MD[3]	111	MDC/MDIO selected. Active LOW interrupt 500hm SERDES option.
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	

10/100/1000 PHY



Title: 10/100/1000 PHY SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241

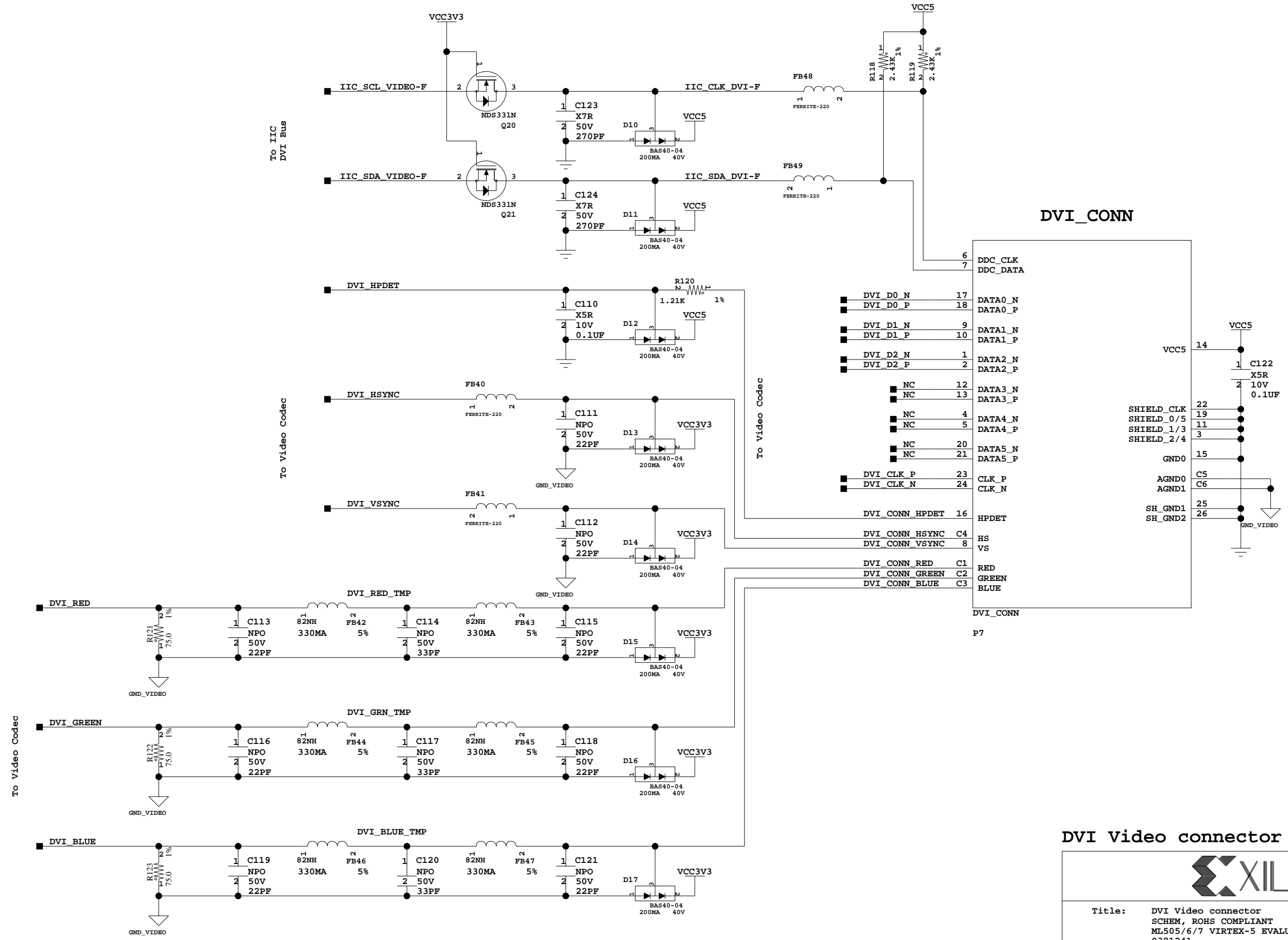
Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
Sheet	14 of 27	Drawn By	BP



IIC Address = 0x76

### VGA Out Codec

Title: VGA Out Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
Sheet 15 of 27	Drawn By BP	



DVI\_CONN

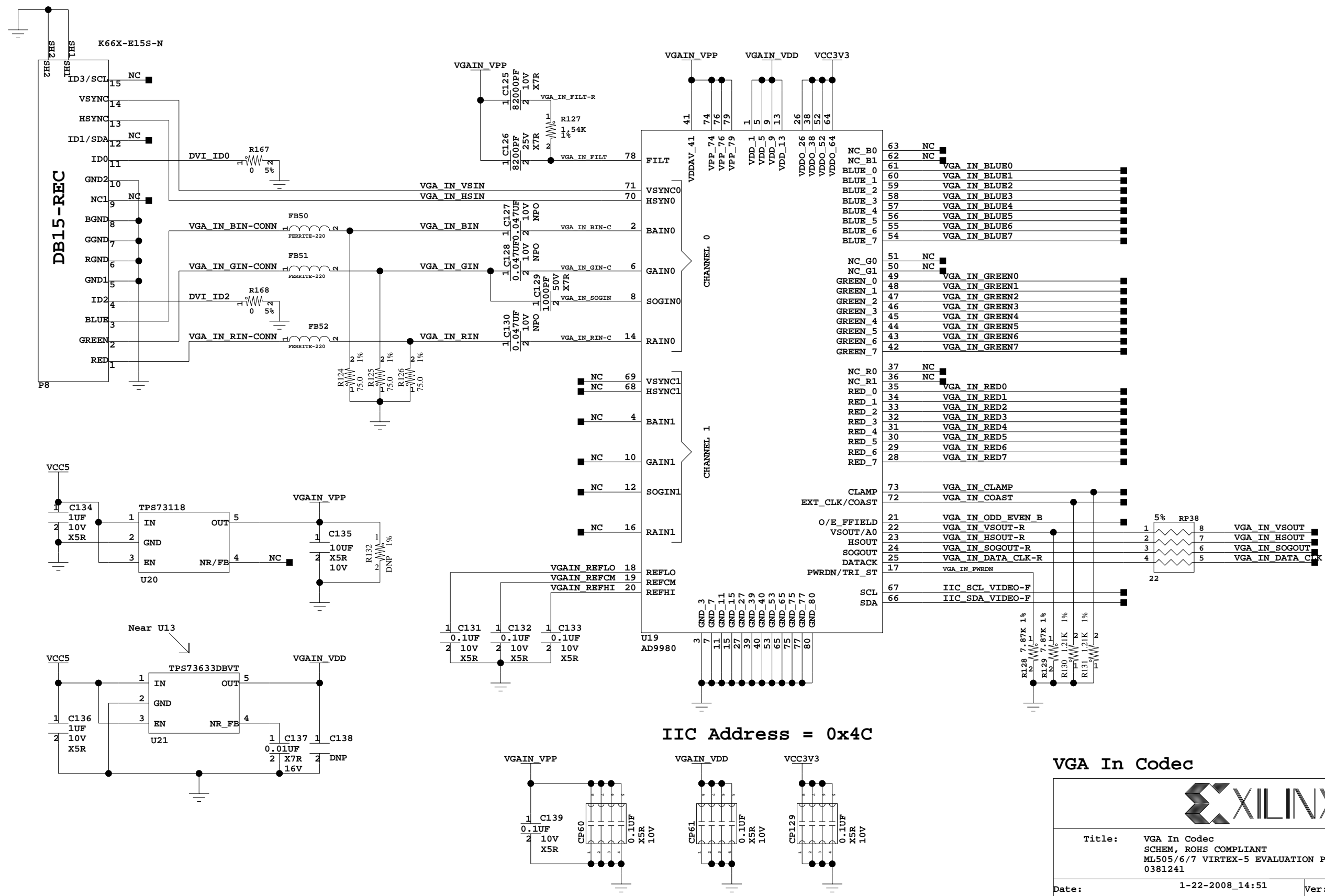
6	DDC_CLK	
7	DDC_DATA	
17	DVI D0 N	DATA0_N
18	DVI D0 P	DATA0_P
9	DVI D1 N	DATA1_N
10	DVI D1 P	DATA1_P
1	DVI D2 N	DATA2_N
2	DVI D2 P	DATA2_P
12	NC	DATA3_N
13	NC	DATA3_P
4	NC	DATA4_N
5	NC	DATA4_P
20	NC	DATA5_N
21	NC	DATA5_P
23	DVI_CLK_P	CLK_P
24	DVI_CLK_N	CLK_N
16	DVI_CONN_HPDET	HPDET
C4	DVI_CONN_HSYNC	HS
8	DVI_CONN_VSYNC	VS
C1	DVI_CONN_RED	RED
C2	DVI_CONN_GREEN	GREEN
C3	DVI_CONN_BLUE	BLUE

DVI Video connector



Title: DVI Video connector SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 16 of 27	Drawn By BP





VGA In Codec



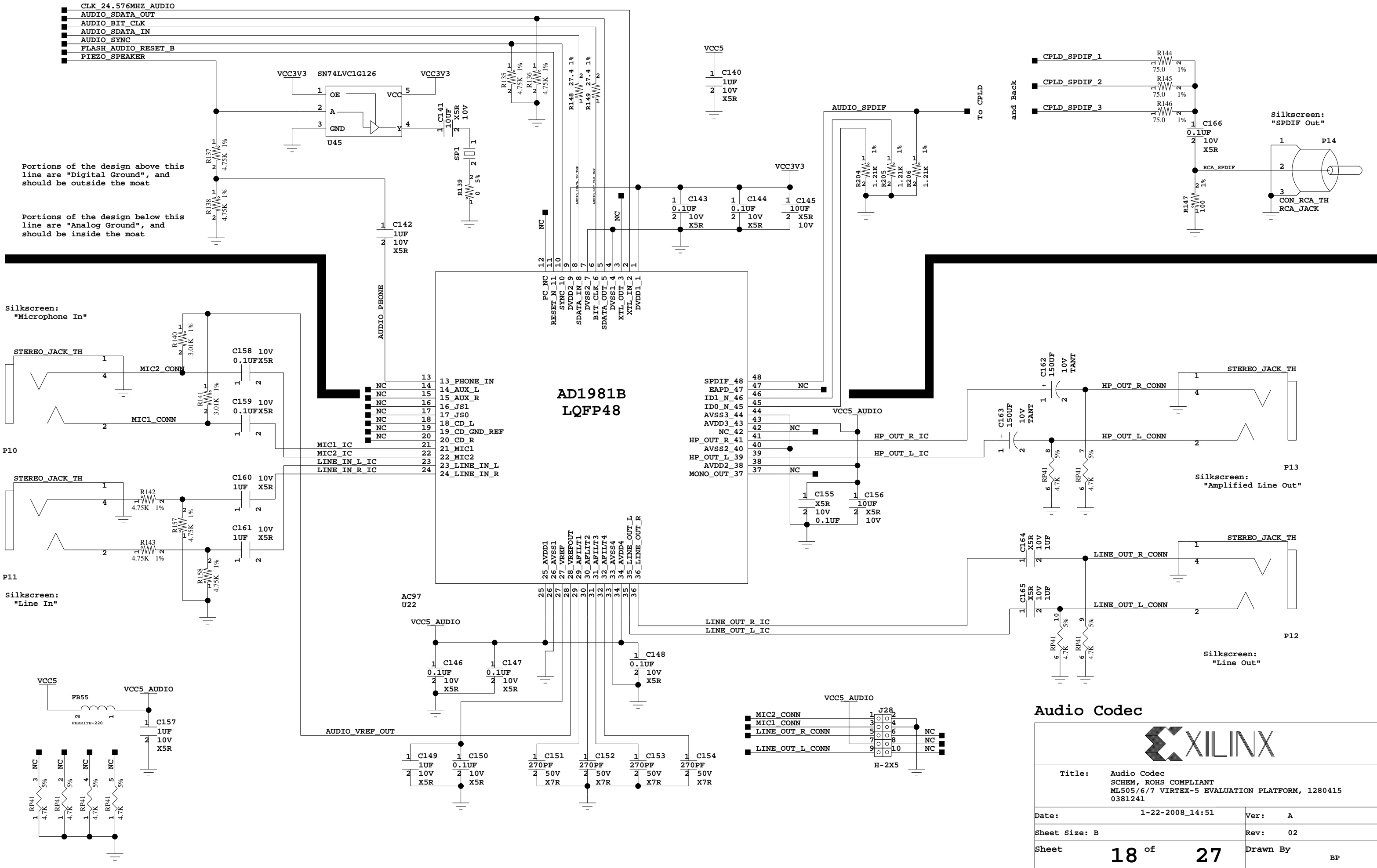
Title: VGA In Codec  
 SCHEM, ROHS COMPLIANT  
 ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
 0381241

Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
Sheet	17 of 27	Drawn By	BP

CLK 24.576MHZ AUDIO  
 AUDIO\_SDATA\_OUT  
 AUDIO\_BIT\_CLK  
 AUDIO\_SDATA\_IN  
 AUDIO\_SYNC  
 FLASH AUDIO RESET\_B  
 PIEZO\_SPEAKER

Portions of the design above this line are "Digital Ground", and should be outside the moat

Portions of the design below this line are "Analog Ground", and should be inside the moat



Audio Codec



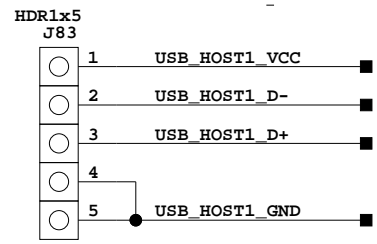
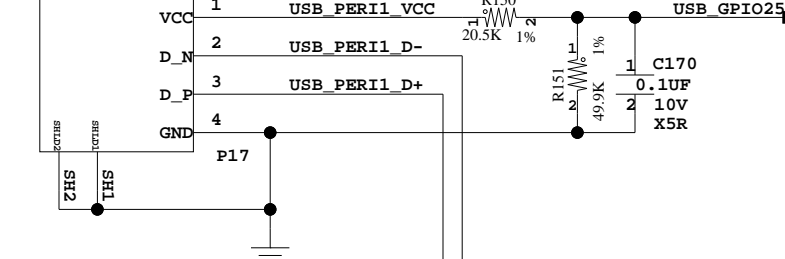
Title: Audio Codec  
 SCHEM, ROHS COMPLIANT  
 ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
 0381241

Date: 1-22-2008\_14:51 Ver: A

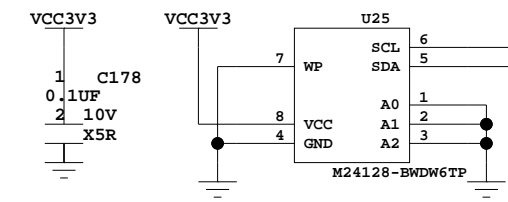
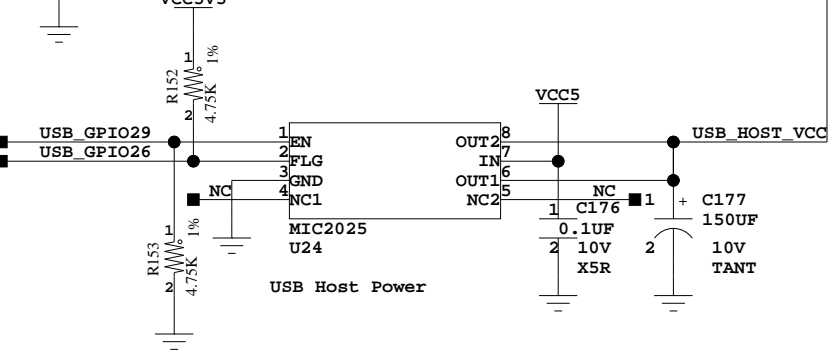
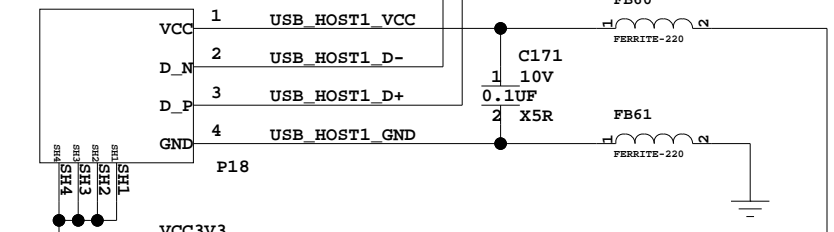
Sheet Size: B Rev: 02

Sheet 18 of 27 Drawn By BP

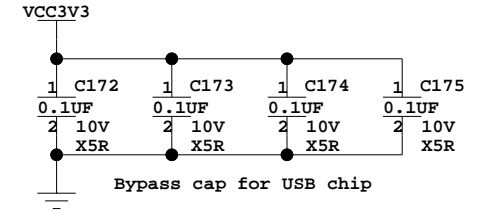
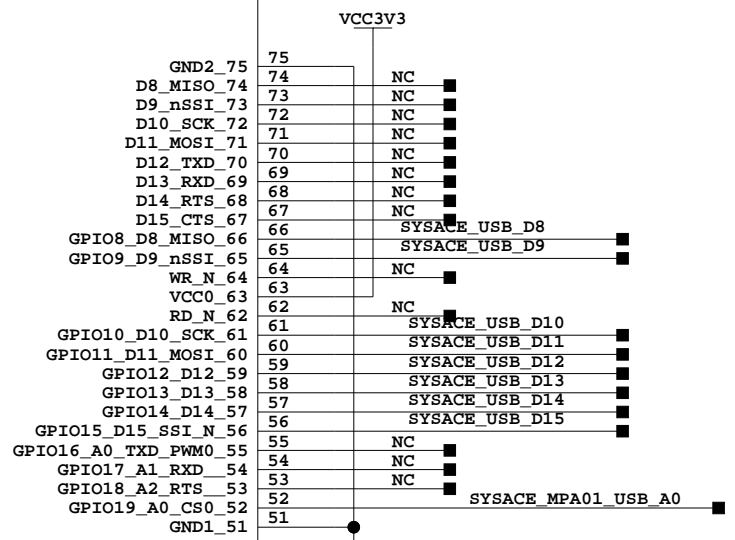
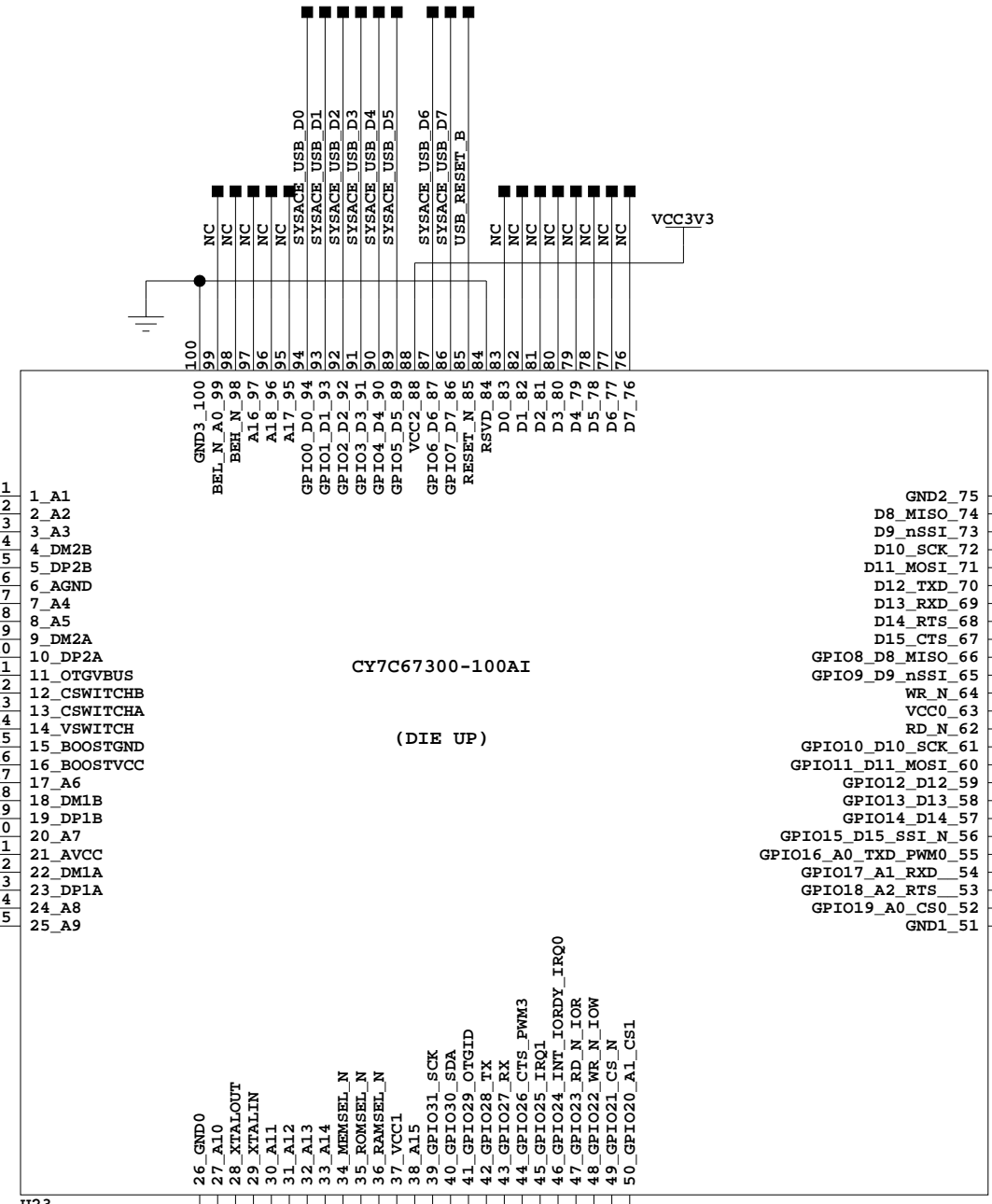
Silkscreen:  
"USB Peripheral 1"  
USB\_B\_PERI\_SMT



Silkscreen:  
"USB Host"



"Abort Boot"  
SDA/SCL lines swapped for an EEPROM larger than 16KB



### USB Controller

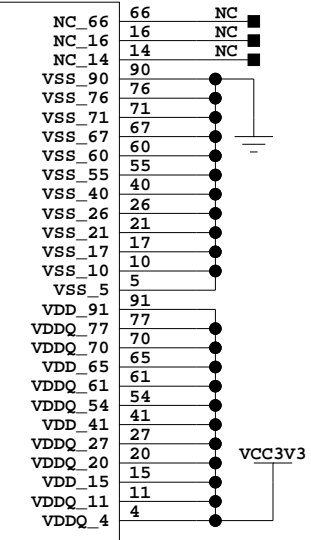
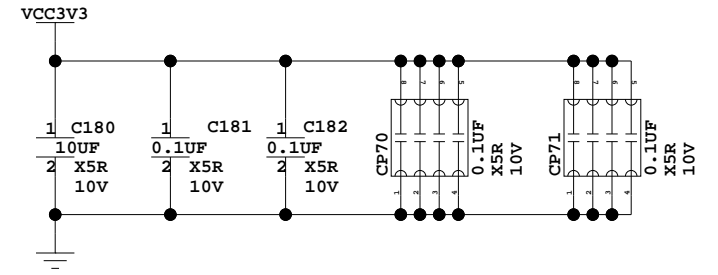


Title: USB Controller SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
Sheet 19 of 27	Drawn By	BP

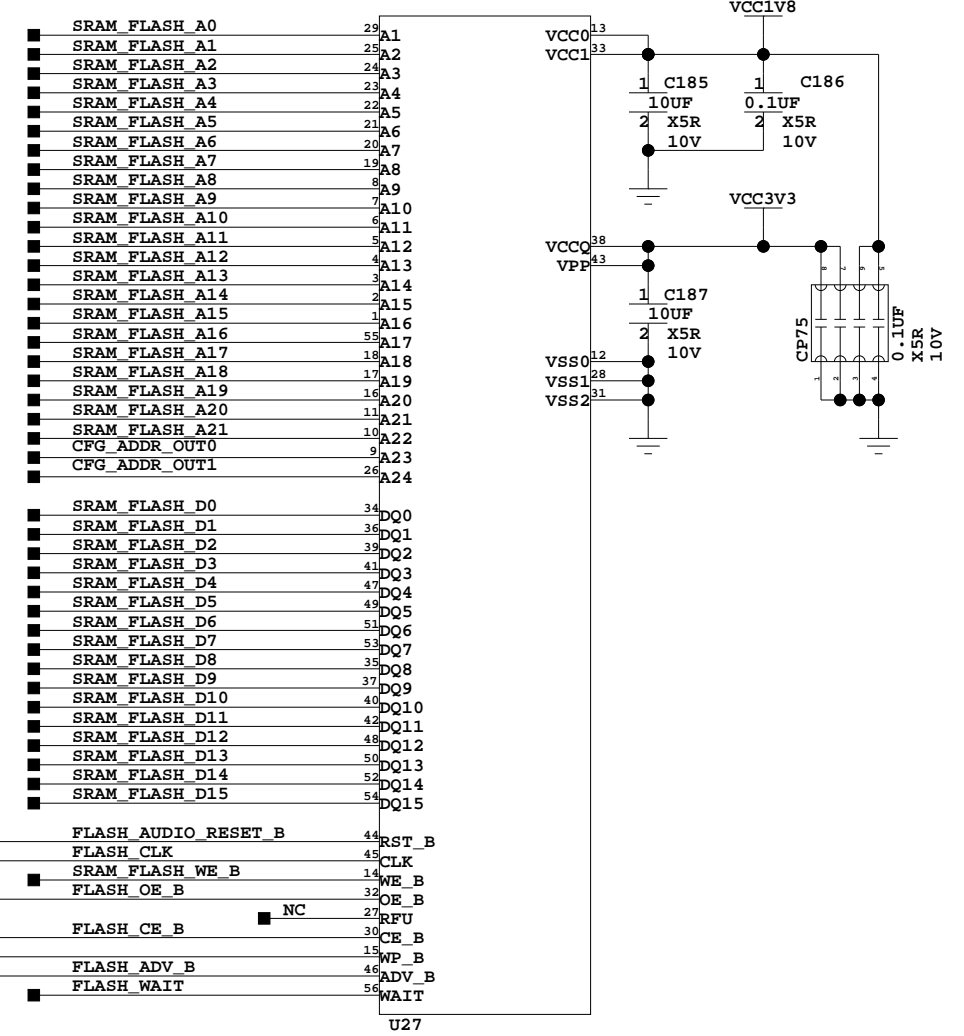
The burst order mode of the SRAM is set to "Linear" by default



SRAM\_ZBT\_256KX36  
U26



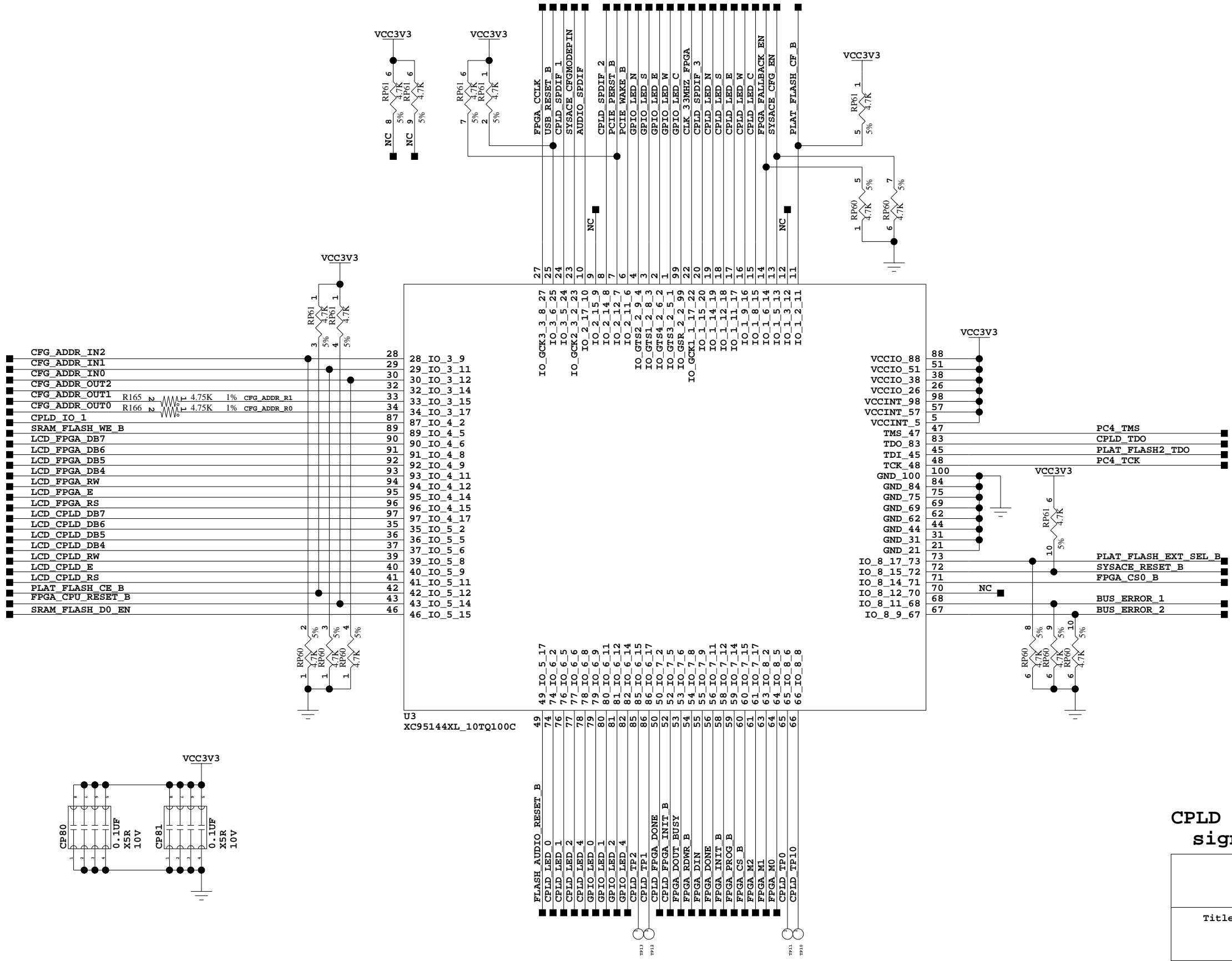
Silkscreen:  
"Strata FLASH"  
"256 MBit"



Memory:  
Synchronous SRAM,  
Strata FLASH



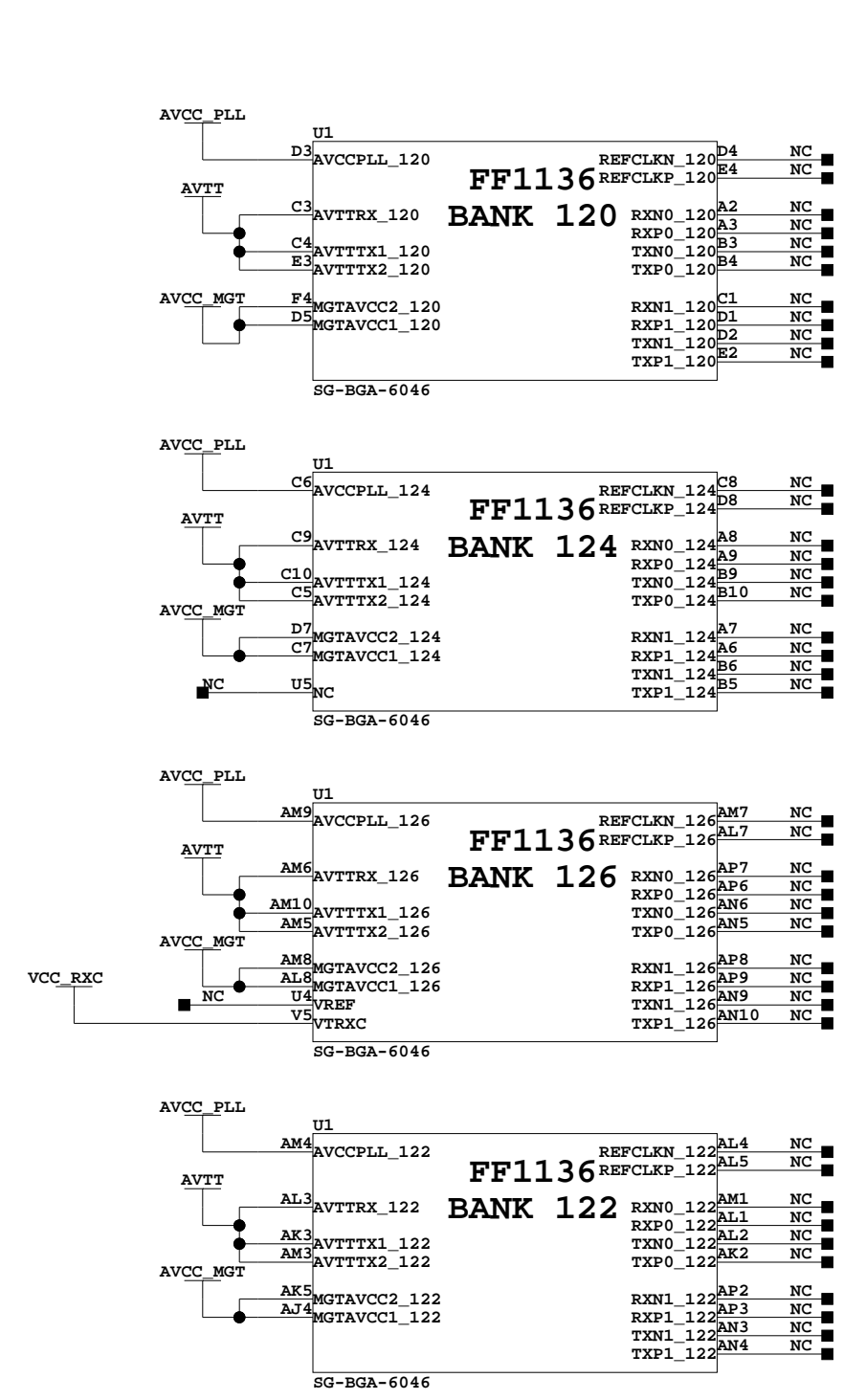
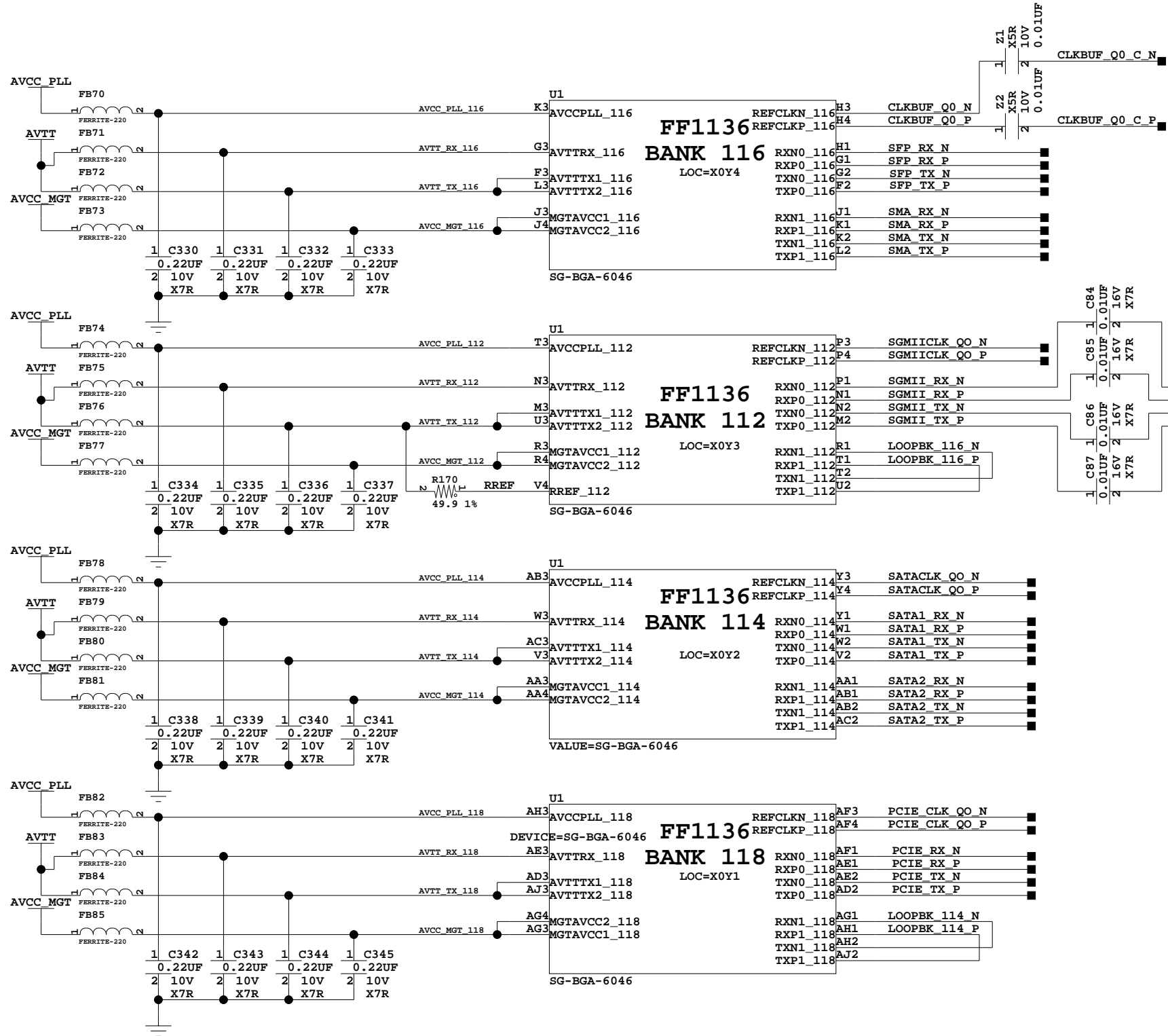
Title: Sync. SRAM, FLASH SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 20 of 27	Drawn By BP



CPLD - Misc  
signal control



Title: CPLD - Misc signal control SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 21 of 27	Drawn By BP

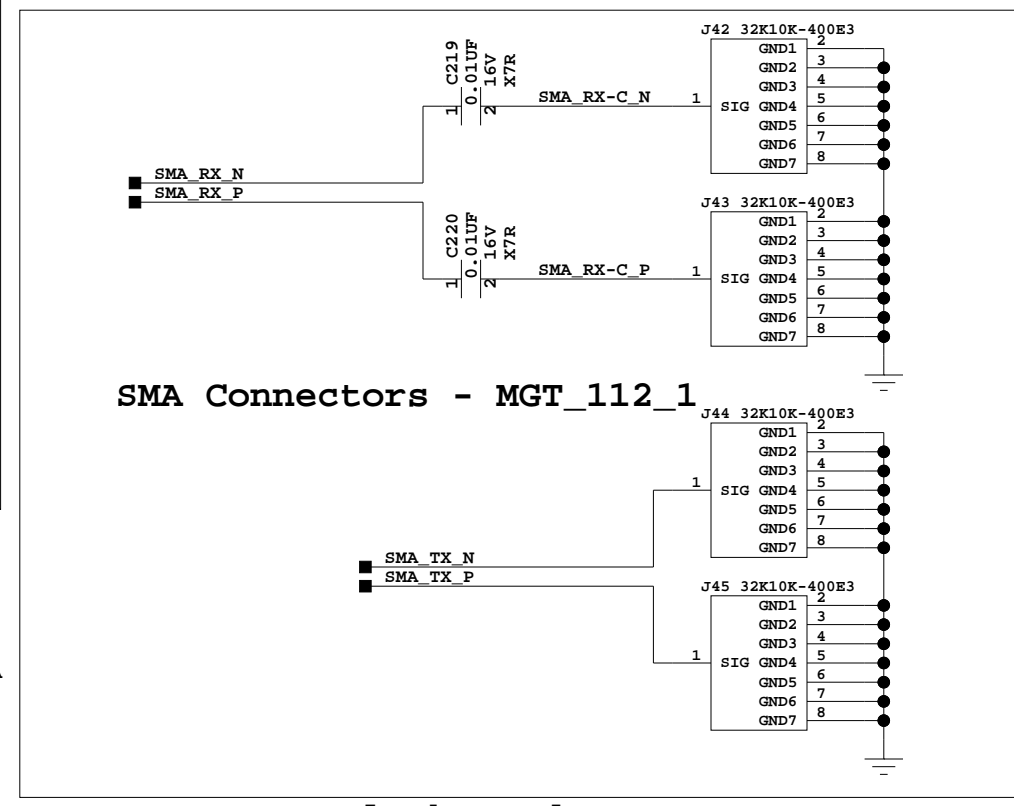
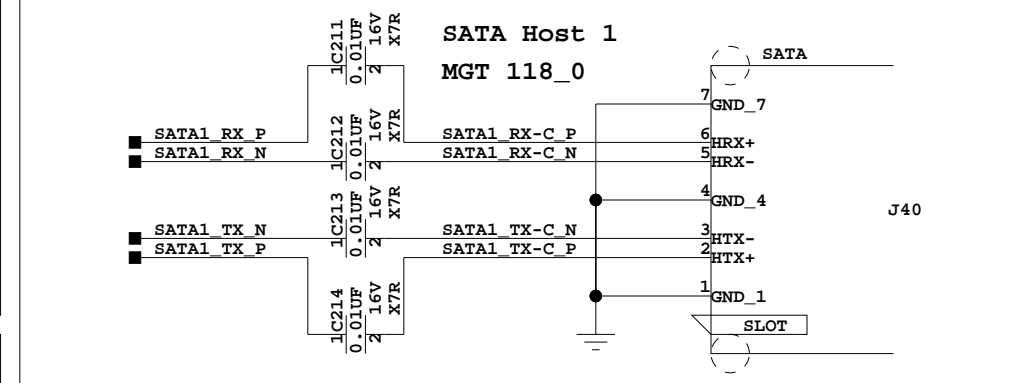
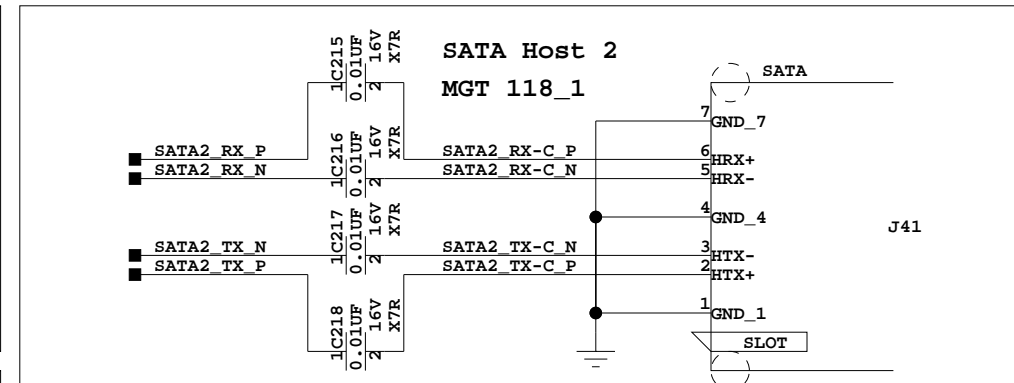
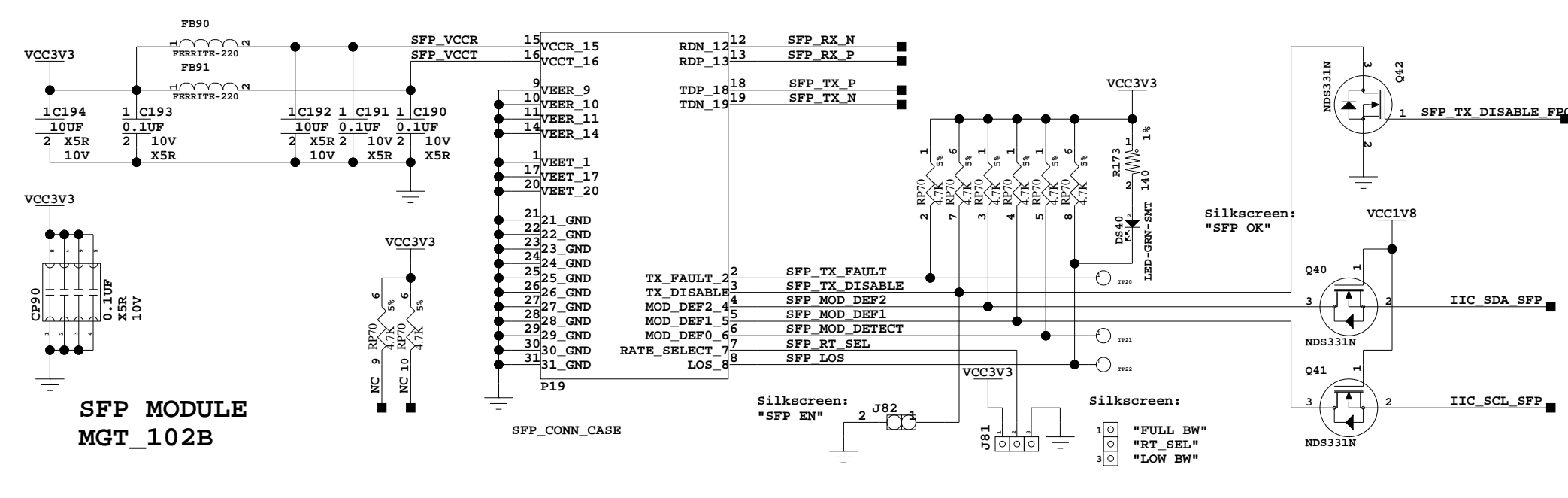
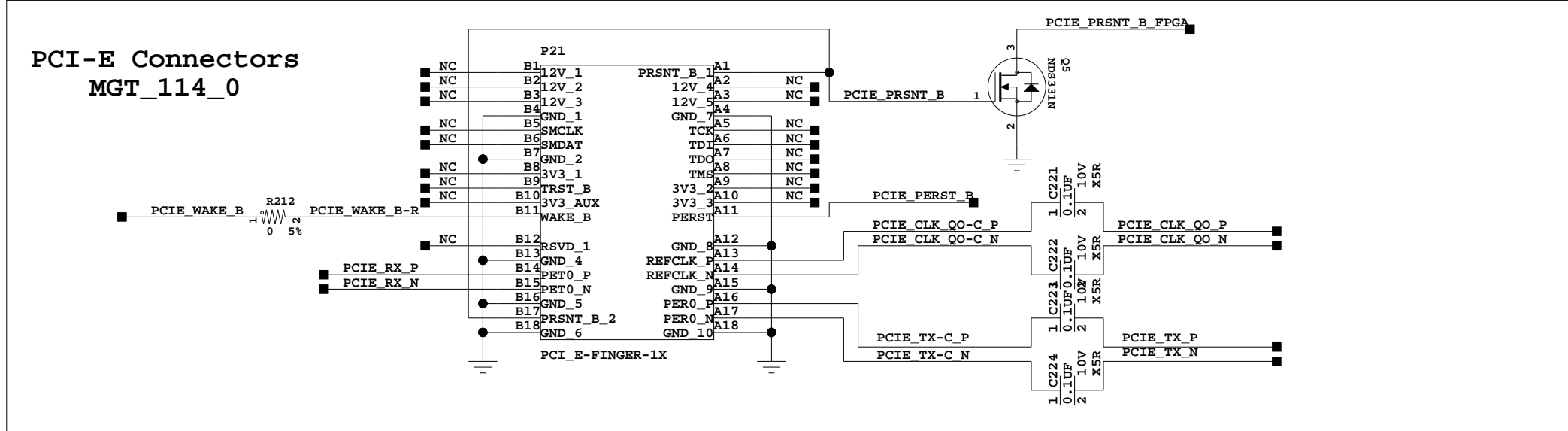
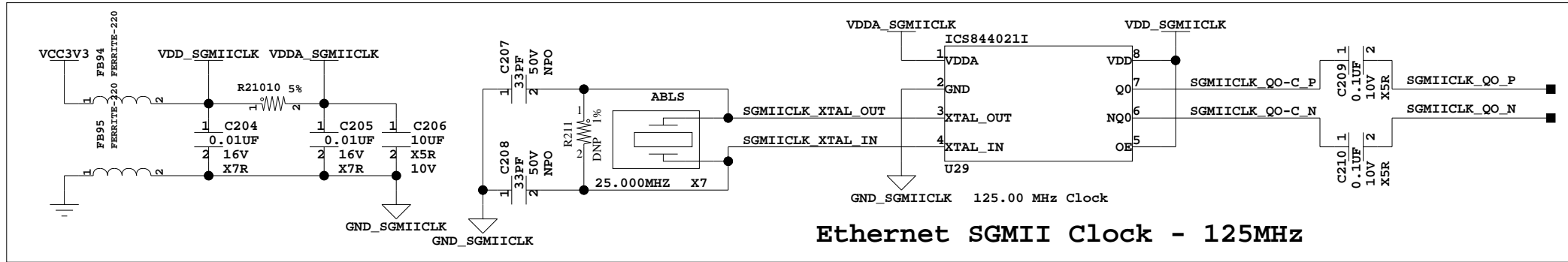
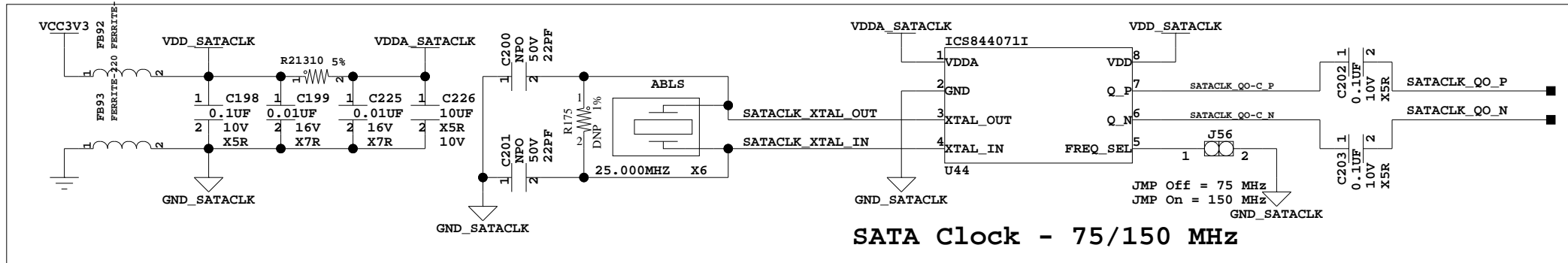


Title: MGT Banks  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

Date: 1-22-2008\_14:55 Ver: A

Sheet Size: B Rev: 02

Sheet 22 of 27 Drawn By BF



**MGT Clocks and Connectors**



Title: MGT Connectors SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 23 of 27	Drawn By BF

### MGT PLL Regulator

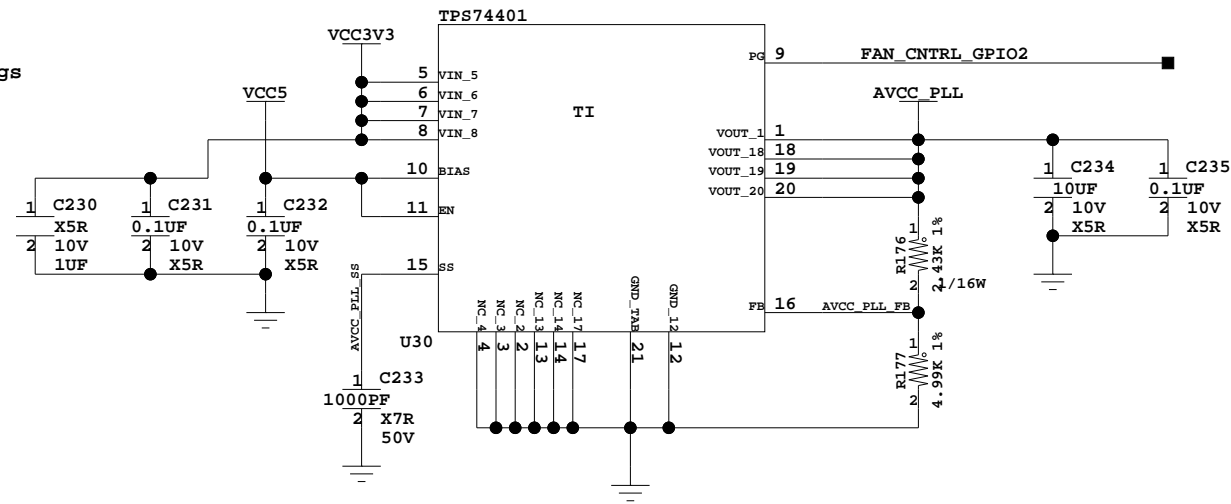
#### Voltage Output Settings

LXT & SXT (ML505/6)  
AVCC\_PLL = 1.2V @ 3A

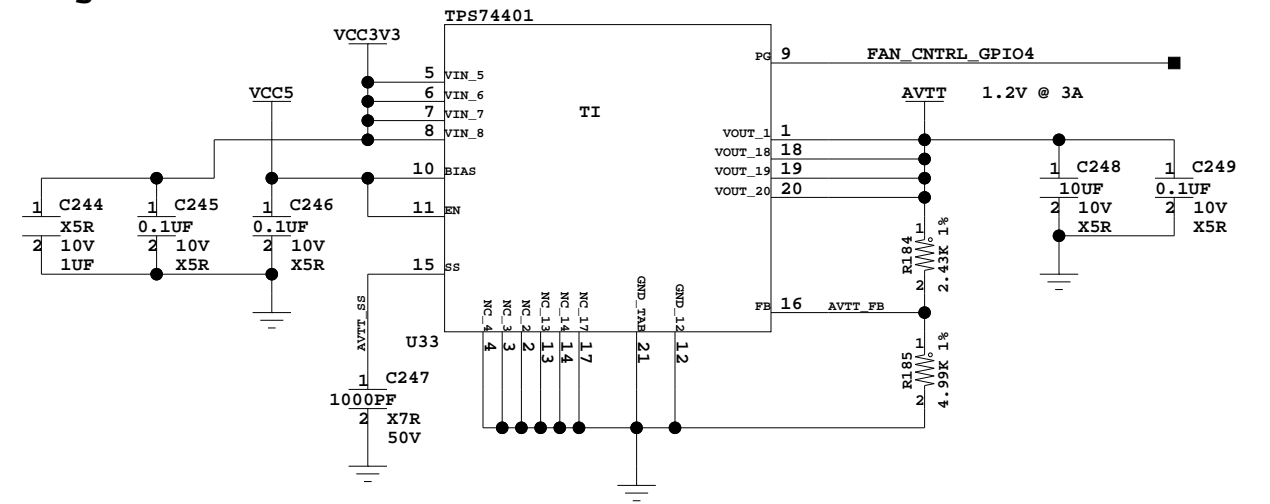
R176 = 2.43K 1%  
R177 = 4.99K 1%

FXT Only (ML507)  
AVCC\_PLL = 1.0V @ 3A

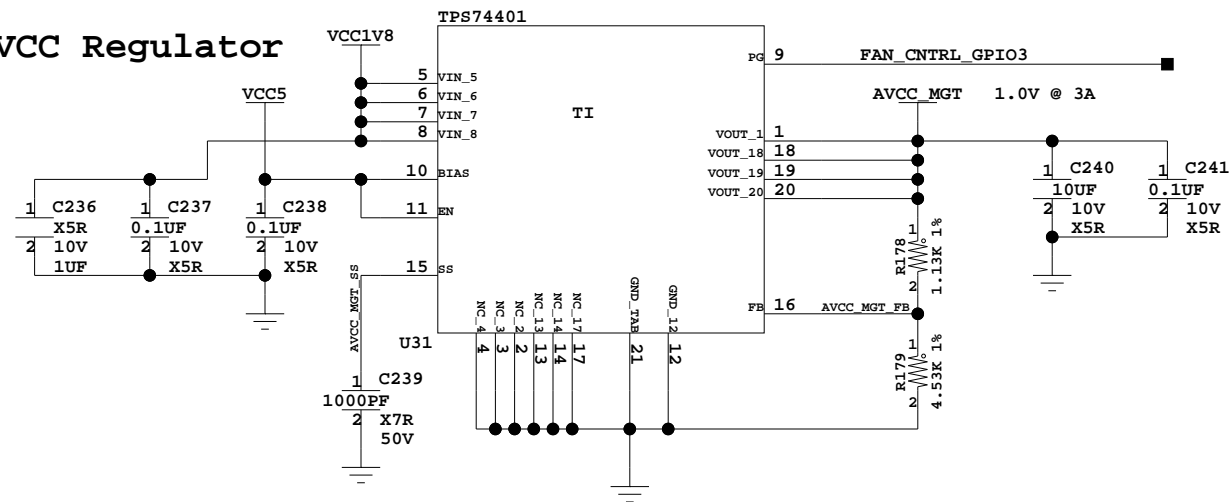
R176 = 1.13K 1%  
R177 = 4.53K 1%



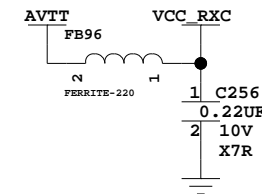
### MGT VTT Regulator



### MGT AVCC Regulator



### MGT RXC Regulator



### MGT Power Supplies

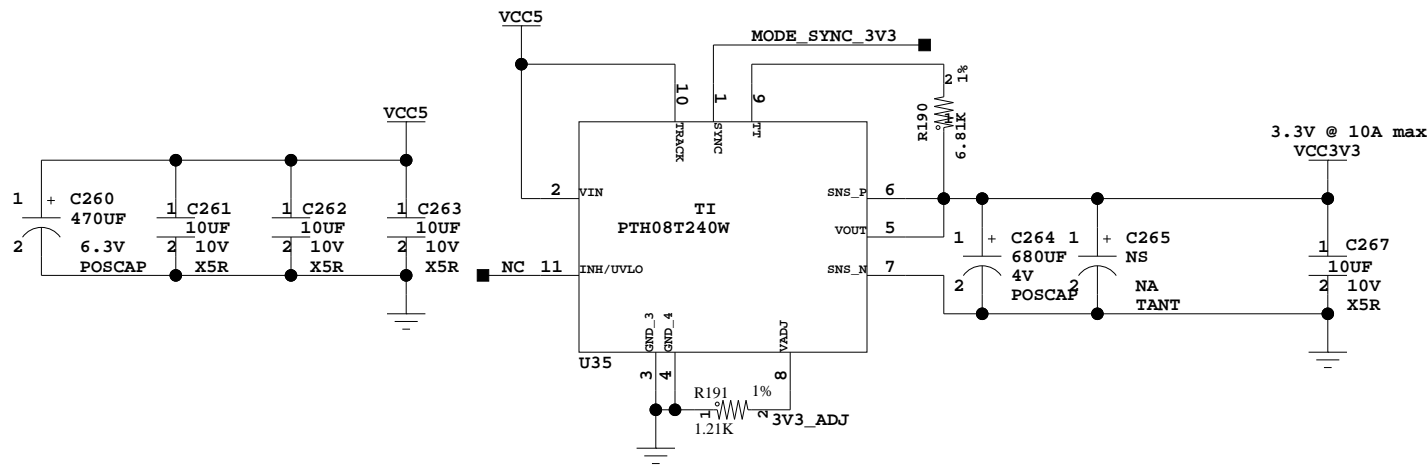


Title: MGT Power Supplies  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

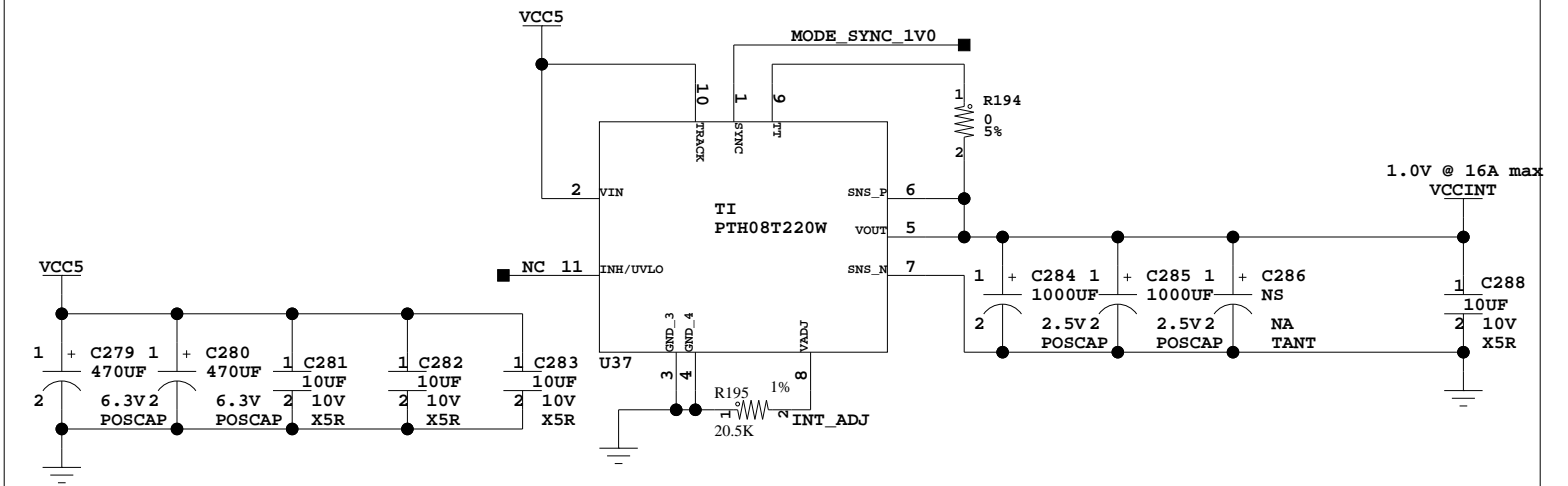
Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
Sheet	24 of 27	Drawn By	BF



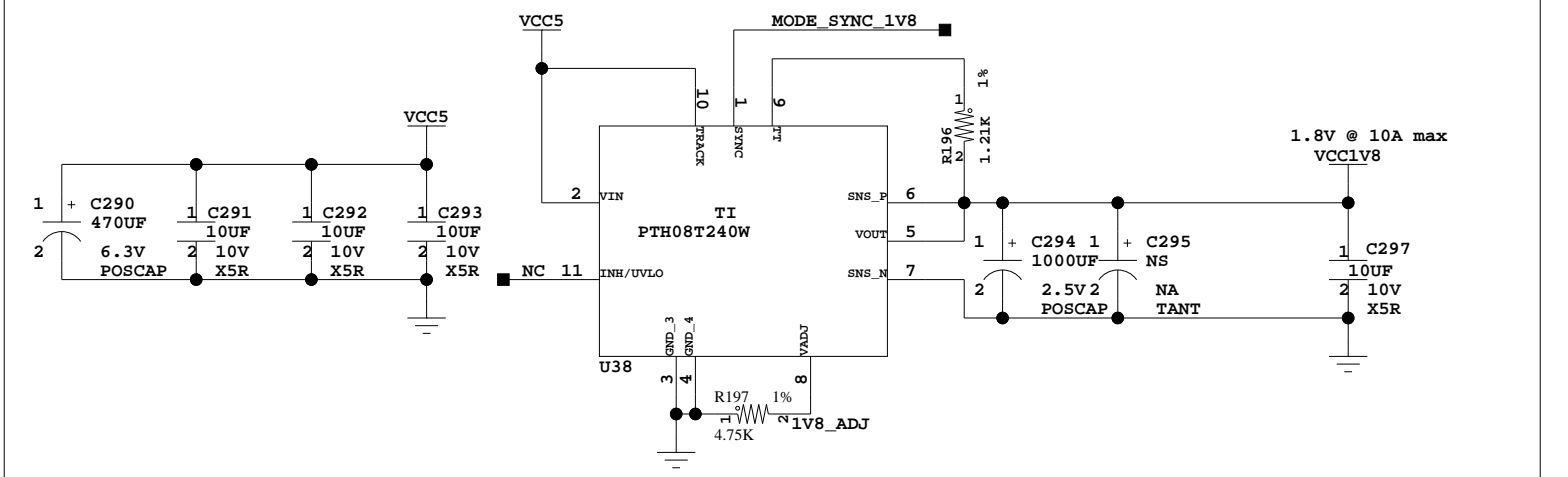
### 5v to 3.3V Regulator



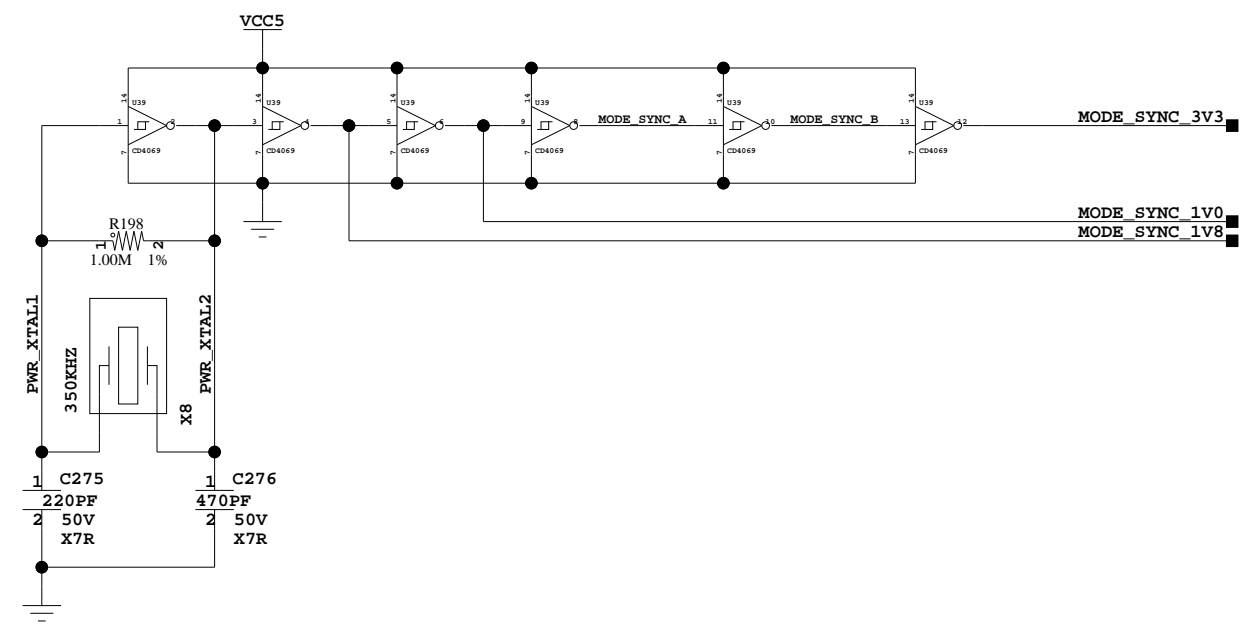
### 5v to 1.0V Regulator



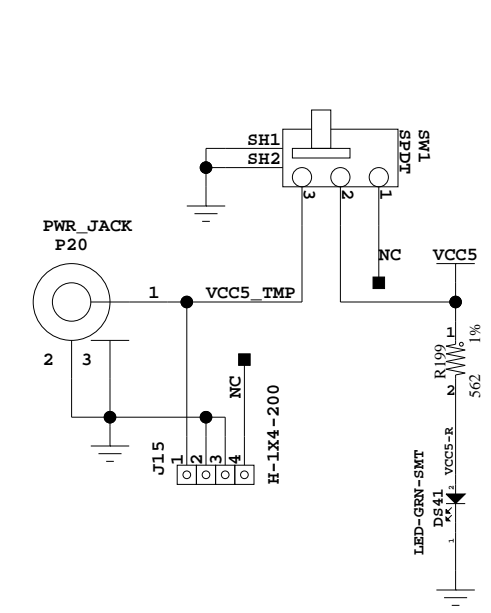
### 5v to 1.8V Regulator



### 5V Power Synchronizing Circuit



### 5V Power - Jack, Switch and LED

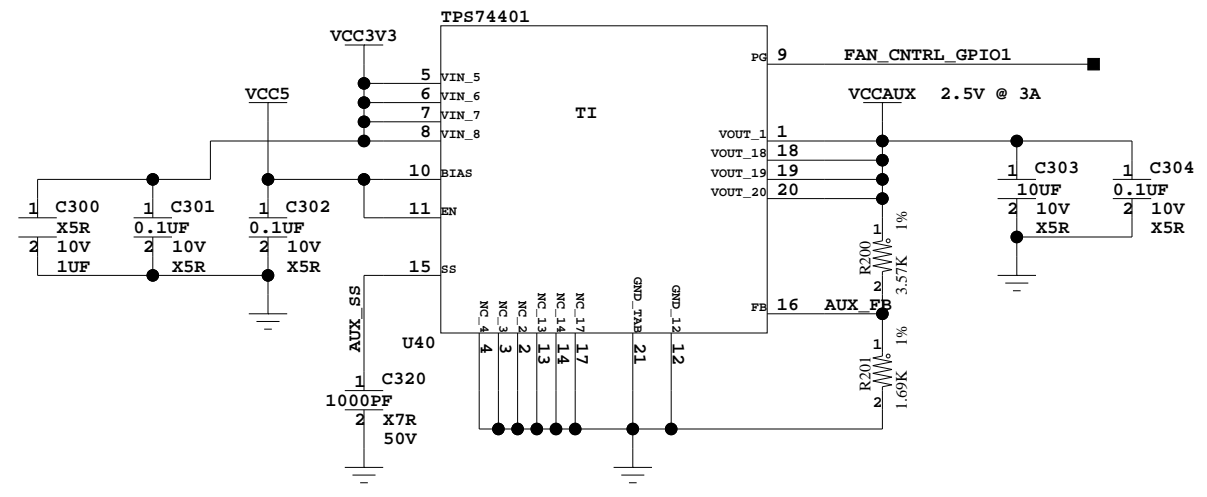


### 5V Power Supplies

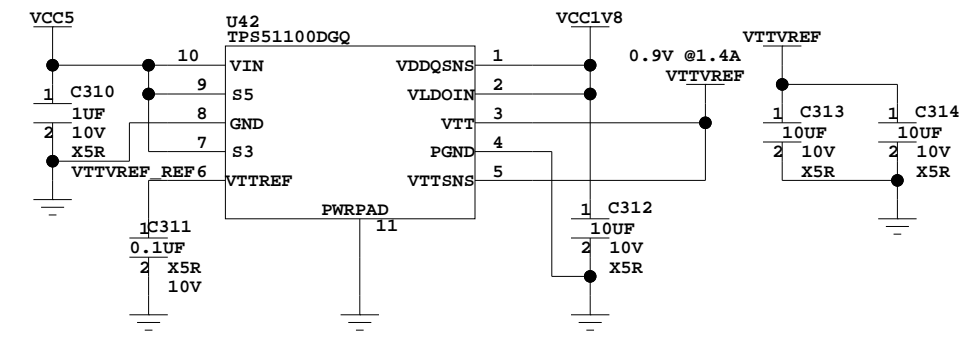


Title: Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 25 of 27	Drawn By BP

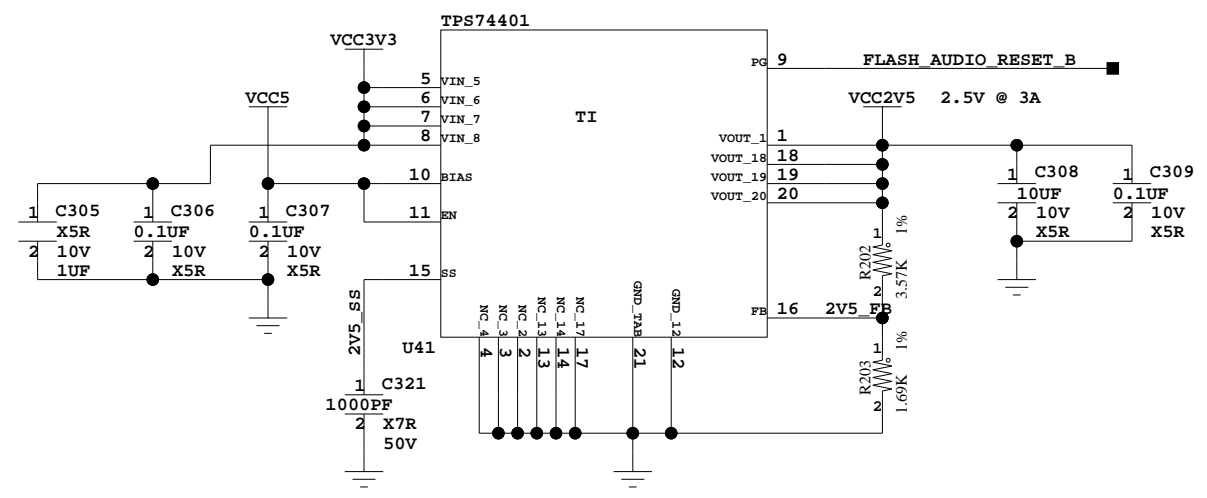
3.3v to 2.5V (VCC AUX) Regulator



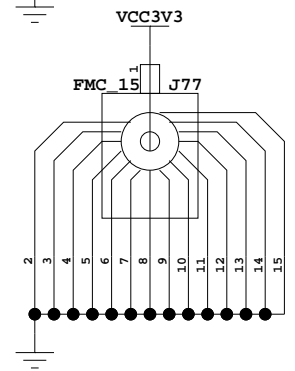
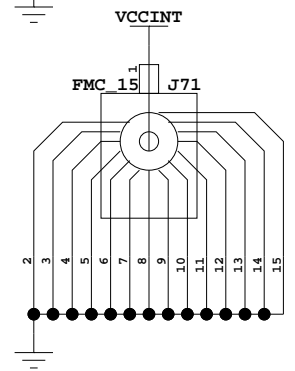
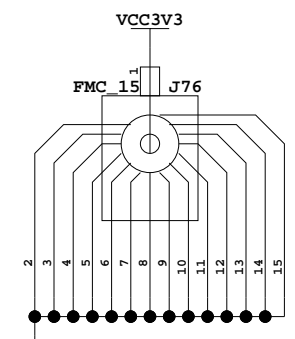
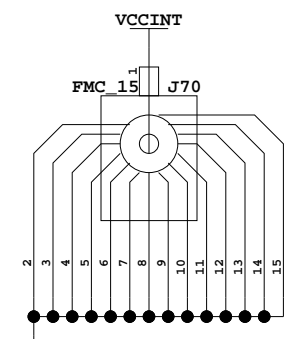
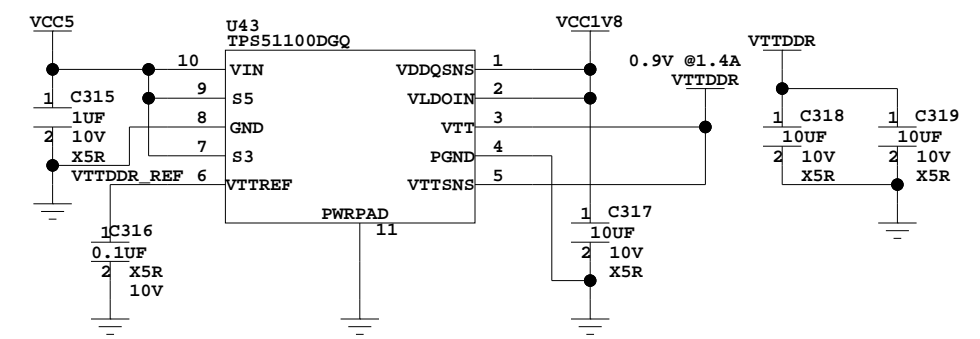
5V to 0.9V (DDR VTT VREF) Regulator



3.3v to 2.5V Regulator



5V to 0.9V (DDR2 VTT DDR) Regulator

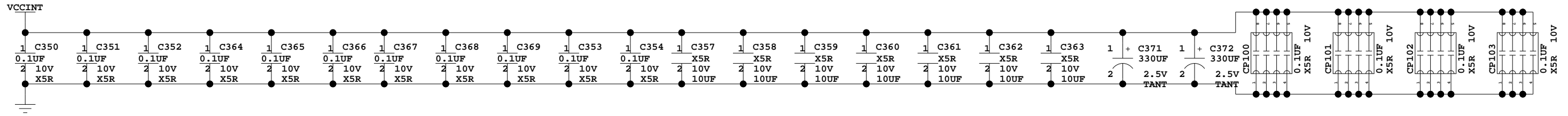


5V and 3.3V Power Supplies

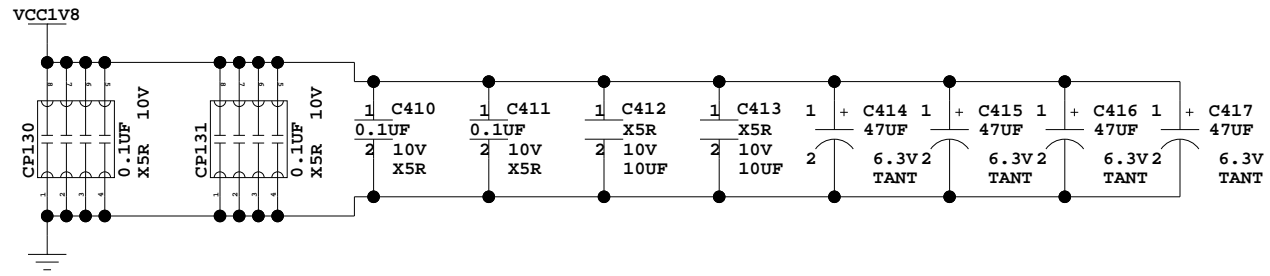
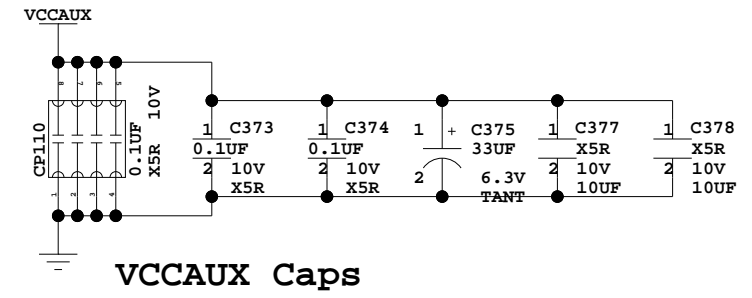
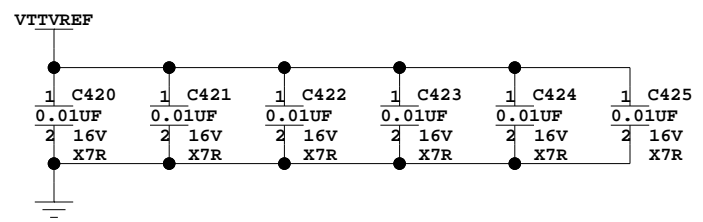
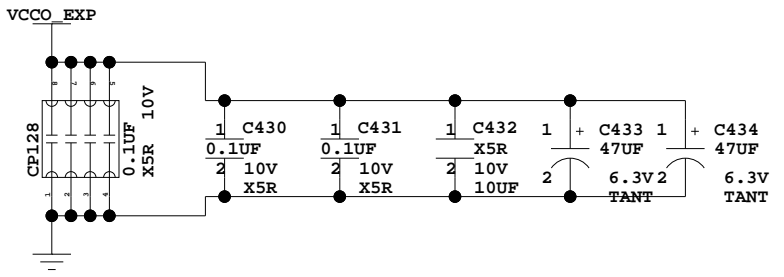
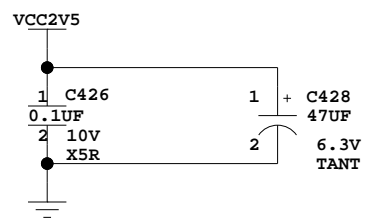
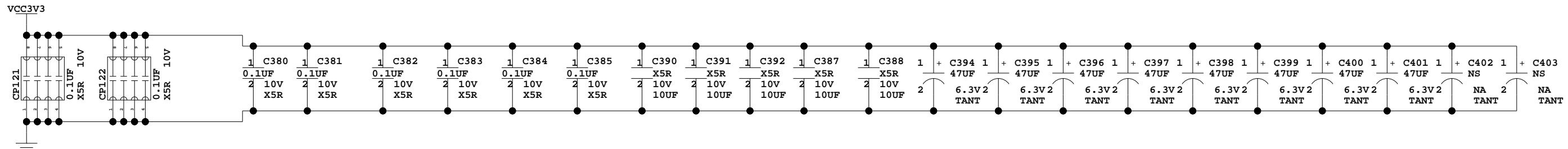


Title: Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
Sheet 26 of 27	Drawn By	BP

### VCCINT Caps



### VCCO Caps



### VCCAUX Caps



Title: FPGA Decoupling SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 27 of 27	Drawn By BP