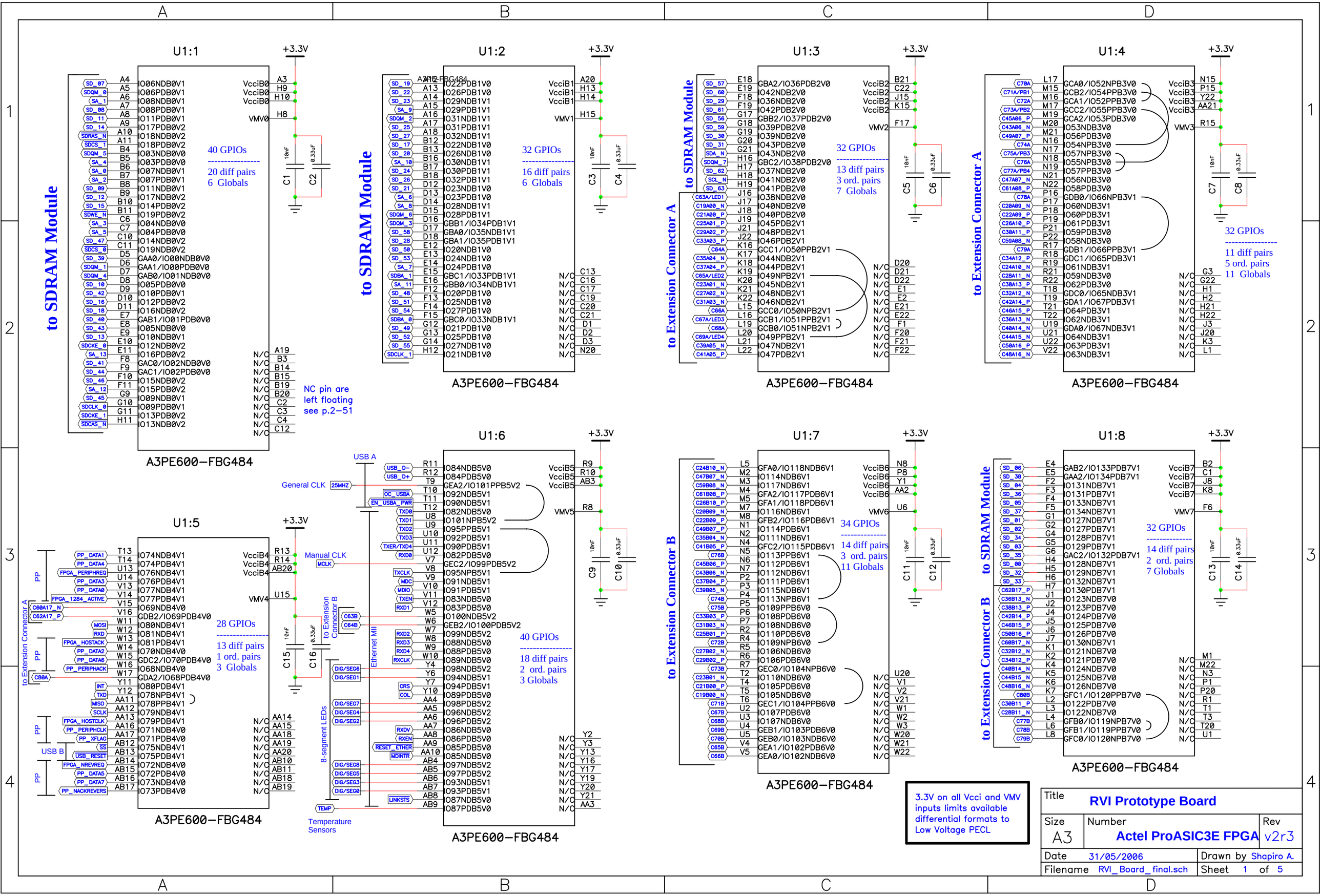
U1:1
+3.3V
to SDRAM Module
40 GPIOs
20 diff pairs
6 Globals
NC pin are left floating see p.2-51
A3PE600-FBG484
U1:2
to SDRAM Module
32 GPIOs
16 diff pairs
6 Globals
A3PE600-FBG484
U1:3
to SDRAM Module
to Extension Connector A
32 GPIOs
13 diff pairs
3 ord. pairs
7 Globals
A3PE600-FBG484
U1:4
to Extension Connector A
32 GPIOs
11 diff pairs
5 ord. pairs
11 Globals
A3PE600-FBG484
U1:5
to Extension Connector A
28 GPIOs
13 diff pairs
1 ord. pairs
3 Globals
USB B
A3PE600-FBG484
U1:6
USB A
General CLK
25MHZ
Manual CLK
Ethernet MII
8-segment LEDs
Temperature Sensors
40 GPIOs
18 diff pairs
2 ord. pairs
3 Globals
A3PE600-FBG484
U1:7
to Extension Connector B
34 GPIOs
14 diff pairs
3 ord. pairs
11 Globals
A3PE600-FBG484
U1:8
to SDRAM Module
to Extension Connector B
32 GPIOs
14 diff pairs
2 ord. pairs
7 Globals
A3PE600-FBG484
3.3V on all Vcci and VMV inputs limits available differential formats to Low Voltage PECL
Title RVI Prototype Board
Size A3
Number Actel ProASIC3E FPGA
Rev v2r3
Date 31/05/2006
Drawn by Shapiro A.
Filename RVI_Board_final.sch
Sheet 1 of 5