Multiprocessor template based on DMA

Introduction

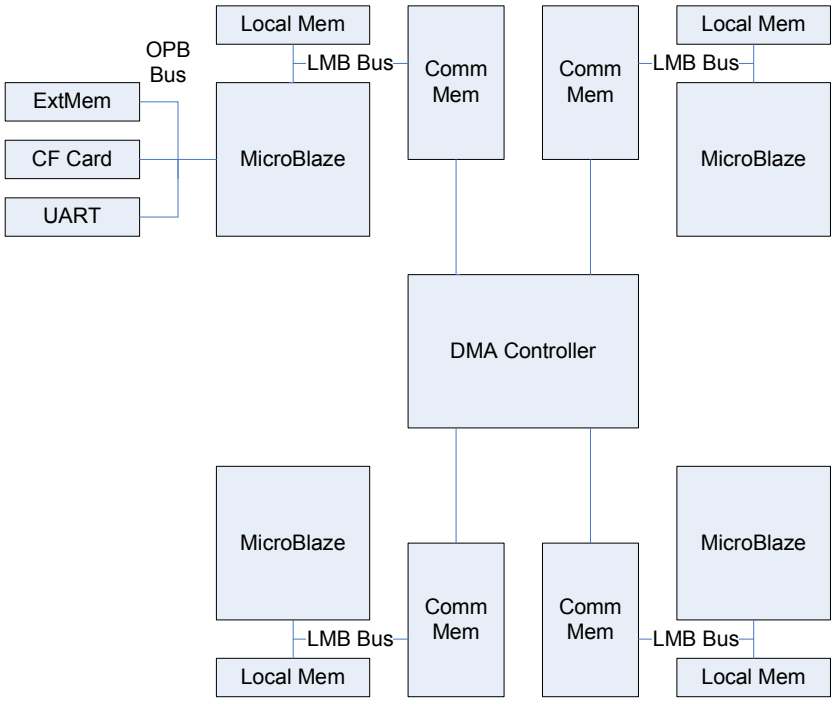
DMA is becoming popular for communication between multiprocessors on a chip. This design is an SoC template consisting of 4 microblaze processors and external memory controller which are connected by a central DMA engine. It is supposed to achieve high predictability, scalability, flexibility and reusability with little cost in area and development efforts. It is the second part of my master project and finally I am going to map video compression algorithm on this template later.

The code can be synthesized by Xilinx EDK7.1 and ISE7.1. The simulator is ModelSim 6.1 starter version. Chipscope is used often to monitor and debug.

It can also be used as an IP core or library for other computing intensive applications with a little modification of bus interface.

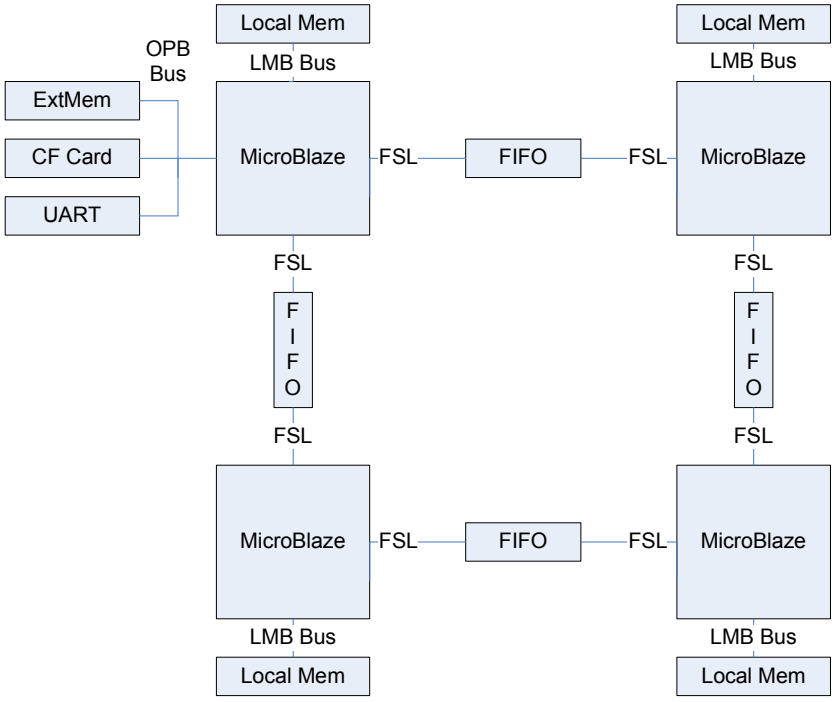
Architecture

1. Block Diagram

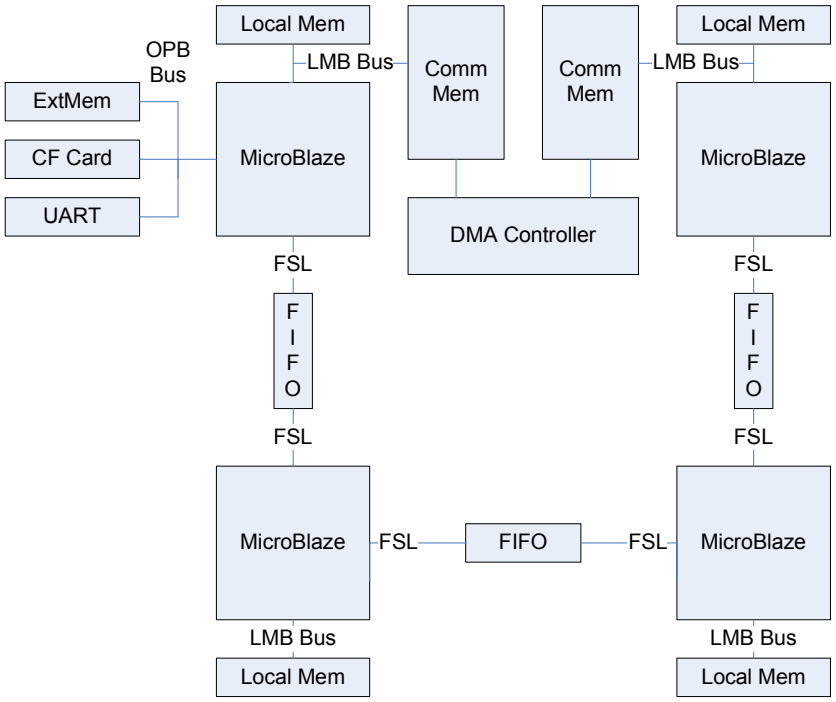


Roadmap

1. Setup four-processor testbench connected by FIFO and map JPEG encoder onto it.



2. Design a two-port DMA controller and replace one FIFO



Reference

1. http://www.opencores.org/projects.cgi/web/mb-jpeg/overview “jpeg codec based on Xilinx Microblaze processor”, Sun Wei, Joris van Emden, Marcel Lauwerijssen, Cristian Tena
2. http://sourceforge.net/projects/mb-jpeg “embedded JPEG codec library”, Sun Wei, Joris van Emden, Marcel Lauwerijssen, Cristian Tena