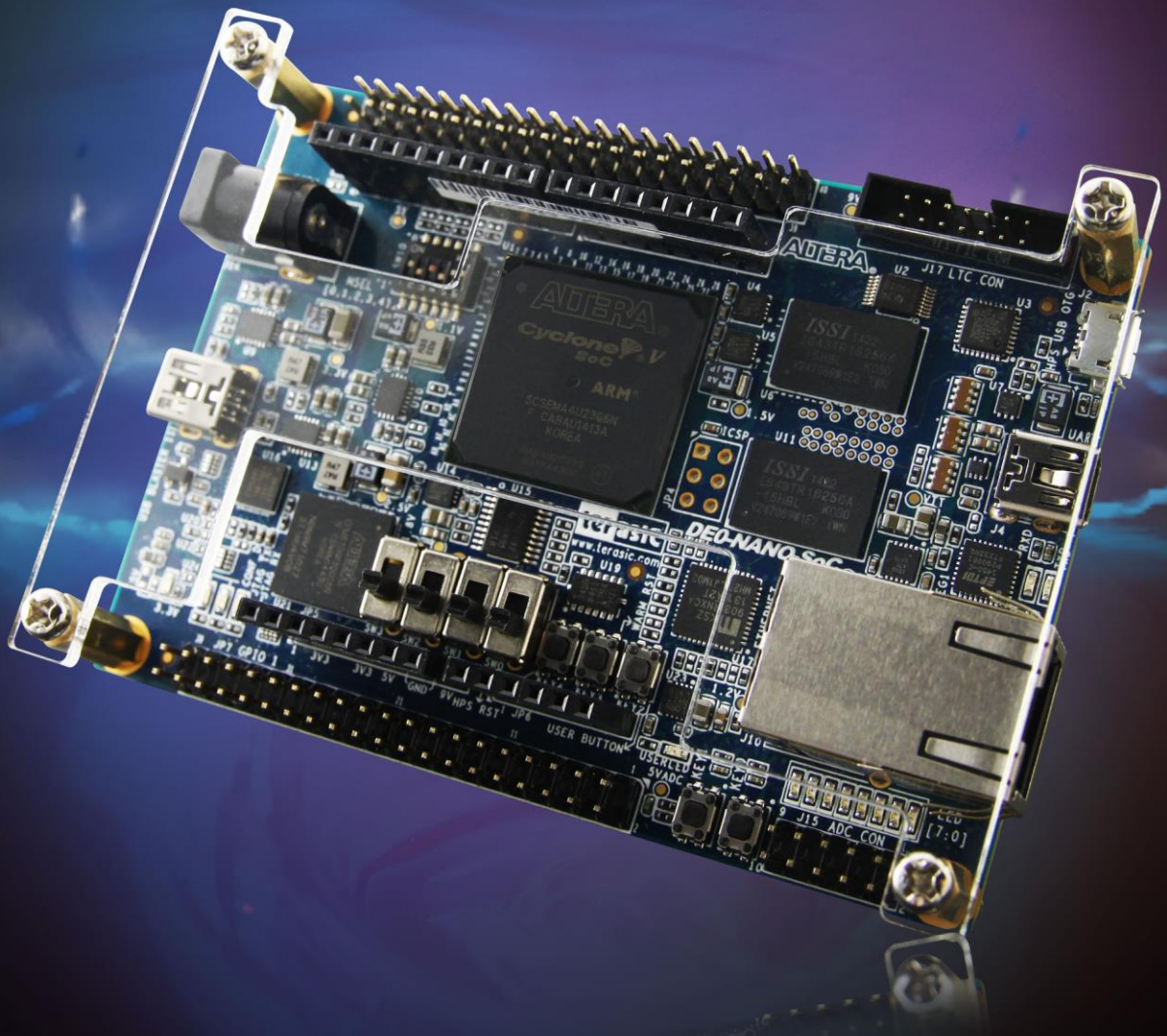
DE0-Nano-SoC

Getting Started Guide



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PROGRAM

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Chapter 1

About this Guide

The DE0-Nano-SoC Getting Started Guide contains a quick overview of the hardware and software setup including step-by-step procedures from installing the necessary software tools to using the DE0-Nano-SoC board. The main topics that this guide covers are listed below:

- Software Installation: Installing Quartus II and SoC EDS
- Development Board Setup: Powering on the DE0-Nano-SoC
- Perform FPGA System Test: Downloading a FPGA SRAM Object File (.sof)
- Running Linux on DE0-Nano-SoC Board

Chapter 2

Software Installation

2.1 Introduction

This section explains how to install the following software:

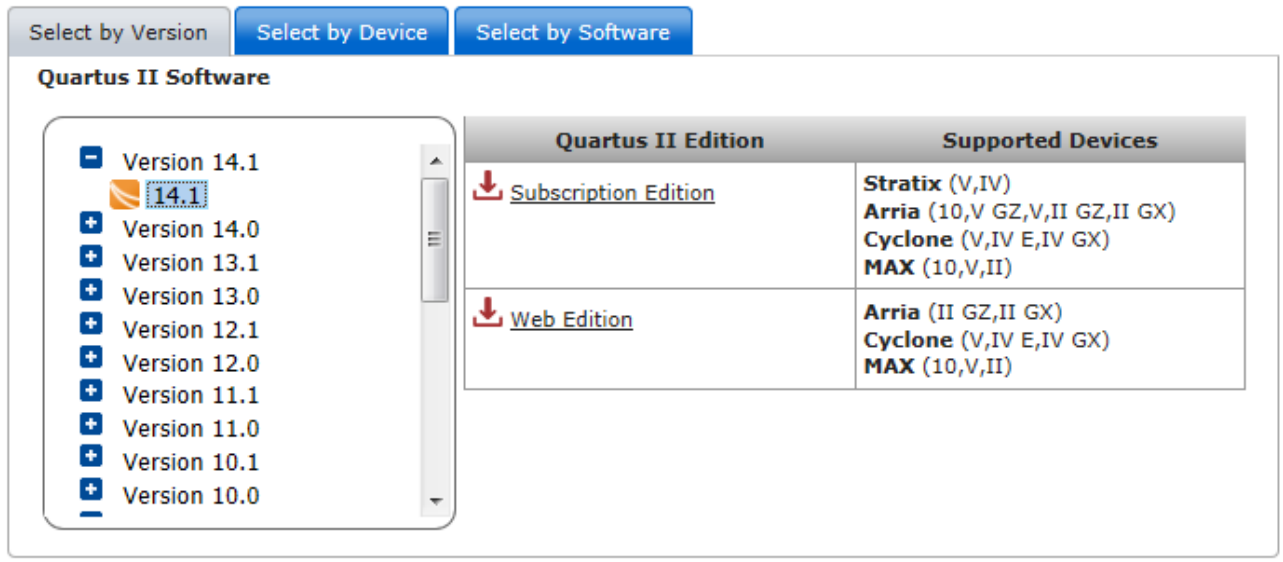
- Altera Quartus II software
- Altera SoC Embedded Design Suite

Note: 64-bit OS required

2.2 Installing Quartus II software

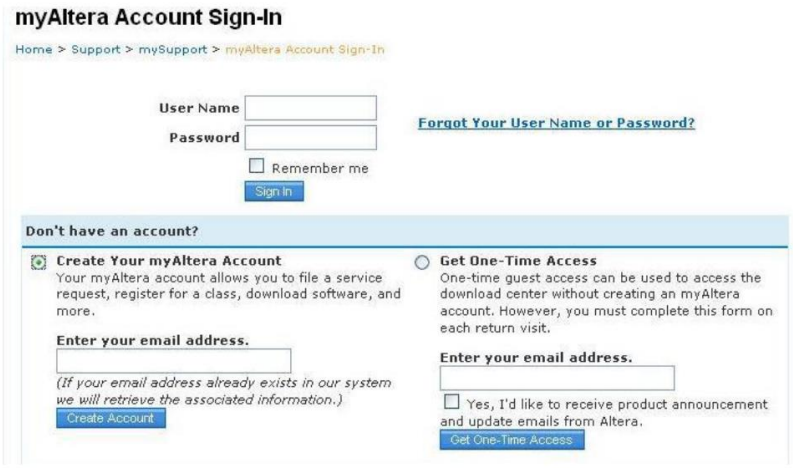
The Altera Complete Design Suite provides the necessary tools used for developing hardware and software solutions for Altera FPGAs. The Quartus II software is the primary FPGA development tool used to create reference designs along with the Nios II soft-core embedded processor integrated development environment

User can download the latest software from https://www.altera.com/download/dnl-index.jsp



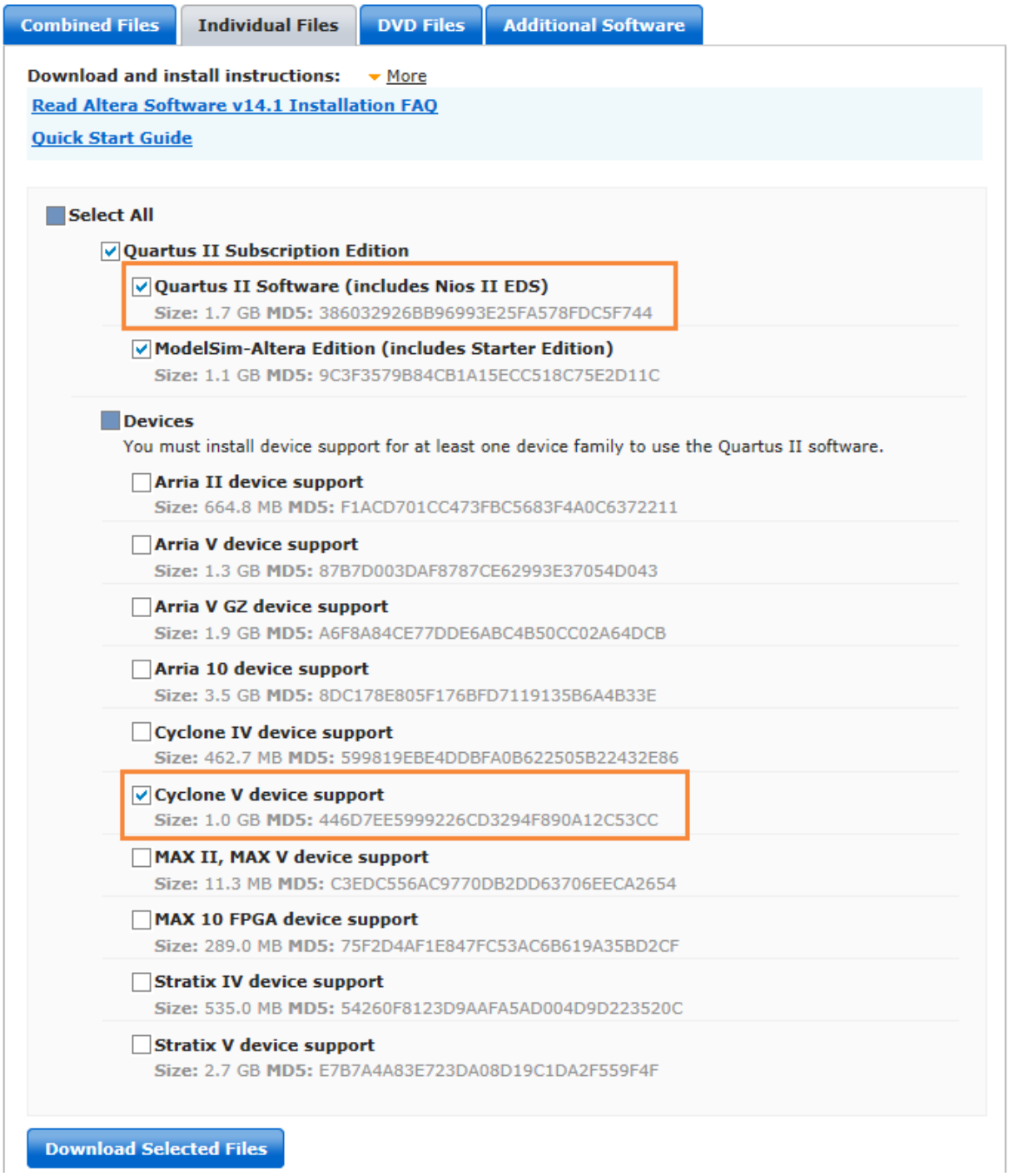
- If you choose to install the Subscription Edition, please note that a purchased license will be required. Please go to the following link for more information on the Subscription Edition: http://www.altera.com/products/software/quartus-ii/subscription-edition/qts-se-index.html

- Select the latest software version for Subscription Edition or web Edition will into "myAltera Account Sign-In" page



- Use your existing login, or get a one-time Access.

- Download files from subscription or web edition page. You must download the Quartus II Software (includes Nios II EDS) and Cyclone V device support (includes all variations).



- After the file is downloaded on the computer, select the *.exe file, and install the software. All of the defaults are to be used.

2.3 Installing Altera SoC Embedded Design Suite

The Altera SoC Embedded Design Suite (EDS) contains development tools, utility programs, run-time software, and application examples to enable embedded development on the Altera SoC hardware platform. User can use the Altera SoC EDS to develop firmware and application software. Users can download the software from the Altera webpage:
https://www.altera.com/download/software/soc-eds

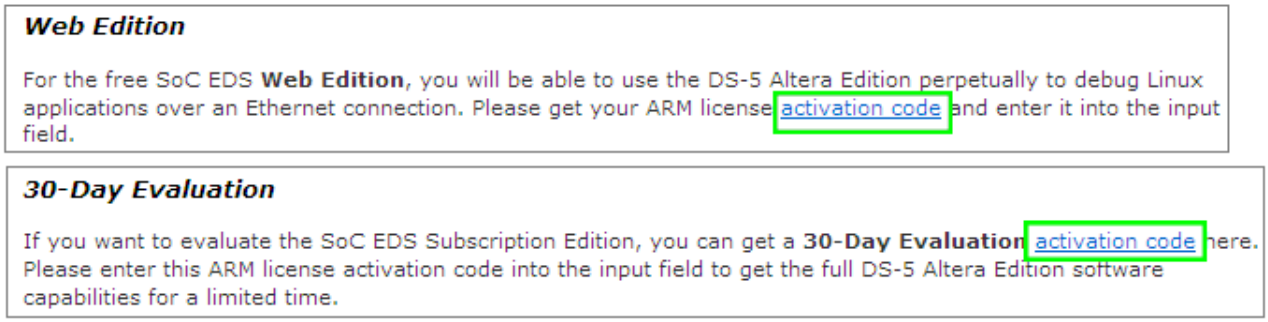
After you have installed the SoC Embedded Design Suite (EDS), you can start the ARM® Development Studio 5 (DS-5™) Altera Edition software. If this is your first time using the DS-5, a popup dialog will automatically ask if you wish to open the license manager.

For the free SoC EDS **Web Edition**, you will be able to use the DS-5 Altera Edition perpetually to debug Linux applications over an Ethernet connection. If you have purchased the SoC EDS **Subscription Edition**, you would have received an ARM license serial number. Or you can obtain a 30-day evaluation license. The following steps show how to obtain a web edition license or a 30-day evaluation license for subscription edition. If the user does not need to design in the ARM DS-5, please skip the section below.

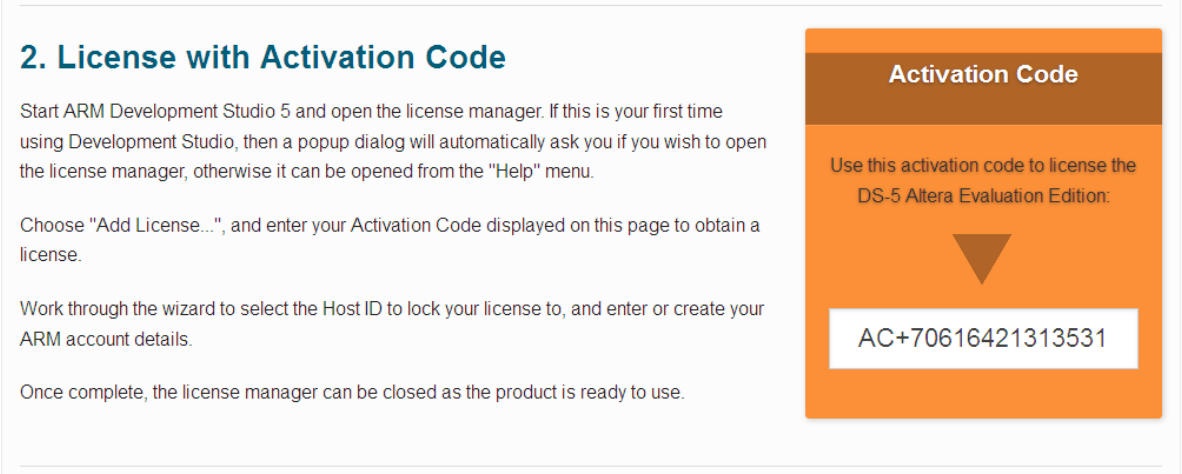
Obtain a Web Edition license or a 30-day evaluation license for Subscription Edition

In the section, we will introduce how to get a serial number from Altera website to active the ARM development Studio 5 (DS-5) Toolkit.

- Visit the website: Altera "SoC Embedded Design Suite" (https://www.altera.com/download/software/soc-eds)
- Browse the webpage to get the same information as the picture shows below, click the “activation code (Web Edition or 30-Day Evaluation) to link to the webpage: “DS-5 Community Edition".

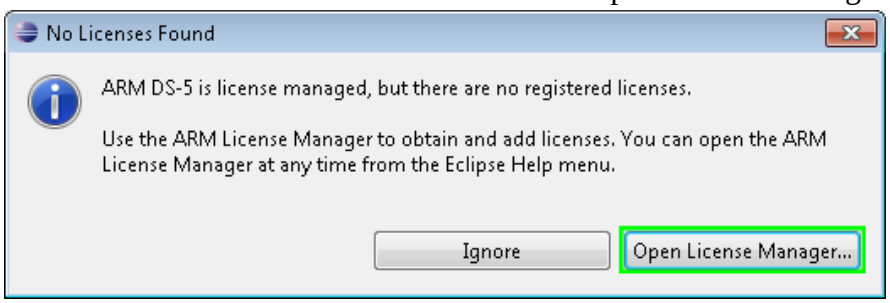


- In this page, record the Activation code displayed on the right of the picture below, such as "AC+70616421313438" as shown in the picture below.

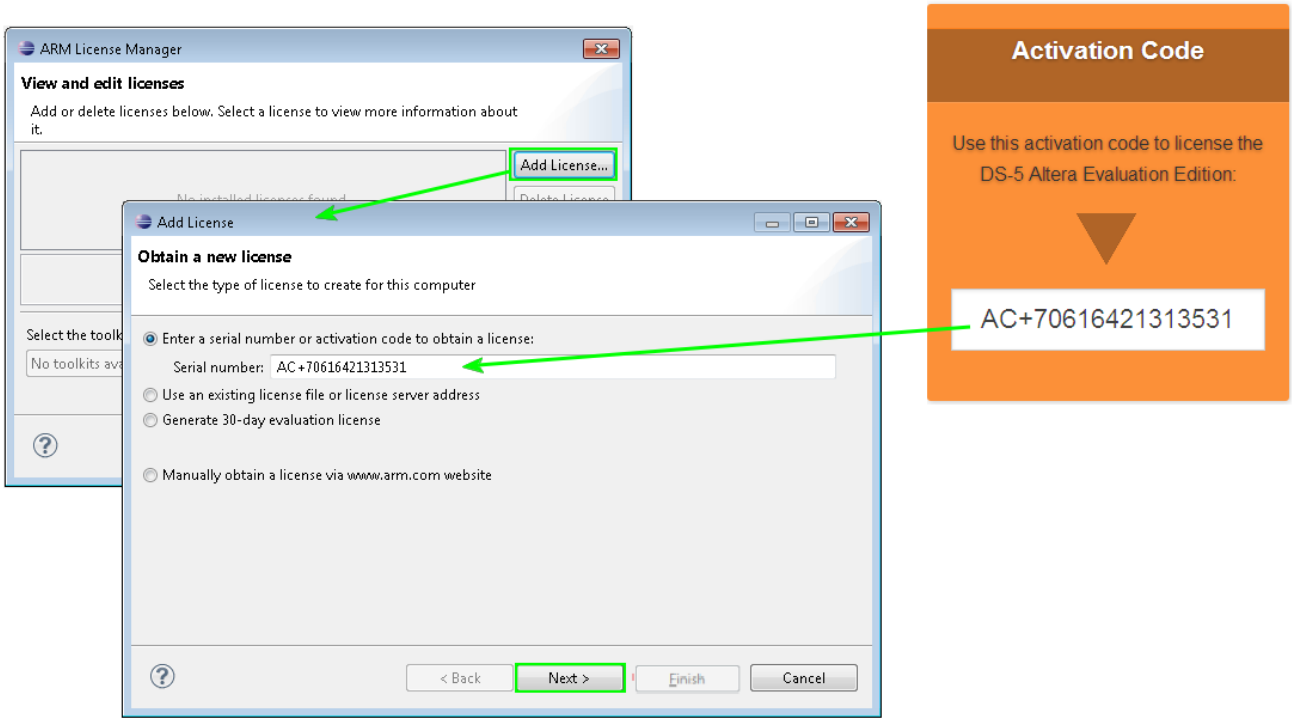


After recording this Activation code, we will continue to introduce how to active DS-5 by using this code. The steps are as follows:

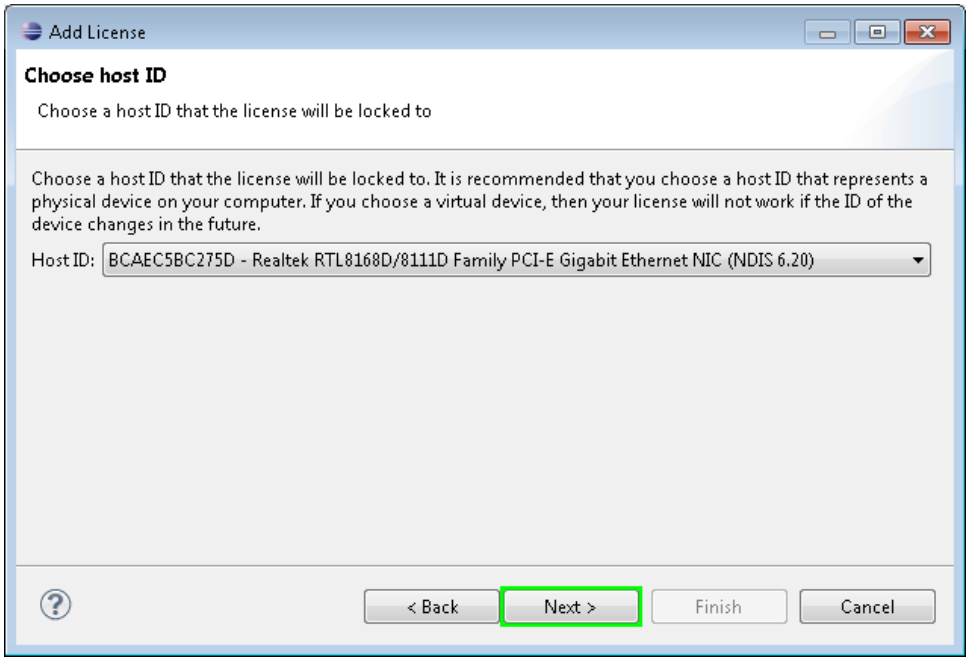
- Launch DS-5. Start --> All Programs --> ARM DS-5 --> Eclipse for DS-5
- A Workspace Launcher window will ask you to select a workspace.
- Press OK to select the default
- You will see a "No Licenses Found" Window. Select Open License Manager



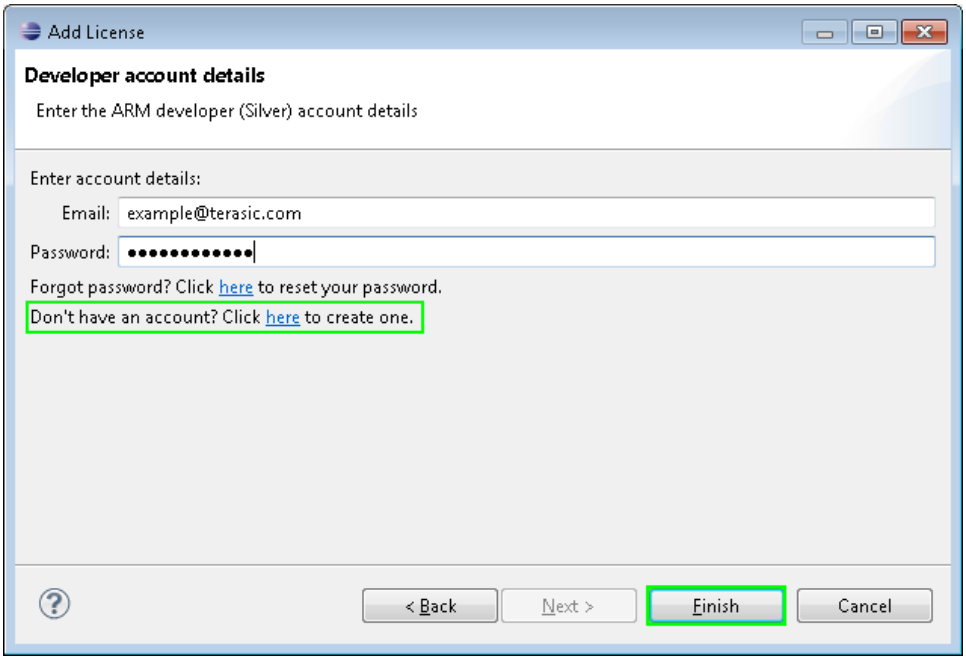
- Press the Add License Button in the ARM License Manager and Enter the activation code that you received earlier. Press the Next Button.



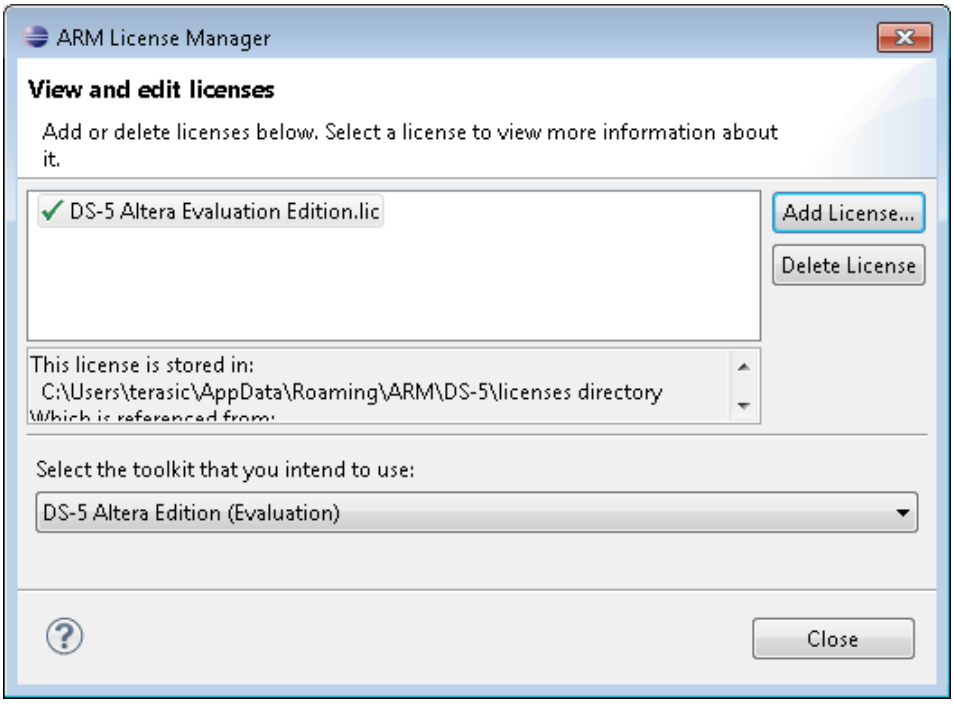
- Use the pull down menu to select a host ID. Press the Next button.



- Enter your ARM account email address and password.



- If you do not have an account then click on the link to create one.
- Press the Finish button.



- A web edition license or 30-day evaluation license for subscription edition is now successfully installed.

Chapter 3

Development Board Setup

3.1 Introduction

The instructions in this section explain how to set up the DE0-Nano-SoC development board. The following pictures show the board overview of DE0-Nano-SoC board.

3.2 Default MSEL Settings

The FPGA Configuration Mode Switch (MSEL) shown in **Figure 3-1** is by default set to 10010 (MSEL[4:0] = 10010). The setting corresponds to FPGA working in ASx4 mode.

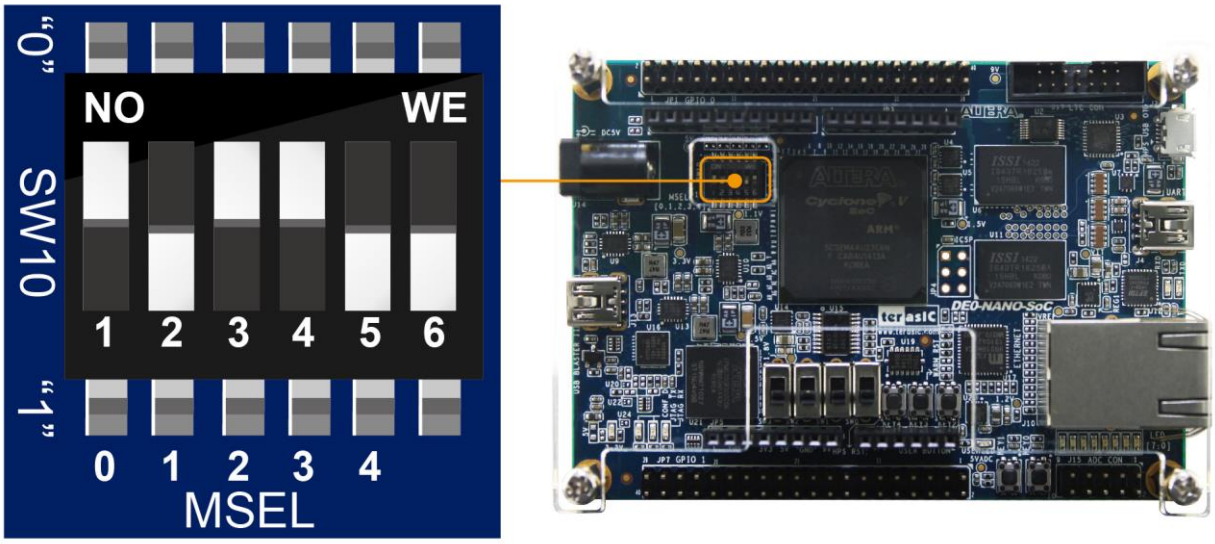


Figure 3-1 FPGA Configuration Mode Switch set in ASx4 Mode

3.3 USB and Power Cables

Cable connections are shown in **Figure 3-2** as below:

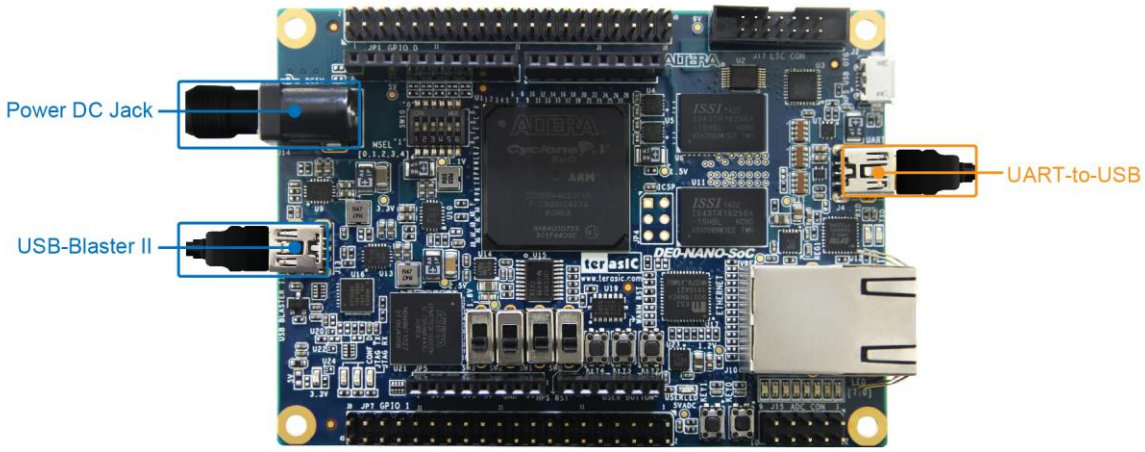


Figure 3-2 USB and Power Cables

3.4 Powering up the DE0-Nano-SoC Board

To power-up the board, perform the following steps below:

1. Connect the provided power cord to the power supply and plug the cord into a power outlet (verify the voltage supplied is the same as the specification on the power supply).

2. Connect the supplied DE0-Nano-SoC power adapter to the power connector (J14) on the DE0-Nano-SoC board. At this point, you should see the 3.3V indicator LED (LED9) turned on.

Chapter 4

Performing a FPGA System Test

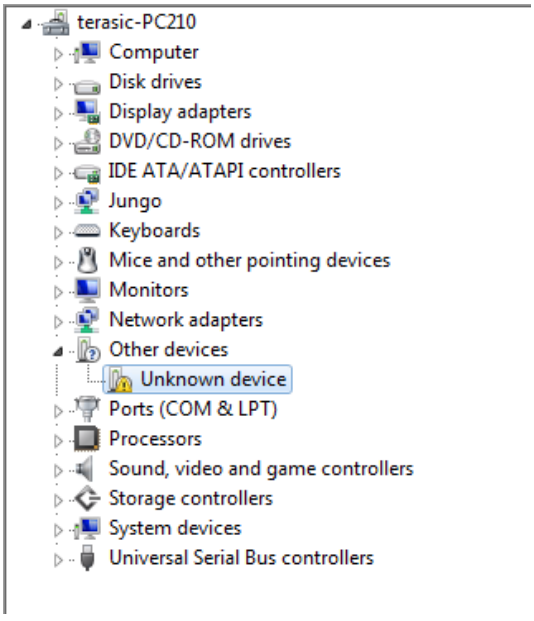
4.1 Introduction

This chapter shows how to install the USB-Blaster II driver and download a FPGA SRAM Object (.sof) file to your FPGA board.

4.2 Installing the USB-Blaster II Driver

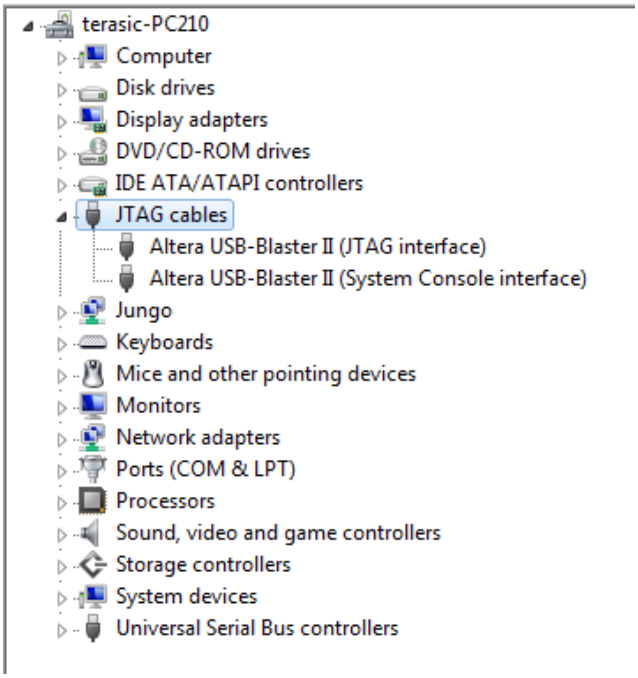
The steps below outline how to install the USB-Blaster II driver.

1. Connect your computer to the development board by plugging the USB cable into the USB connector (J13) of DE0-Nan0-SoC (connection shown in **Figure 3-2**)
2. Power up the board and open the device manager in Windows. You will find an unknown device.



3. Select the unknown device to update the driver software. The driver file is in the \<Quartus II installation directory>\drivers\ usb-blaster-ii directory.

4. After the driver is installed correctly, the device is recognized as Altera USB-Blaster II as shown in following picture.

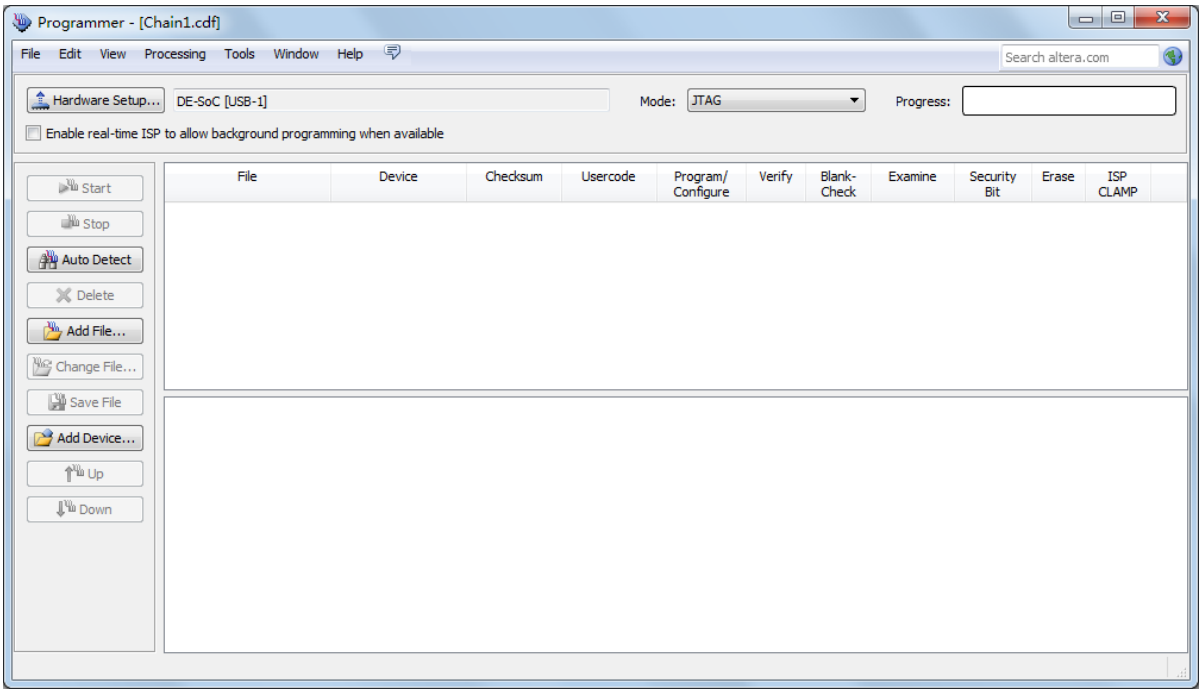


4.3 Downloading a FPGA SRAM Object File

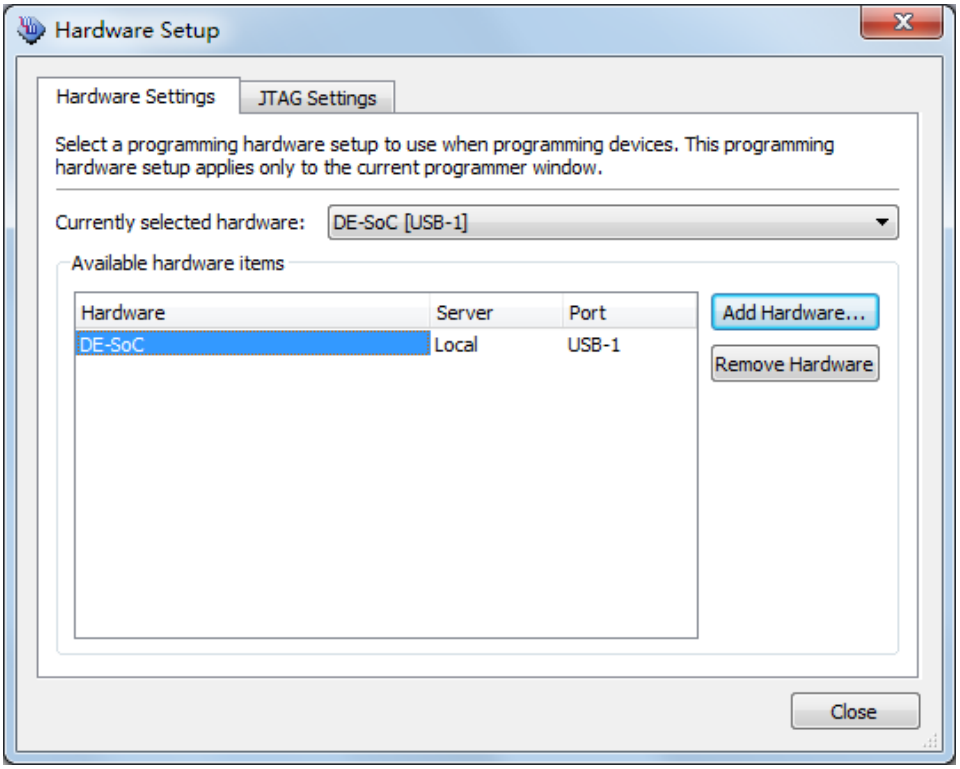
The Quartus II Programmer is used to configure the FPGA with a specific .sof file. Before configuring the FPGA, ensure that the Quartus II software and the USB-Blaster II driver are installed on the host computer.

If users would like to program their SRAM Object File (.sof) into the Cyclone V SOC FPGA device on the DE0-Nano-SoC board, There are two devices (FPGA and HPS) on the JTAG Chain, the configure flow is different from the one used with DE0-Nano. The following shows the programming flow with JTAG mode step by step.

1. Connect your computer to the DE0-Nano-SoC board by plugging the USB cable into the USB connector (J13) of DE0-Nano-SoC and power up the board (details shown in **Chapter 3**)
2. Open the Quartus II software and select Tools > Programmer. The Programmer window will appear.

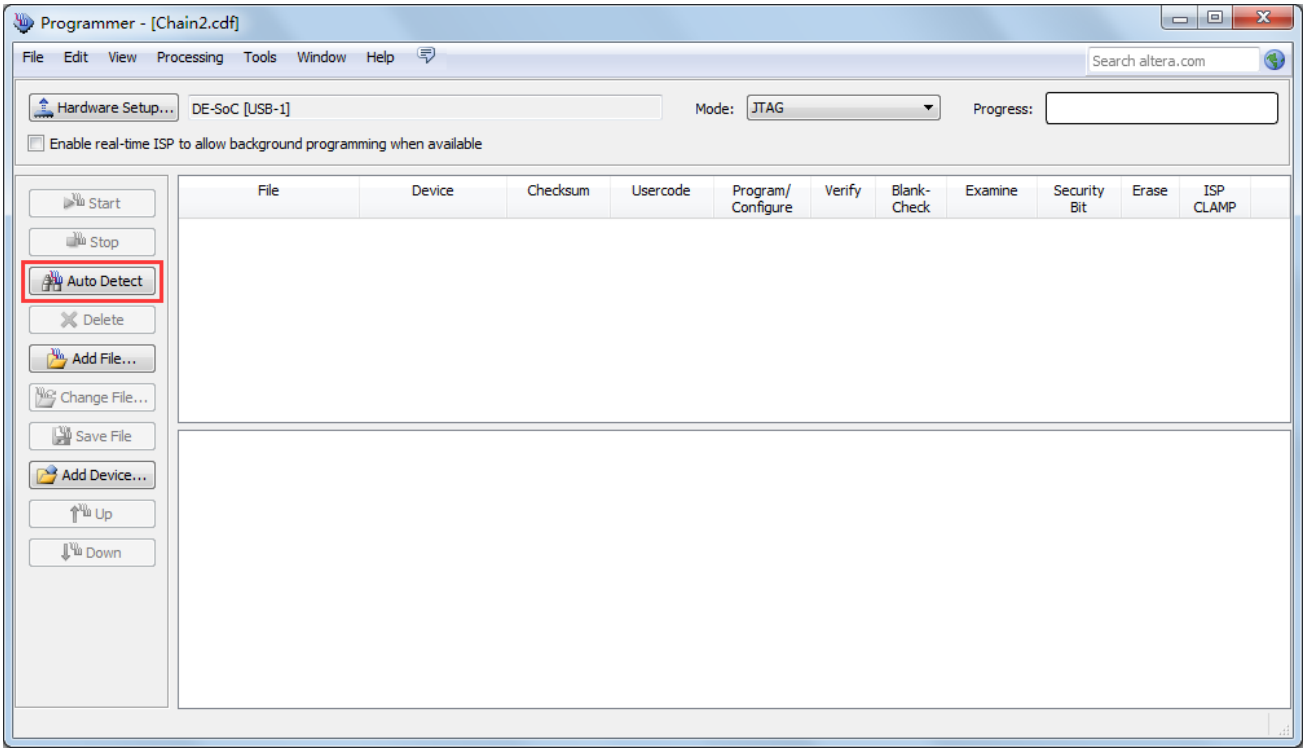


3. Click **Hardware Setup**.
4. If **DE-SoC [USB-1]** does not appear under **Currently Selected Hardware**, select that option and click **Close** as shown below.

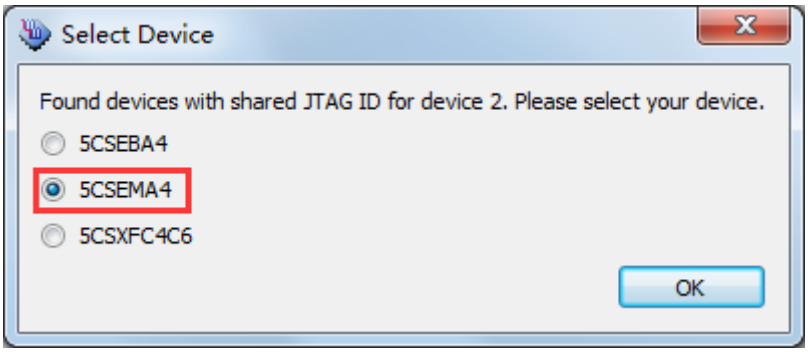


If the USB-Blaster II does not appear under hardware options list, please confirm if the USB-Blaster II driver has been correctly installed, and the USB cable has been properly connected between the DE0-Nano-SoC board and host computer.

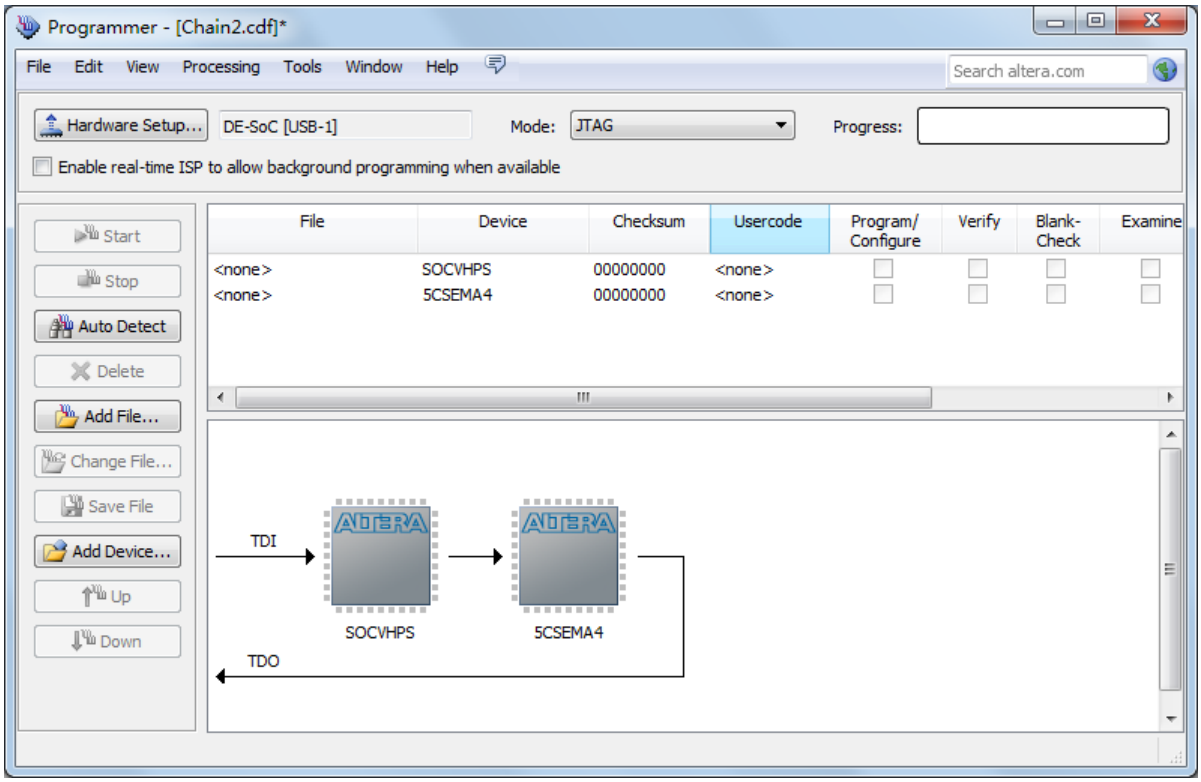
5. Click "Auto Detect".



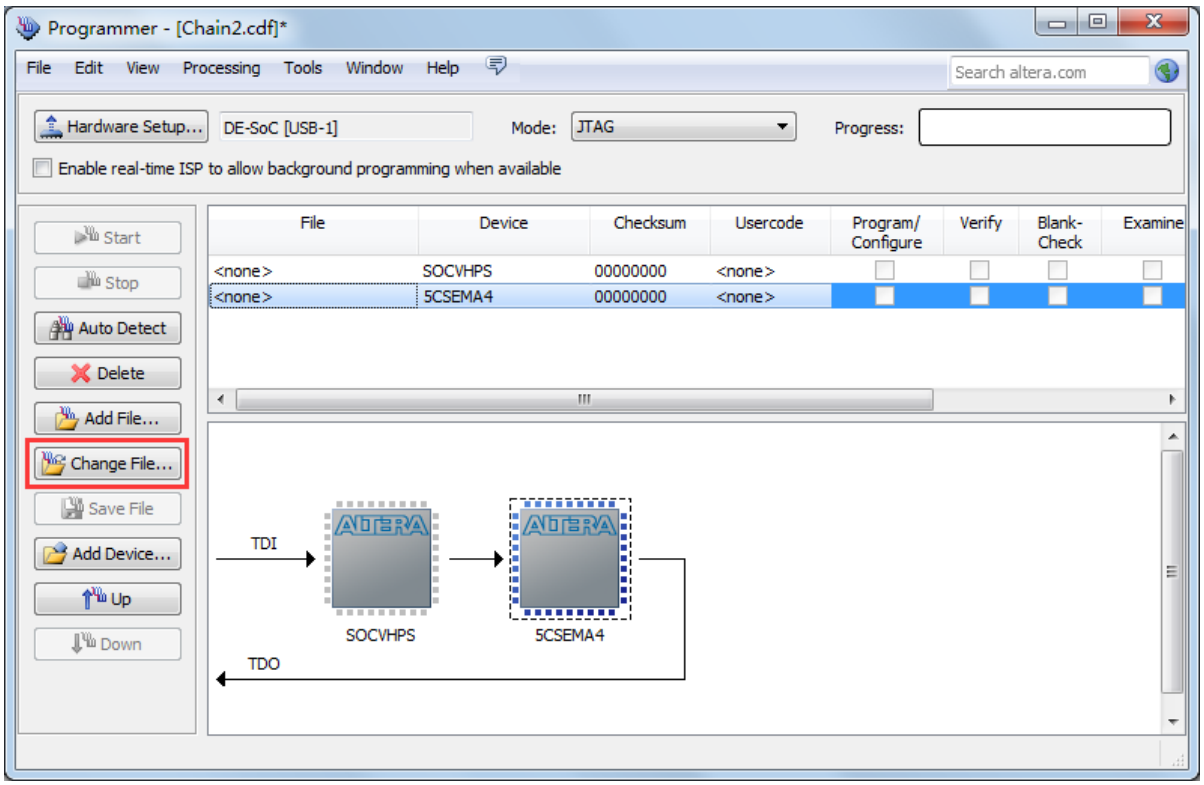
6. Select the device associated with the board



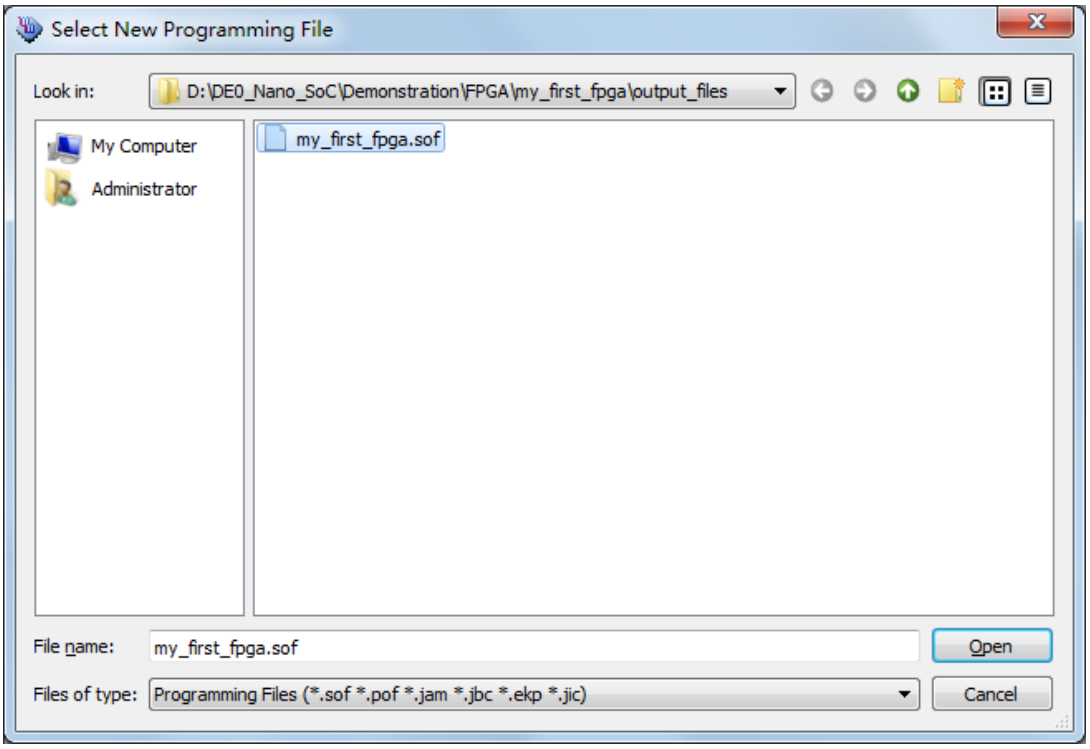
7. FPGA and HPS devices are all show in the jtag chain.



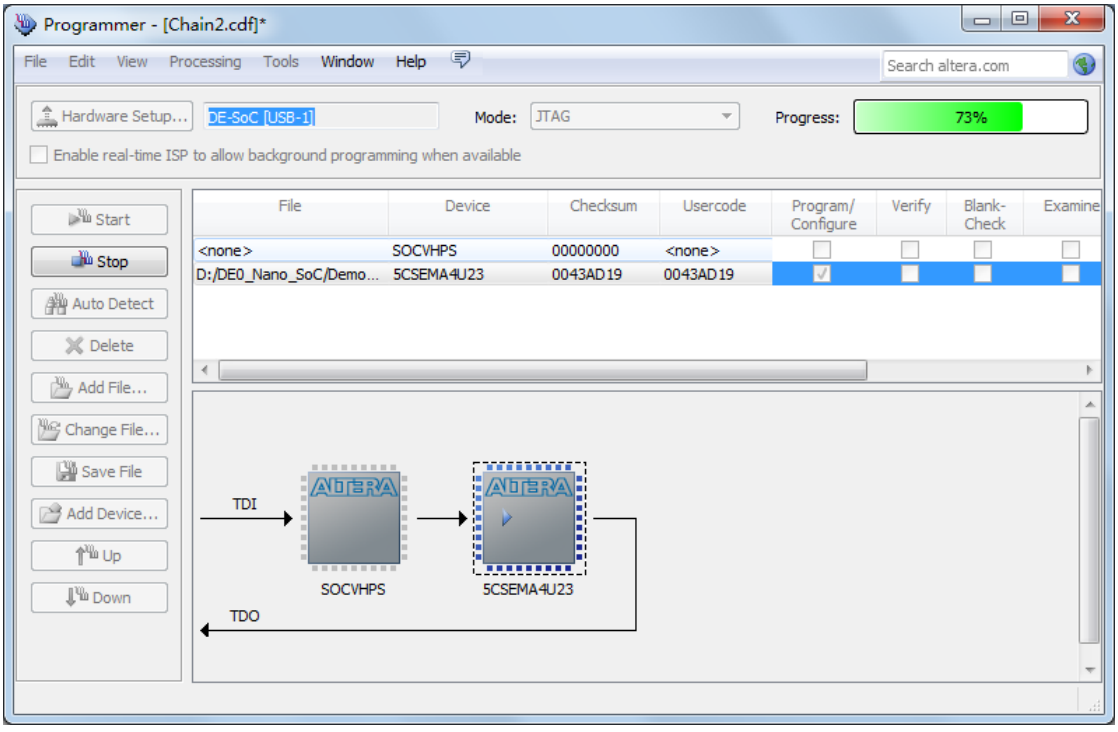
8. Click the FPGA device, click “Change File..”, and then select .sof file for FPGA



9. Select \<CD directory>\Demonstration\FPGA\my_first_fpga\ output_files\my_first_fpga.sof.



10. Click “Program/Configure” check box, and then click “Start” button to download .sof file into FPGA



Chapter 5

Running Linux on the DE0-Nano-SoC board

5.1 Introduction

This chapter demonstrates how to create a Micro SD card image, set up a UART Terminal, and run Linux on DE0-Nano-SoC Board. User can download the latest SD Card image file from Terasic's website (Choose **Linux Console** in Linux BSP (Board Support Package)): http://cd_de0-nano-soc.terasic.com.

5.2 Creating a microSD Card Image

To program a microSD card Linux image you can use a free tool called **Win32DiskImager.exe** from http://sourceforge.net/projects/win32diskimager/ on a Windows machine.

■ MicroSD Specification

- Capacity: 4GB minimum
- Speed: Class 4 (at least)

■ Pre-built SD Card Image

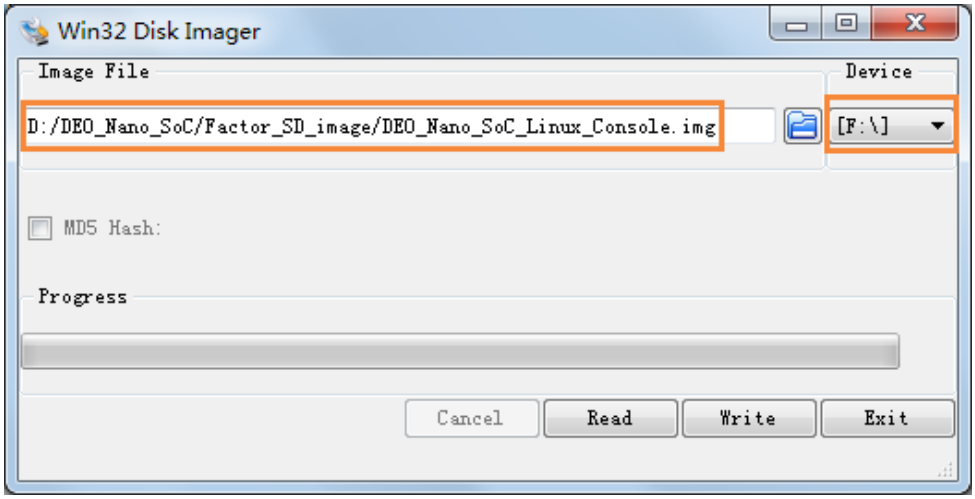
The pre-built binaries are delivered as an archive named DE0_Nano_SoC_Linux_Console.img. This SD card image file contains all the items that are needed to run Linux on DE0_NanoSoC board. (You can download the compressed file from the link: http://www.terasic.com/downloads/cd-rom/de0-nano-soc/linux_BSP/ DE0_Nano_SoC_Linux_Console.zip. And extract file to get the image file after downloading)

- SPL Pre-loader

- U-boot
- Device Tree Blob
- Linux Kernel
- Linux Root File system

The SD card image file needs to be programmed to a microSD card before it can be used. The steps below present how to create microSD card on a windows machine using Win32DiskImager.exe.

1. Connect the microSD card to a Windows PC
2. Execute Win32DiskImager.exe
3. Select the image file for microSD card
4. Select the microSD card device



5. Click “write” to start writing the image file to the microSD card. Wait until the image is written successfully.

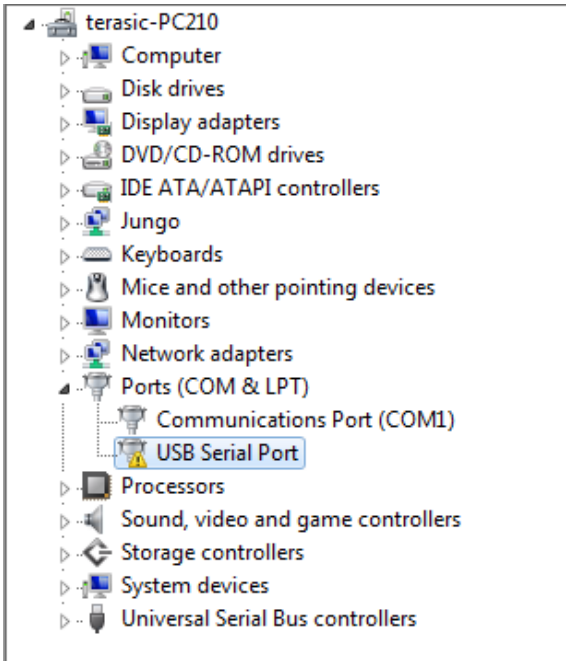
5.3 Setting Up UART Terminal

This section presents how to install the drivers for the USB to UART chip on the DE0-Nano-SoC board and set up the UART terminal on your host PC. The DE0-Nano-SoC board communicates with the PC through the micro USB connector J4.You should install the USB to UART driver and configure the UART terminal before you run Linux on the board.

■ Installing the Driver

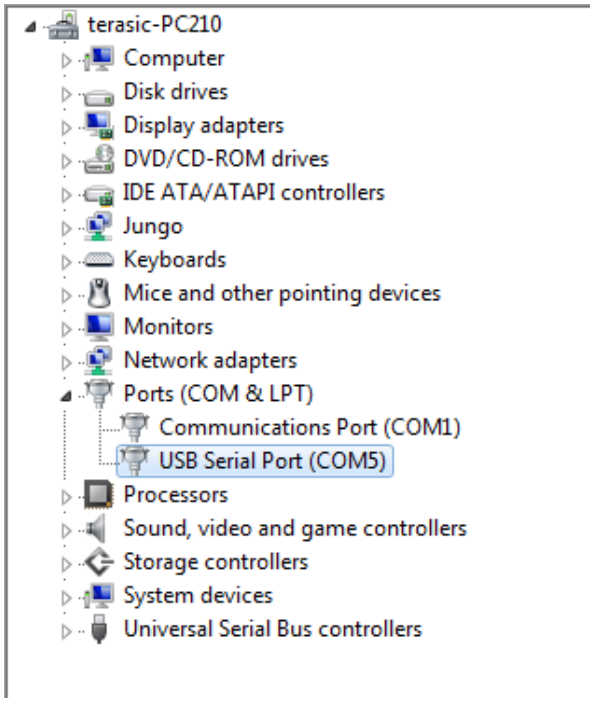
This section presents how to install the drivers for USB to UART communication. The necessary steps on Windows 7 are:

1. Connect your computer to the development board by plugging the USB cable into the micro USB connector (J4) of DE0-Nano-SoC (connection shown in **Figure 3-2**)
2. Power on the board then open the computer device manager in Windows. You will find an unrecognized FT232R USB UART.



Select the FT232R USB UART to update the driver software. The driver can be downloaded from http://www.ftdichip.com/Drivers/VCP.htm.

3. After the driver has been installed correctly, the USB Serial Port is recognized as a port such as ***COM5*** *(Open the device manager to know which COM port assigned in your computer)*



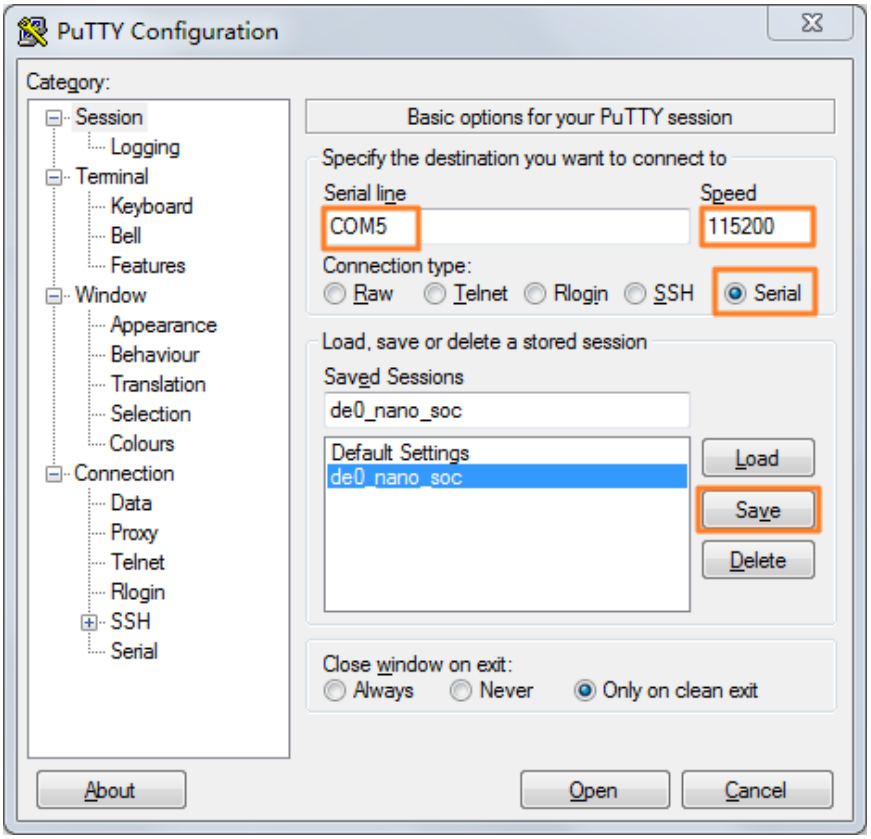
4. Now you can power off the DE0-Nano-SoC board

■ Configure UART terminal UART terminal spec:

- 115200 baud rate
- no parity
- 1 stop bit
- no flow control settings

The following steps present how to configure a PuTTY terminal window (can be downloaded from the link: http://the.earth.li/~sgtatham/putty/latest/x86/putty.exe)

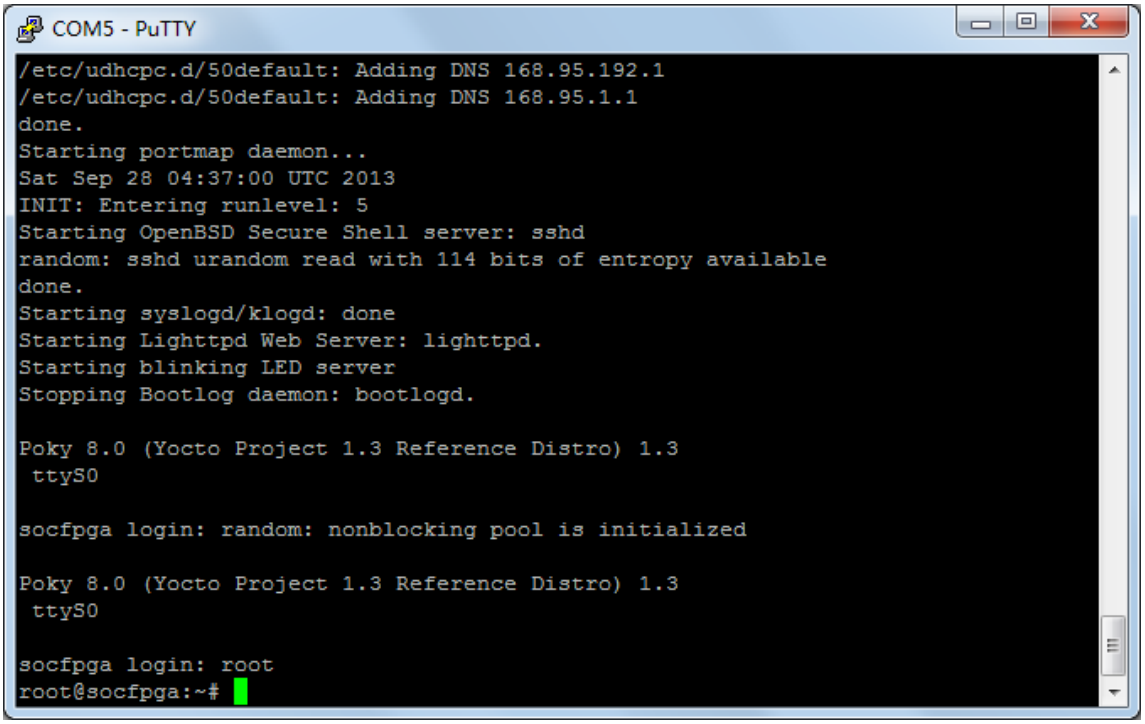
1. Open putty.exe, click ***Serial*** go to a serial configure interface.
2. Configure the window like the flowing picture and click save button to save the configuration.



5.4 Running Linux on DE0-Nano-SoC board

This section presents how to run the pre-built Linux images on the DE0-Nano-SoC board. You can run the Linux by following the steps below:

1. Insert the microSD card with the pre-built image into the board (See Section 5.2 to prepare a microSD card)
2. Power up the board (See Chapter 3 for details)
3. Open putty.exe, select the saved configuration **de0_nano_soc** and click open button.
4. After a successful boot, the Linux will ask for the login name. Type **root** and press **Enter** to login to the system.


COM5 - PuTTY
/etc/udhcpc.d/50default: Adding DNS 168.95.192.1
/etc/udhcpc.d/50default: Adding DNS 168.95.1.1
done.
Starting portmap daemon...
Sat Sep 28 04:37:00 UTC 2013
INIT: Entering runlevel: 5
Starting OpenBSD Secure Shell server: sshd
random: sshd urandom read with 114 bits of entropy available
done.
Starting syslogd/klogd: done
Starting Lighttpd Web Server: lighttpd.
Starting blinking LED server
Stopping Bootlog daemon: bootlogd.
Poky 8.0 (Yocto Project 1.3 Reference Distro) 1.3
ttyS0
socfpga login: random: nonblocking pool is initialized
Poky 8.0 (Yocto Project 1.3 Reference Distro) 1.3
ttyS0
socfpga login: root
root@socfpga:~#

Additional Information

Getting Help

Here are the addresses where you can get help if you encounter problems:

- Terasic Technologies
  9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan, 30070
  Email: **support@terasic.com**
  Web: **www.terasic.com**

Revision History

Date	Version	Changes
2015.01.08	V1.0	First Version
2015.05.18	V1.1	Minor corrections: fixing typos and broken links