Configuring the Xilinx Spartan-6 LX9 MicroBoard

Version 13.2.1

Revision History

Version	Description	Date
1.1	Initial release for ISE 13.1 and 12.x	3/7/11
1.2	Eliminated redundant step in Appendix A	3/22/11
1.3	Added steps to open Windows Device Manager. Added link for MCS creation instructions, Tested fully against Windows7,64-bit.	4/18/11
13.2.1	Updated for IDS 13.2	9/1/11

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Requirements

The following items are required for configuration and programming of the FPGA and attached serial Flash.

Software

The following software setup is required to test this reference design:

- Windows XP or Windows 7
- Xilinx ISE WebPack version 13.2

Hardware

The hardware setup used by this reference design includes:

- Computer with a minimum of 300-900 MB (depending on O/S) to complete an XC6SLX9 design[1]
- Avnet Spartan-6 LX9 MicroBoard Kit
  - Avnet Spartan-6 LX9 MicroBoard
  - USB Extension cable (if necessary)
- Recommended: Digilent JTAG HS1 Programming Cable or Xilinx JTAG Programming Cable.

Recommended Reading

Available from Avnet: *http://em.avnet.com/s6microboard*

- The hardware used on the Spartan-6 LX9 MicroBoard is described in detail in Avnet document, *Spartan-6 LX9 MicroBoard User Guide*.

Available from Xilinx: *http://www.xilinx.com/support/documentation/spartan-6.htm*

- Details on the Spartan-6 FPGA family are included in the following Xilinx documents:
  - *Spartan-6 Family Overview (DS160)*
  - *Spartan-6 FPGA Configuration User Guide (UG380)*

[1] Refer to www.xilinx.com/ise/products/memory.htm

Overview

The Spartan-6 LX9 MicroBoard has two external interfaces for configuring the FPGA. There is a traditional Platform Cable JTAG header on the bottom of the board (J6) and a new on-board USB-to-JTAG circuit. Both interfaces offer the ability to configure the FPGA and program the on-board serial flash, as well as other Xilinx JTAG functions like ChipScope and SDK Debugger.

The FPGA is pre-set to Master Serial Mode, which means it initiates configuration upon power-up and generates a configuration clock. It reads configuration data from an on-board Micron 128Mb Serial Flash memory. This flash can be programmed through either of the two aforementioned interfaces. This document will illustrate how to use these interfaces to configure the FPGA and program the on-board serial flash.

Note: Throughout this document, the word '**configuration**' applies to downloading a bitstream to the FPGA whereas the word '**programming**' applies to downloading a flash image to the on-board serial flash.

This board provides three ways to program the serial flash:

1. iMPACT Indirect SPI Programming via on-board USB-to-JTAG (Procedure #1)
2. SFUTIL Direct SPI Programming via on-board USB-to-SPI (Procedure #2)
3. iMPACT Indirect SPI Programming via external JTAG cable (Procedure #3)

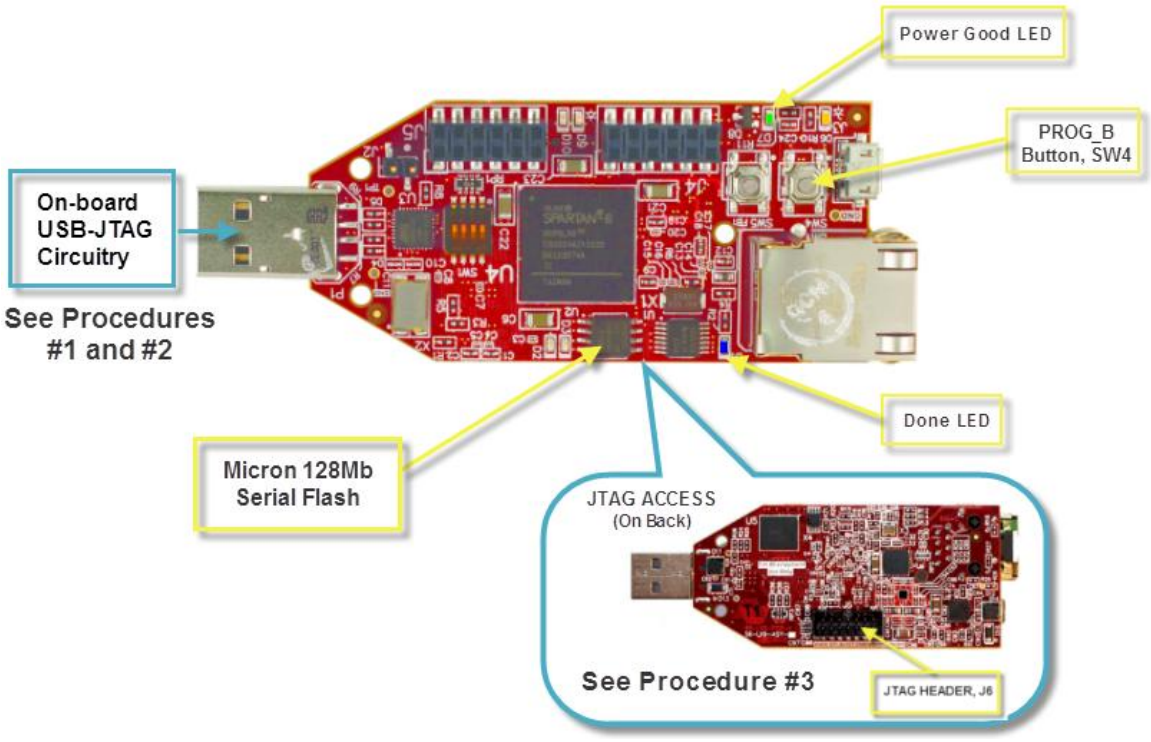

Figure 1 - Spartan-6 LX9 MicroBoard Configuration Interfaces

Configuration and Programming via the on-board USB-JTAG Circuitry

This board incorporates an on-board USB-JTAG access circuit that eliminates the need for an external Xilinx JTAG cable. The on-board JTAG is compatible with all Xilinx tools, including iMPACT, ChipScope, and SDK Debugger. This circuit can be utilized in your design if you would like JTAG access and Xilinx tool support in your product. Digilent sells this solution to customers who wish to have this capability on their own designs.

The on-board USB programming circuit interfaces to a PC via an Atmel AT90USB162 Full-Speed USB microcontroller. This microcontroller is pre-programmed by Digilent to translate USB-to-JTAG and thus providing access to the on-board JTAG chain. Since this is a Full-Speed USB interface, it will not perform as fast as Hi-Speed USB interfaces. So if faster performance is required for programming or debugging, the Xilinx Platform Cables or a High-Speed Digilent USB cable (JTAG-HS1) can be used.

There are two methods of using this on-board USB-JTAG circuitry. One uses iMPACT software that is included with Xilinx ISE design tools. This method gives you all the access to the FPGA that the Platform Cable solution provides. The other method uses a Digilent programming utility called SFUTIL.exe, which is run via a command line batch file. This utility only programs the attached serial flash and is much faster than using the iMPACT GUI.

Procedure 1: Configuration and Programming using iMPACT with the on-board USB-JTAG Circuitry

1. Make sure no Xilinx or Digilent programming cable is attached to the PC.

Connect the Spartan-6 LX9 MicroBoard to the host PC by plugging it into an open USB port or by using the USB extension cable (Type A Male to Type A Female) as show below. **NOTE:** The first time the LX9 MicroBoard is connected to a PC, the Digilent drivers may install.

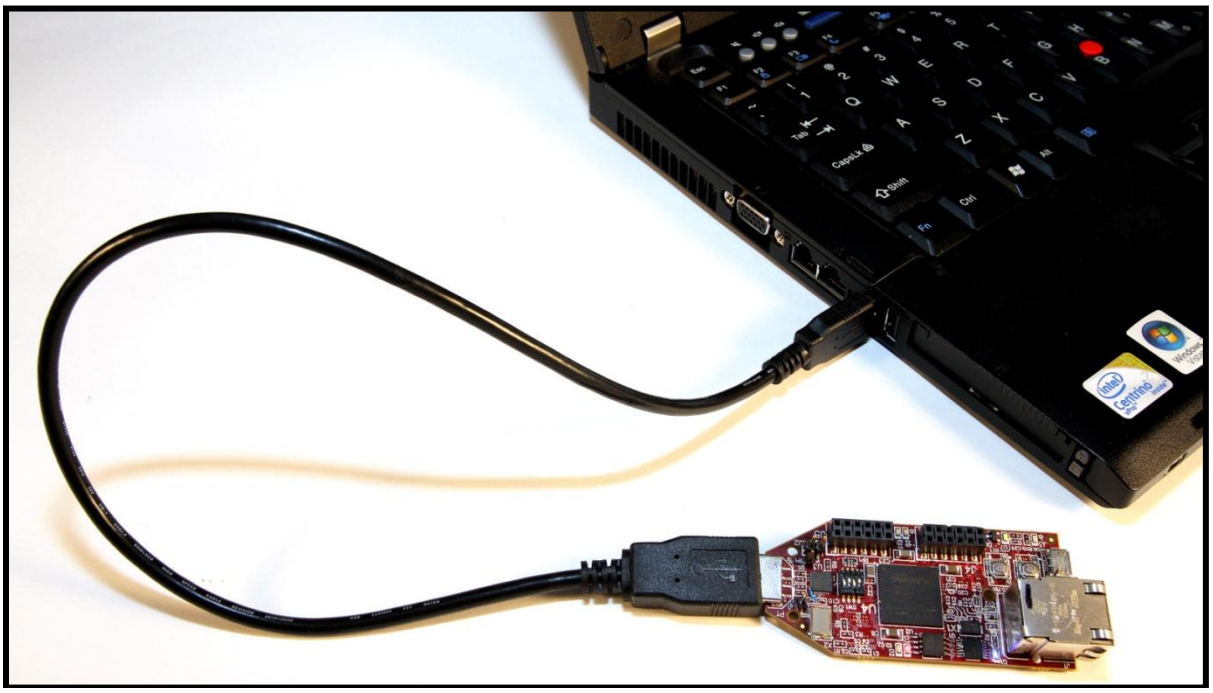

Figure 2 - Connect USB-JTAG programming interface to host PC

2. Check in the Windows Device Manager to ensure the Digilent USB Driver is available. To open Windows Device Manager, select **Start → Control Panel → System (System and Security for Windows 7).** For WinXP, In the System Properties window, select the **Hardware** tab then click on **Device Manager**. For Windows 7, just click on **Device Manager**. Expand Universal Serial Bus Controllers, if the Digilent USB device is not listed, please follow the steps in the section, Download and Install the Digilent Drivers:

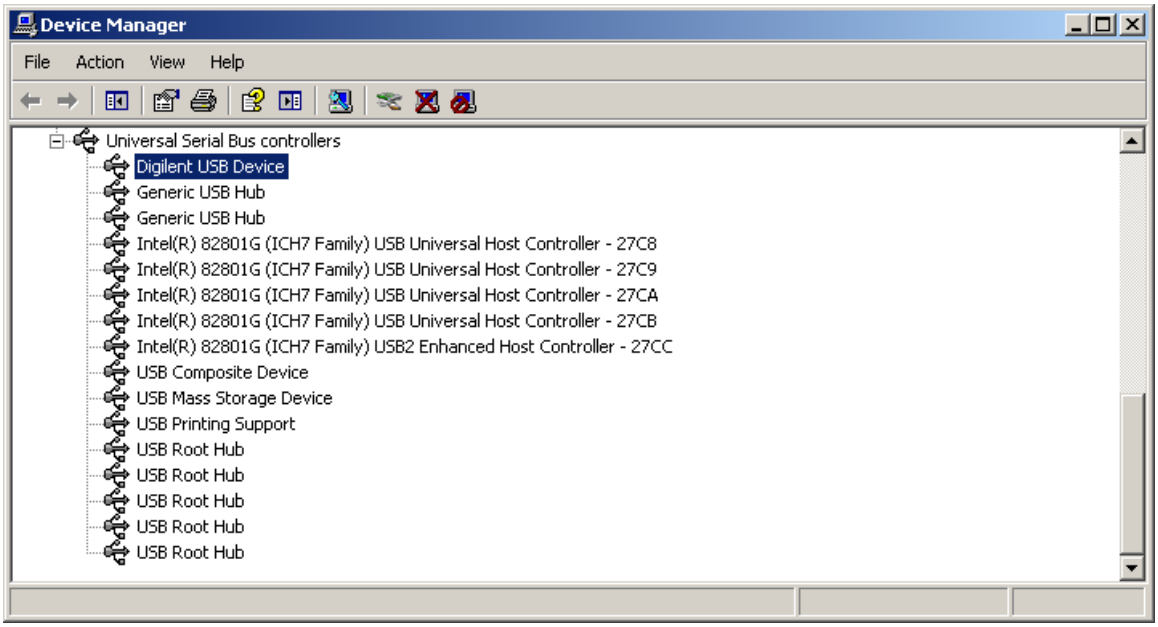

Figure 3 - Windows Device Manager

3. Launch iMPACT 13.2 by selecting **Start → Programs → Xilinx ISE Design Suite 13.2 → ISE Design Tools → Tools → iMPACT**.

4. A pop-up window will ask, "Do you want the system to automatically create and save a project file for you?" Select **No**.

5. Select **create a new project (.ipf)** at the New iMPACT Project Wizard. Click **Browse** to select directory to save this file. Click **OK**.

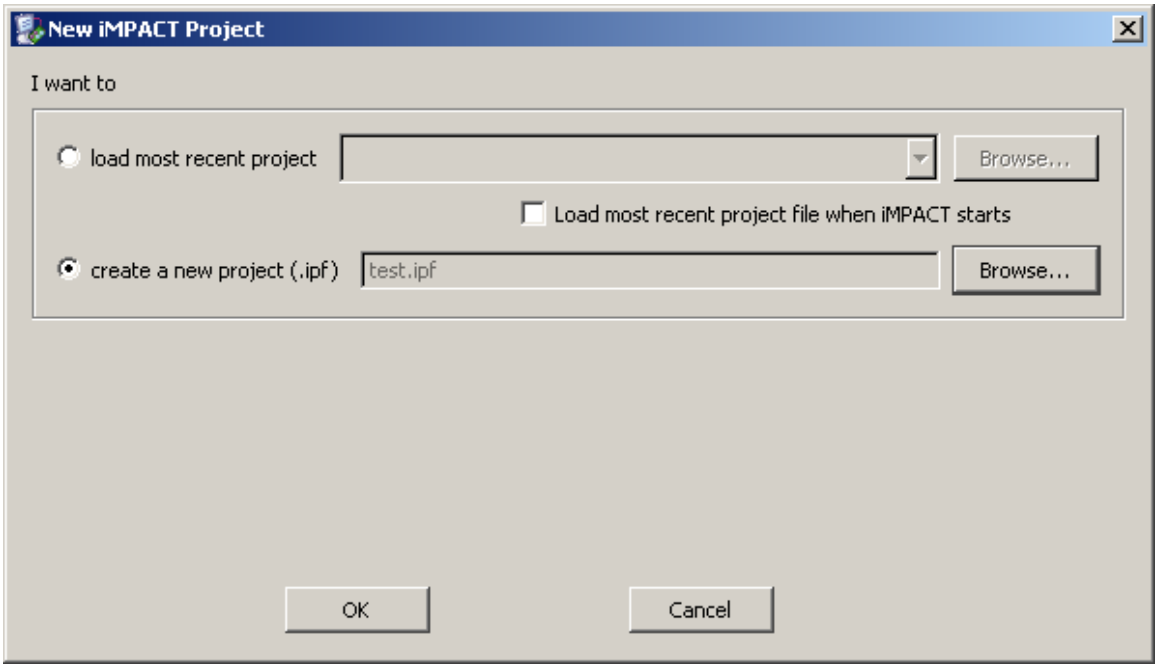

Figure 4 - New iMPACT Project Wizard

6. Select the option to **Configure devices using Boundary-Scan (JTAG)** then click **OK**.

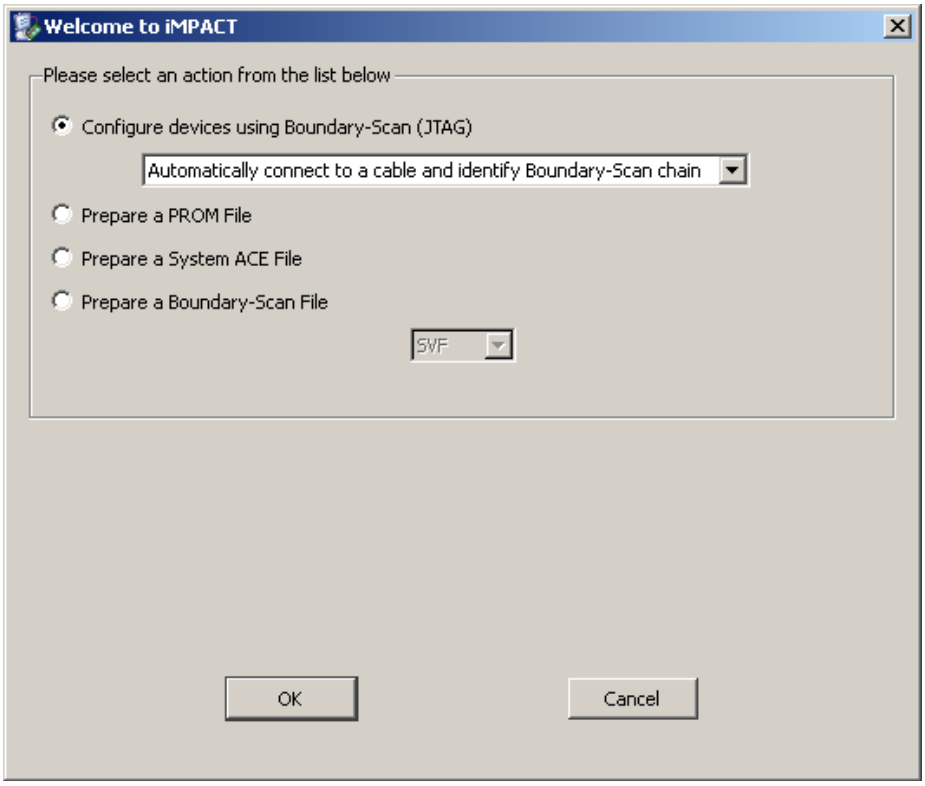

Figure 5 - Configure Devices

7. iMPACT will open and auto-detect the boundary scan chain.. If not, right-click in the Boundary Scan window and select Initialize Chain.

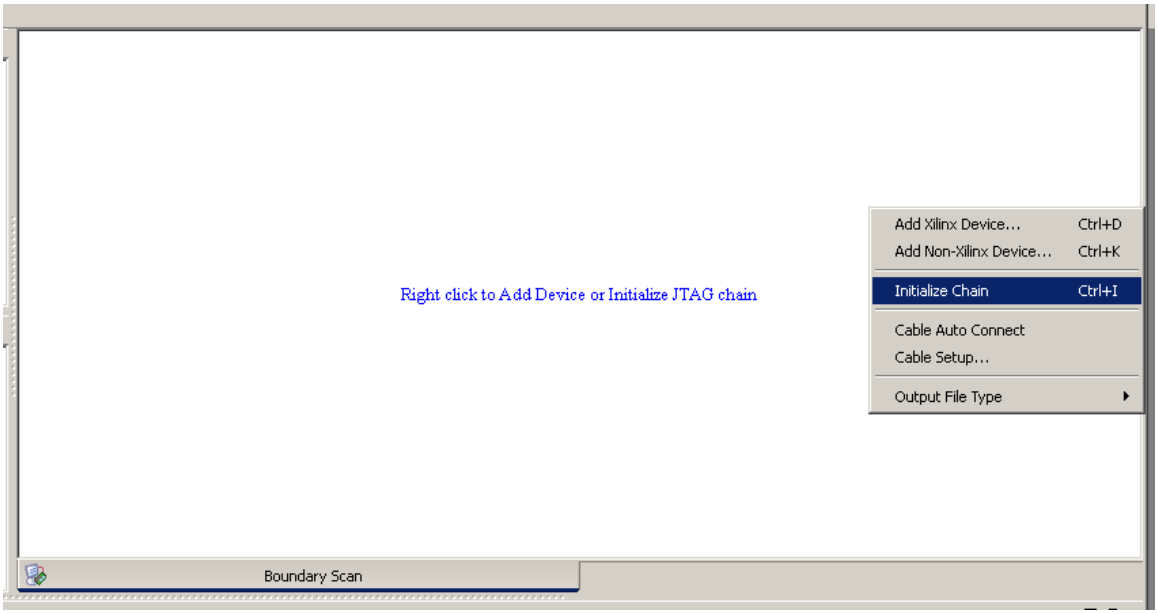

Figure 6 - Initialize Chain

8. Follow the pop-up dialog window to select a .BIT file by clicking **Yes**. Selecting a .BIT file will directly configure the FPGA. The FPGA is non-volatile however and thus a power-cycle or pressing the PROG pushbutton, SW4, will cause the FPGA to lose this configuration.

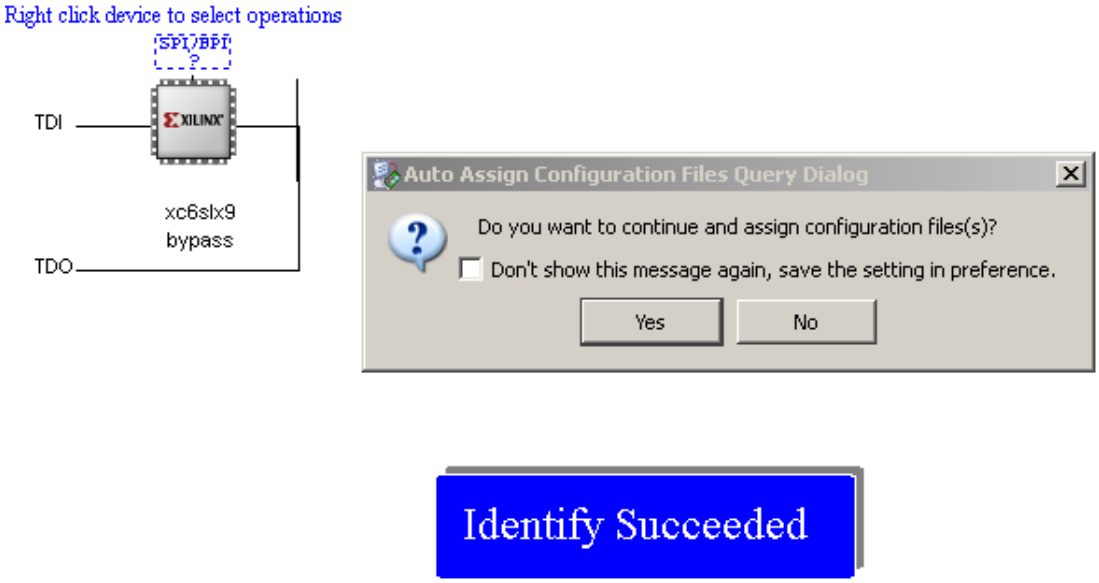

Figure 7 - JTAG Chain Identified

9. To program the attached SPI Flash, either continue with the Configuration File Assignment or right-click on the SPI/BPI link above the FPGA and select 'Add SPI/BPI Flash'. This will require a .MCS file which can be generated from a .BIT file in the iMPACT software. To create a .MCS file, see Appendix A or consult iMPACT help or the Xilinx Spartan-6 FPGA Configuration Guide.

   NOTE: programming an uncompressed LX9 bitstream to the Flash using the iMPACT GUI can take several minutes. The command-line mode detailed in Procedure 2 is much faster as it bypasses the JTAG protocol and programs the Flash directly.

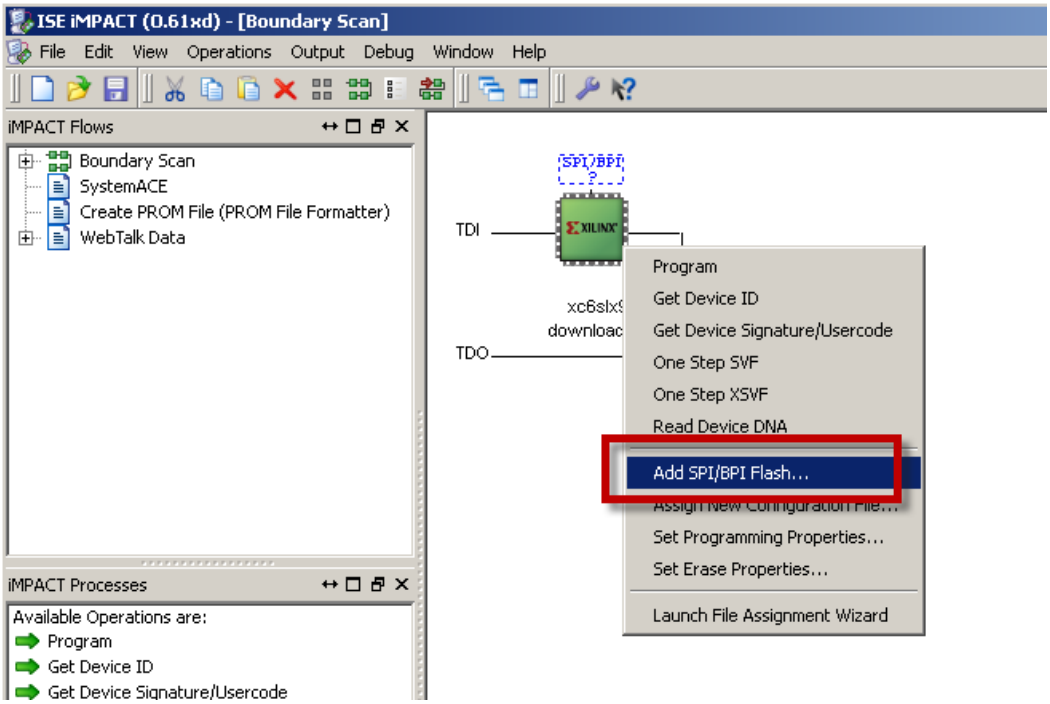

Figure 8 - Selecting SPI Flash

10. Select **SPI PROM**, **N25Q128** and change the **Data Width** to **4**. Setting the Data Width to four bits wide requires that the bitstream and MCS files were created to support this width. It is acceptable to use x1 and x2 data widths as well. See Appendix A for details on how to create bitstreams that support wider data widths.

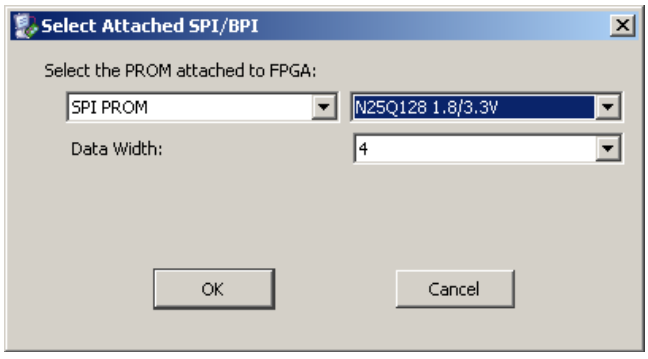

Figure 9 - Select N25Q128 PROM

11. The Flash above the FPGA will now look like an IC labeled 'FLASH'. Right-click on this and select **Program**:

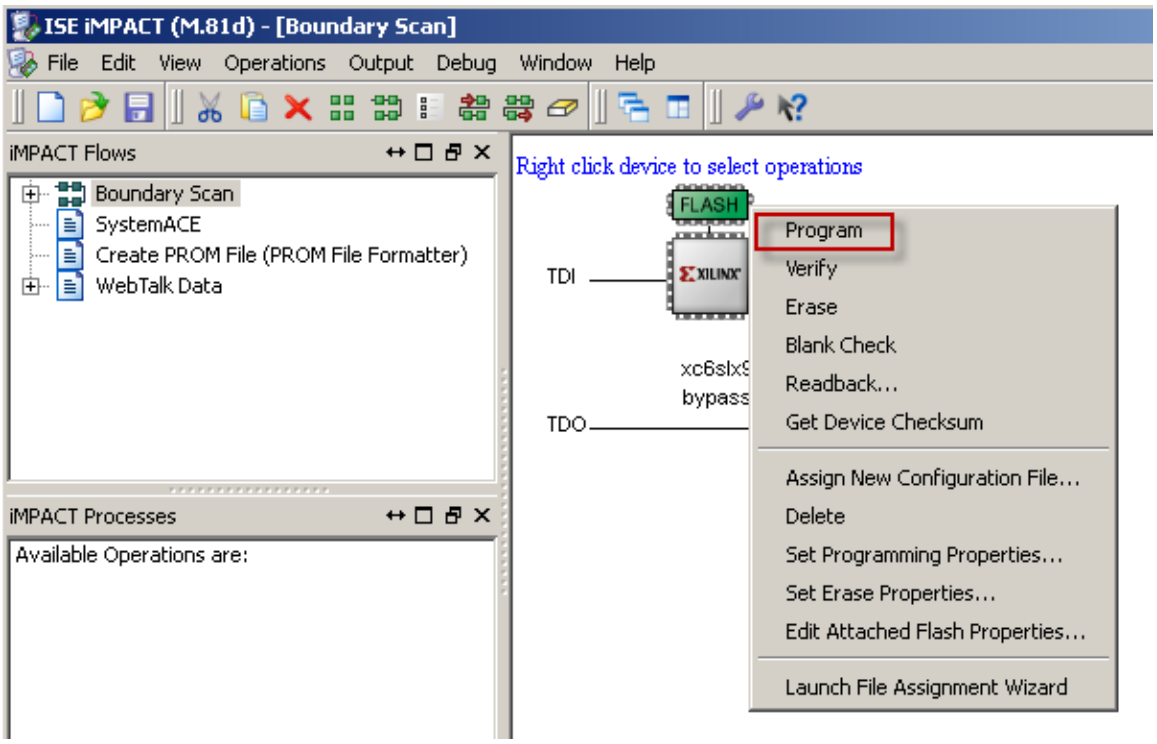

Figure 10 - Right-click on FLASH and select Program

12. Device Programming Properties will appear. Click **OK**.

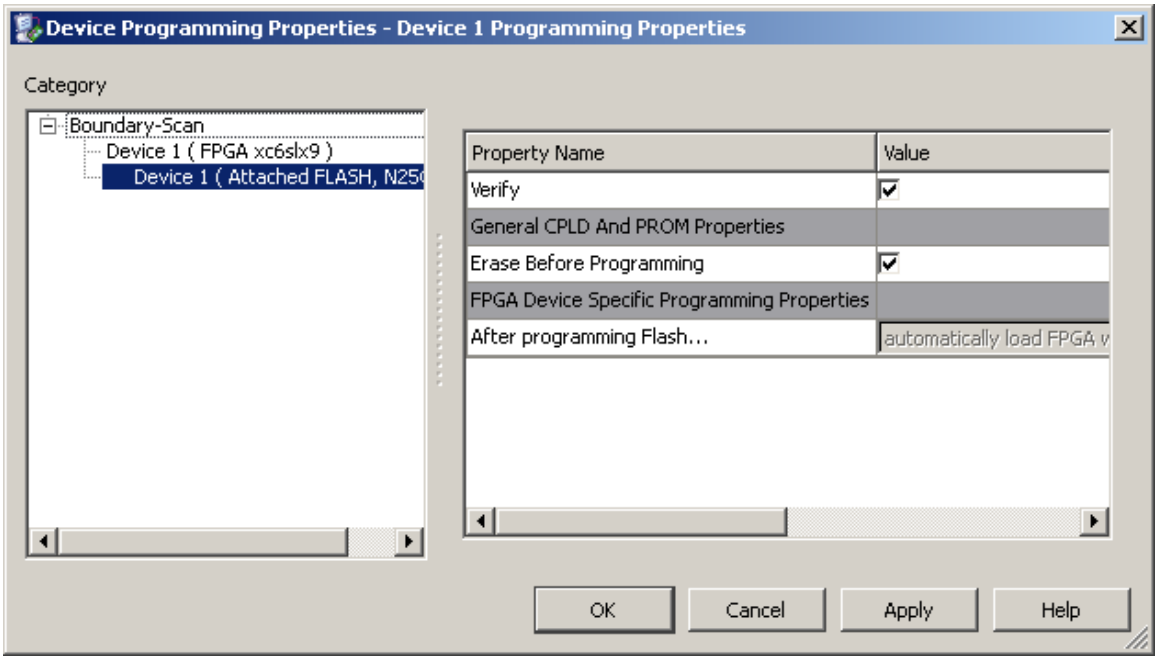

Figure 11 - Device Programming Properties

13. iMPACT will begin programming the Flash, depending on the size of the MCS file, this could take several minutes. Once completed, assuming no errors are encountered, the Flash is programmed and the FPGA will now have its configuration data stored in non-volatile memory. The FPGA will automatically reconfigure with this new image upon pressing the PROG_B pushbutton, SW4, or power cycling the board.

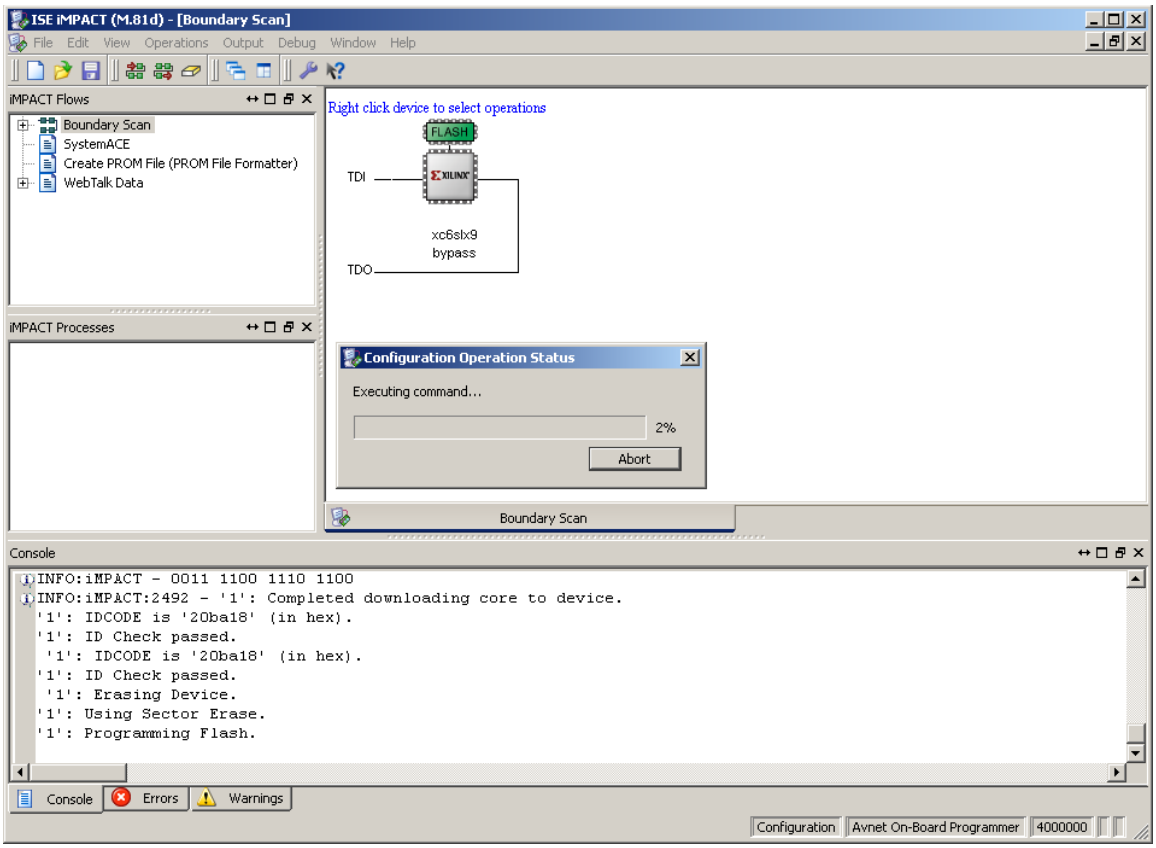

Figure 12 - Device Programming

Note: See Appendix B for improved programming performance.

This concludes this section. Programming of the serial flash and configuration of the FPGA are completed.

Procedure 2: Programming via on-board USB-JTAG Circuitry and Digilent's Serial Flash Utility

The Digilent SFUTIL.exe utility provides a fast programming interface to the on-board serial flash. The utility must be downloaded from Digilent's website. Once downloaded, this utility can be run from Windows command line or a batch file. Additionally this utility is customizable to perform a number of functions. To use this utility, follow the below instructions:

1. Open a Web Browser and navigate to Digilent's website:

http://www.digilentinc.com/

2. Click on **Software** link under Products:

Figure 13 - Select Software on Digilent's Webpage

3. Scroll down to Serial Flash Utility and click **Download!**

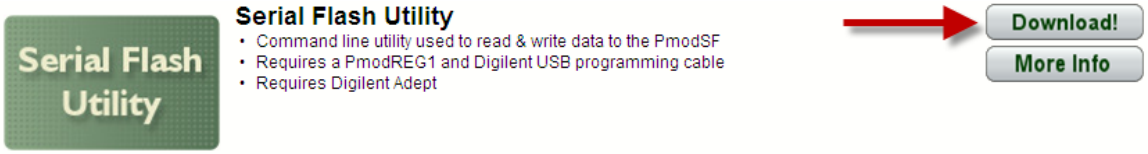

Figure 14 - Download Serial Flash Utility

4. **Save** the attached zip file and extract it to a known place on your PC.

5. In this same directory **create a batch file**. Open a text editor, such as Notepad, and copy the following commands:

```
cls
echo off
cls
ECHO    *** Spartan-6 LX9 MicroBoard Factory Test Flash Loader with Erase ***
ECHO      ------------------------------------------------------------------------
ECHO
rem
rem This batch file will perform a sector erase of the specified length and
rem then write the specified file to the flash starting at address 0..
sfutil -d obp -cr -m N25Q128 -e -fi -w PROGRAMMING_IMAGE.mcs -t
ECHO
ECHO    Press any key to exit...
```

6. The 'sfutil' executable is called with options to program this S6LX9 MicroBoard's on-board serial flash. This serial flash utility accepts MCS format files. These files can be created with ISE iMPACT software from a FPGA's bitstream file. **The placeholder, 'PROGRAMMING_IMAGE.mcs', must be replaced with your MCS file.**

7. **Save this batch file**, for example S6_LX9_EraseProgram.bat, and close the editor.

8. **Connect** the S6LX9 MicroBoard to the host PC as shown in Figure 15.

9. **Double-click the batch file** created above to execute it. Programming will ensue. **Note:** Programming times will vary based on FPGA Utilization as well as USB port speed.

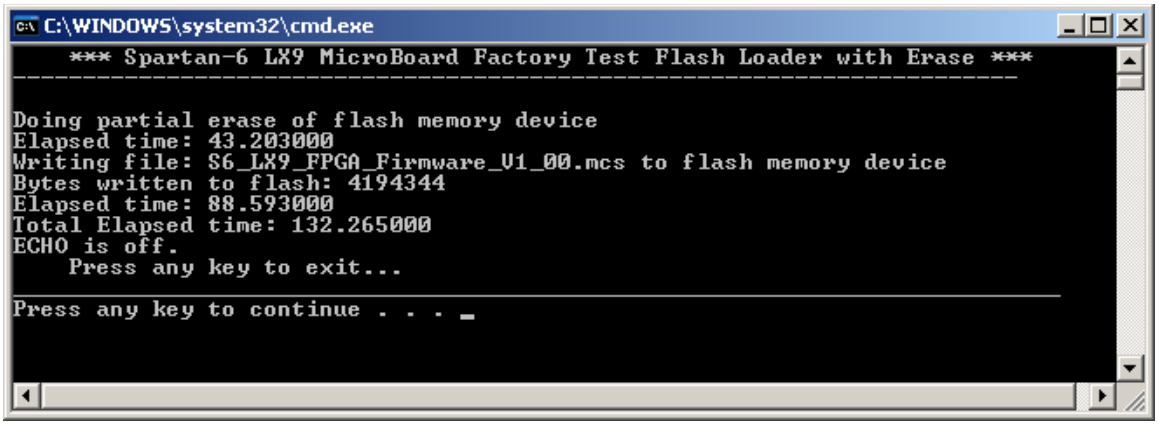

Figure 15 - SFUTIL Programming

Note: This programming method only works with the on-board USB JTAG circuitry as it has direct connections to the flash.

Note: See Appendix B for improved programming performance.

This concludes this section, to learn more about SFUTIL, type 'sfutil ?' at a DOS prompt or visit Digilent's Website.

Configuration and Programming using Xilinx iMPACT with an External Programming Cable

Using a Xilinx USB JTAG Platform Cable or Digilent JTAG HS1 Programming Cable and Xilinx's iMPACT programming tool, the FPGA can be configured directly, as well as program the attached flash device. The iMPACT programming tool is a subset of the Xilinx ISE WebPACK or ISE Design Suites which can be downloaded from here:

http://www.xilinx.com/tools/designtools.htm

Procedure 3: iMPACT using an External Programming Cable

To configure the Spartan-6 LX9 FPGA and program the attached serial flash using this method, follow the steps outlined below:

14. Power must be applied to the MicroBoard. This is done by connecting a PC to the board via a MicroUSB cable. Plug the cable into the Type-A USB connector, J3, as shown below.

15. Connect the external programming cable to the host PC and S6LX9 MicroBoard's JTAG port, J6. When completed, the S6LX9 MicroBoard should be connected to the host PC as shown in the figure below:

Figure 16 - Configuration Setup with Xilinx Platform Cable USB

16. Launch iMPACT 13.2 or 13.1 by selecting **Start → Programs → Xilinx ISE Design Suite 13.1 → ISE Design Tools → Tools → iMPACT**.

17. Select **No** when asked to automatically load the last project and when asked to create and save a project.

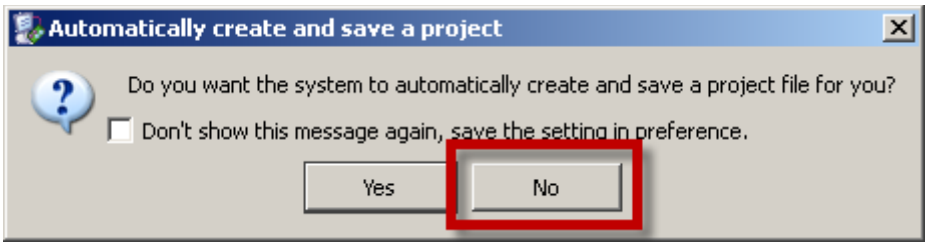

Figure 17 - Automatic iMPACT Project Wizard

18. Select **create a new project (.ipf)** at the New iMPACT Project Wizard and click **OK**.

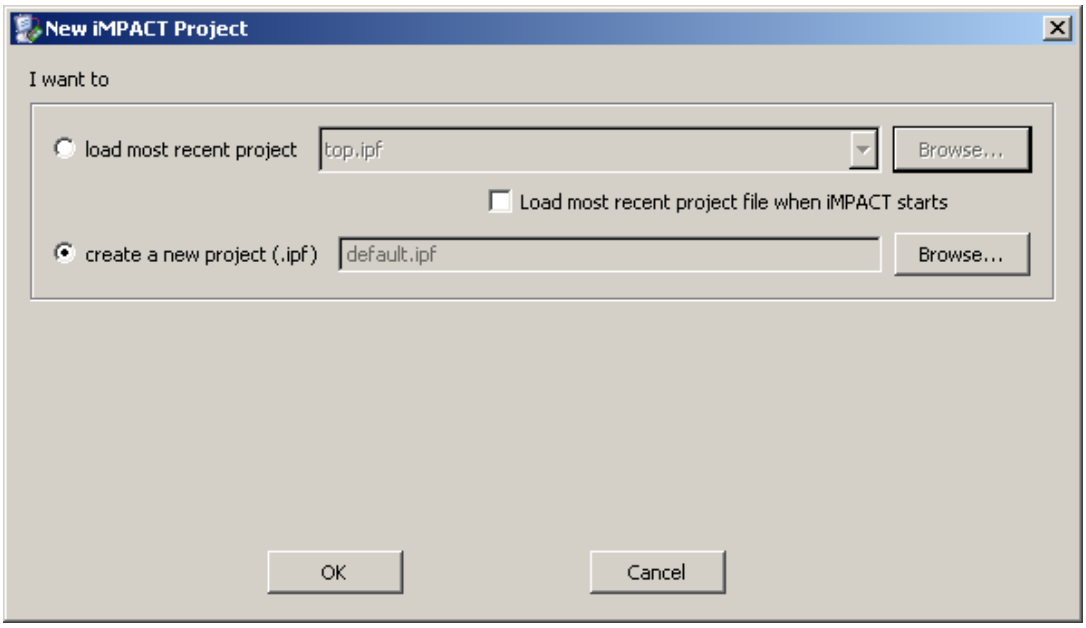

Figure 18 - New iMPACT Project Wizard

19. Select the option to **Configure devices using Boundary-Scan (JTAG)** then click **OK**.

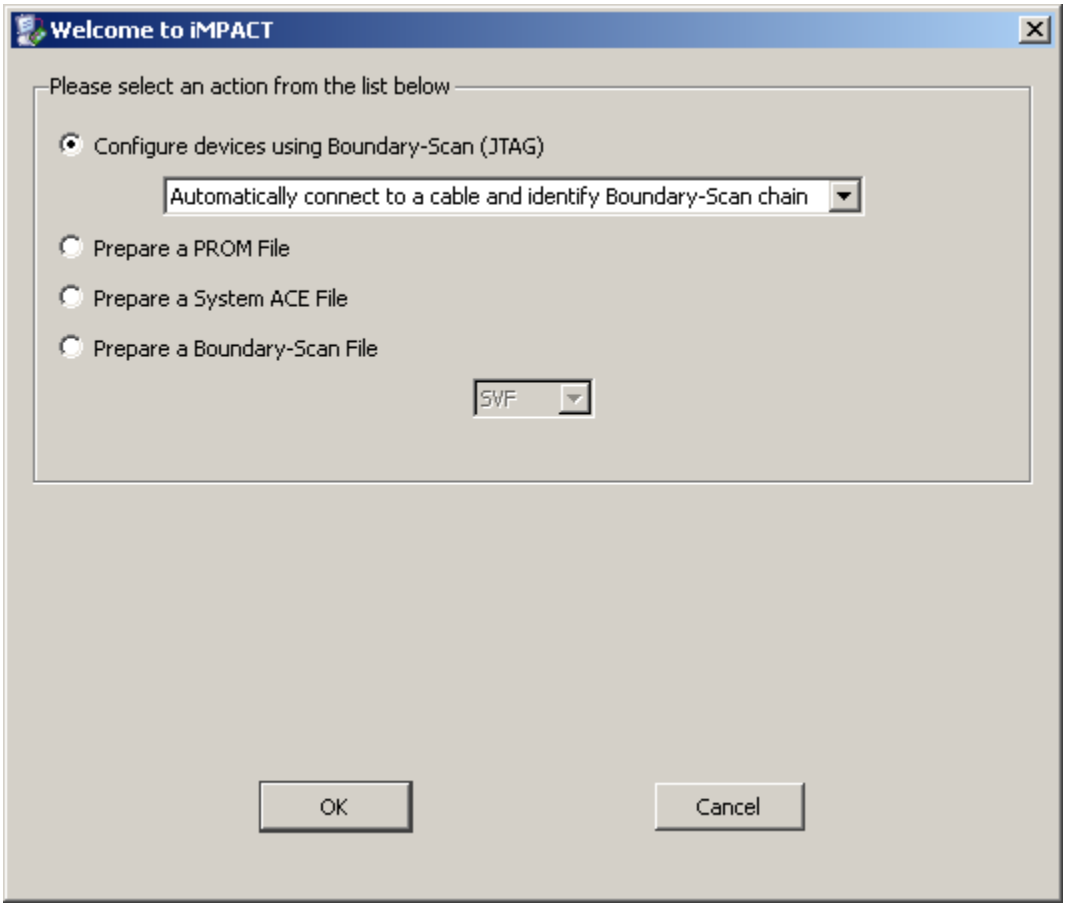

Figure 19 - Configure Devices

20. Follow the pop-up dialog window to select a .BIT file by clicking **Yes**. Selecting a .BIT file will directly configure the FPGA. The FPGA is non-volatile however and thus a power cycle or pressing the PROG pushbutton, SW4, will cause the FPGA to lose this configuration.

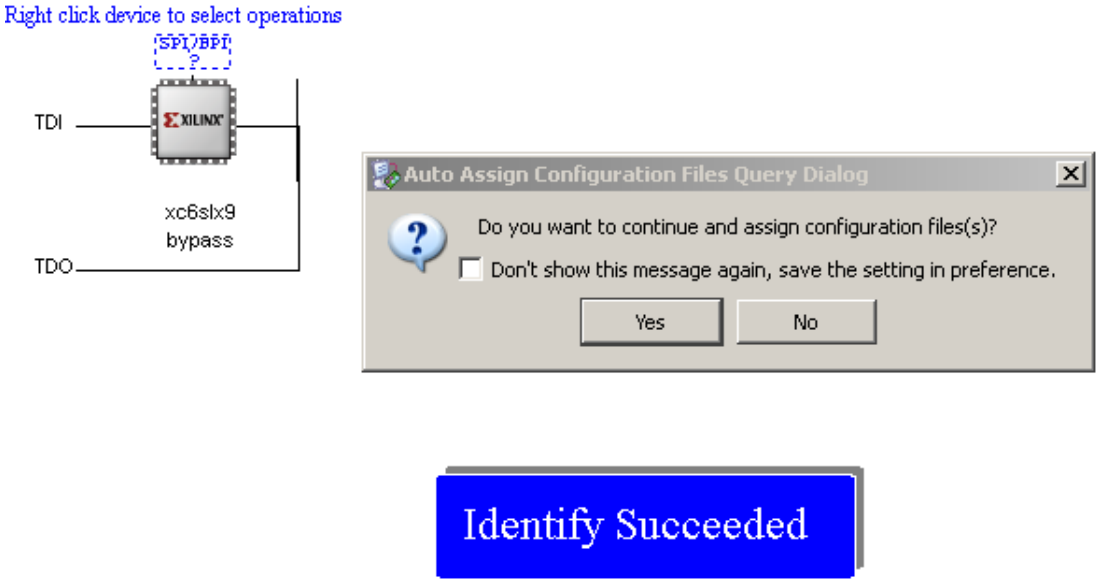

Figure 20 - JTAG Chain Identified

21. The next pop-up dialog window asks if you want to attach a PROM device. It is OK to say YES and continue with the Configuration File Assignment Wizard, however for this example, click **No**.

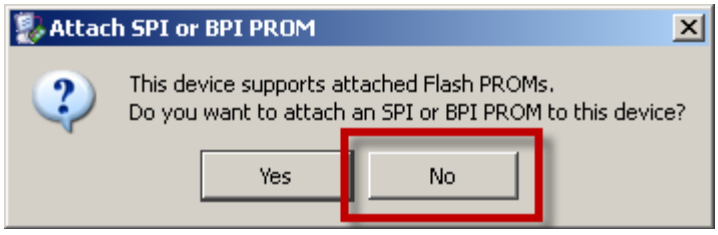

Figure 21 - Attach PROM

22. Finally, Click **OK** to accept default programming properties.

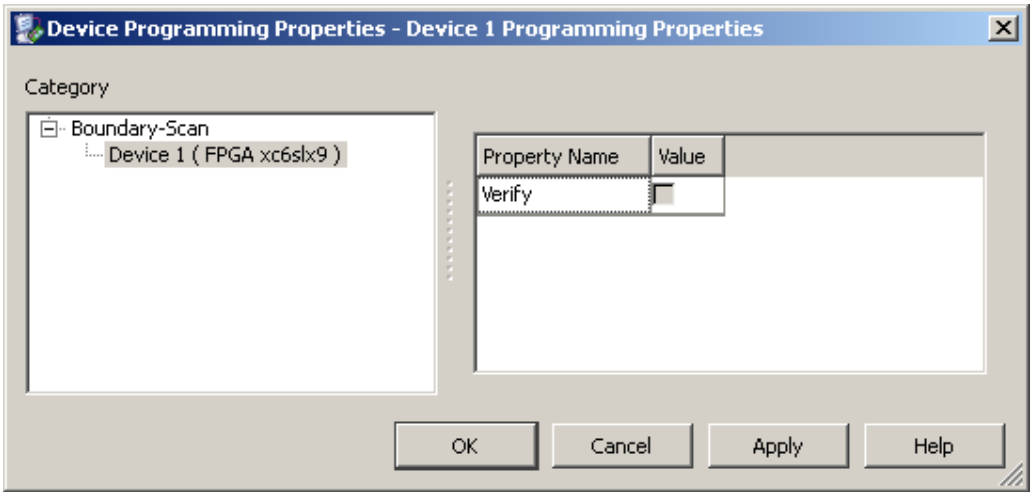

Figure 22 - Accept Default Programming Properties

23. To program the attached SPI Flash, right-click on the SPI FPGA and select '**Add SPI/BPI Flash**'. This will require a .MCS file which can be generated from a .BIT file in the iMPACT software.

    NOTE: programming the Flash using the iMPACT GUI can take several minutes using the Xilinx Platform Cable USB. The Digilent JTAG HS1 Programming Cable several times faster as it has an improved programming interface. Alternatively, Procedure 2, may provide the fastest Flash programming method.

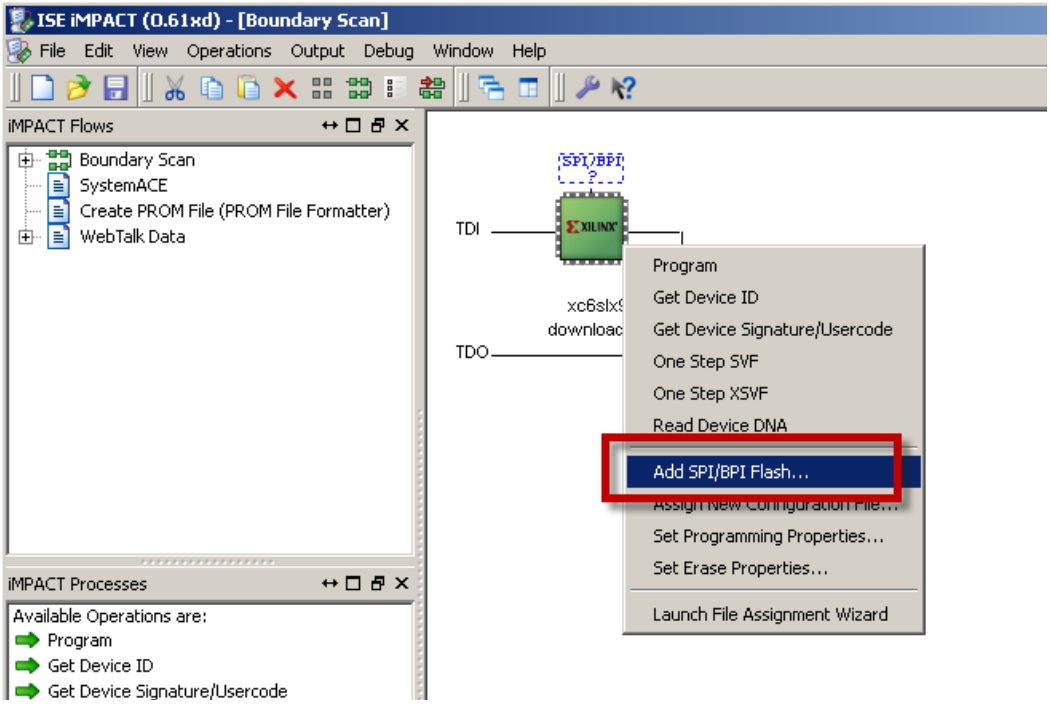

Figure 23 - Selecting SPI Flash

24. When asked, select the desired .MCS file to program the serial flash.

25. Select **SPI PROM**, **N25Q128** and change the **Data Width** to **4**. Setting the Data Width to four bits wide requires that the bitstream and MCS files were created to support this width. It is acceptable to use x1 and x2 data widths as well. See Appendix A for details on how to create bitstreams that support wider data widths. Note: ISE 12.x may not show the voltages (1.8V/3.3V) after N25Q128.

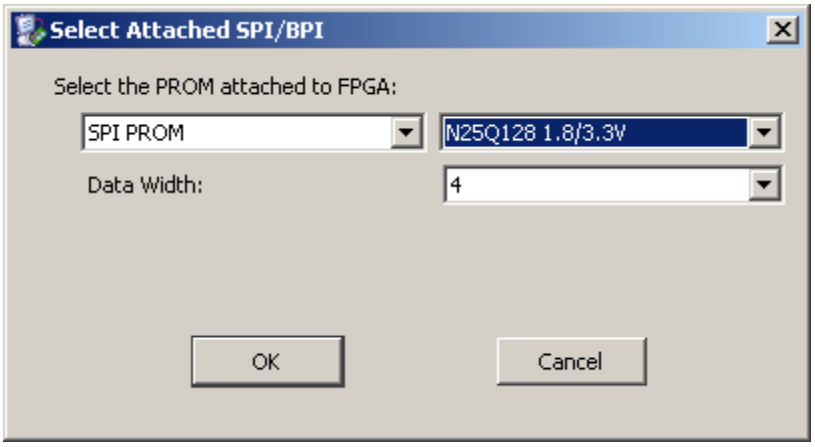

Figure 24 - Select N25Q128 PROM and Data Width

26. The Flash above the FPGA will now look like an IC labeled 'FLASH'. Right-click on this and select **Program**:

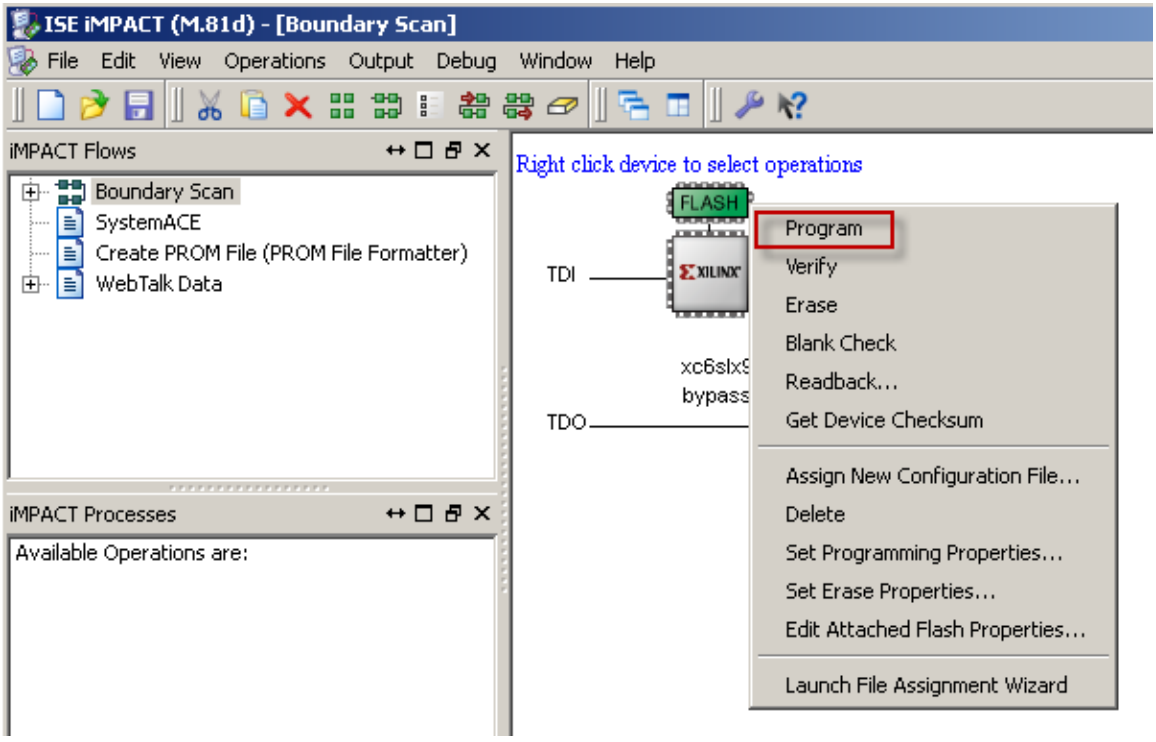

Figure 25 - Program Flash

27. Device Programming Properties will appear. Click **OK**. Note, properties are shown for the Attached Flash in the window below. Leave all settings as default.

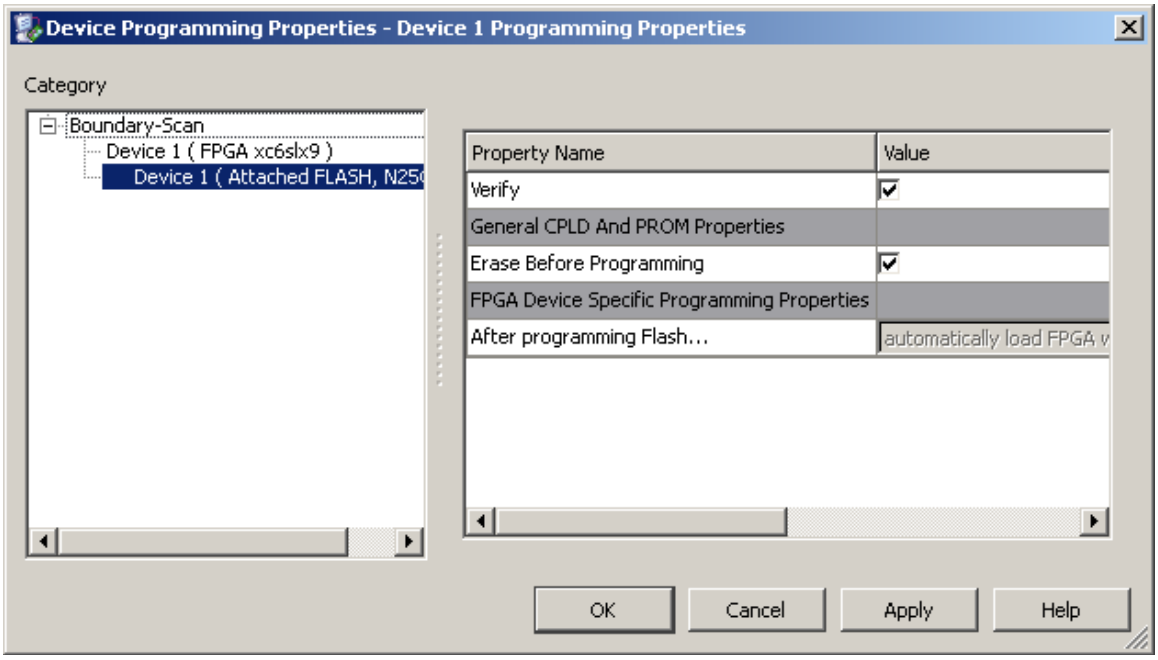

Figure 26 - Device Programming Properties

28. iMPACT will begin programming the Flash, depending on the size of the MCS file, this could take several minutes. Once completed, assuming no errors are encountered, the Flash is programmed and FPGA will now have its configuration data stored in non-volatile memory. The FPGA will automatically reconfigure with this new image upon pressing the PROG_B pushbutton, SW4, or power cycling the board.

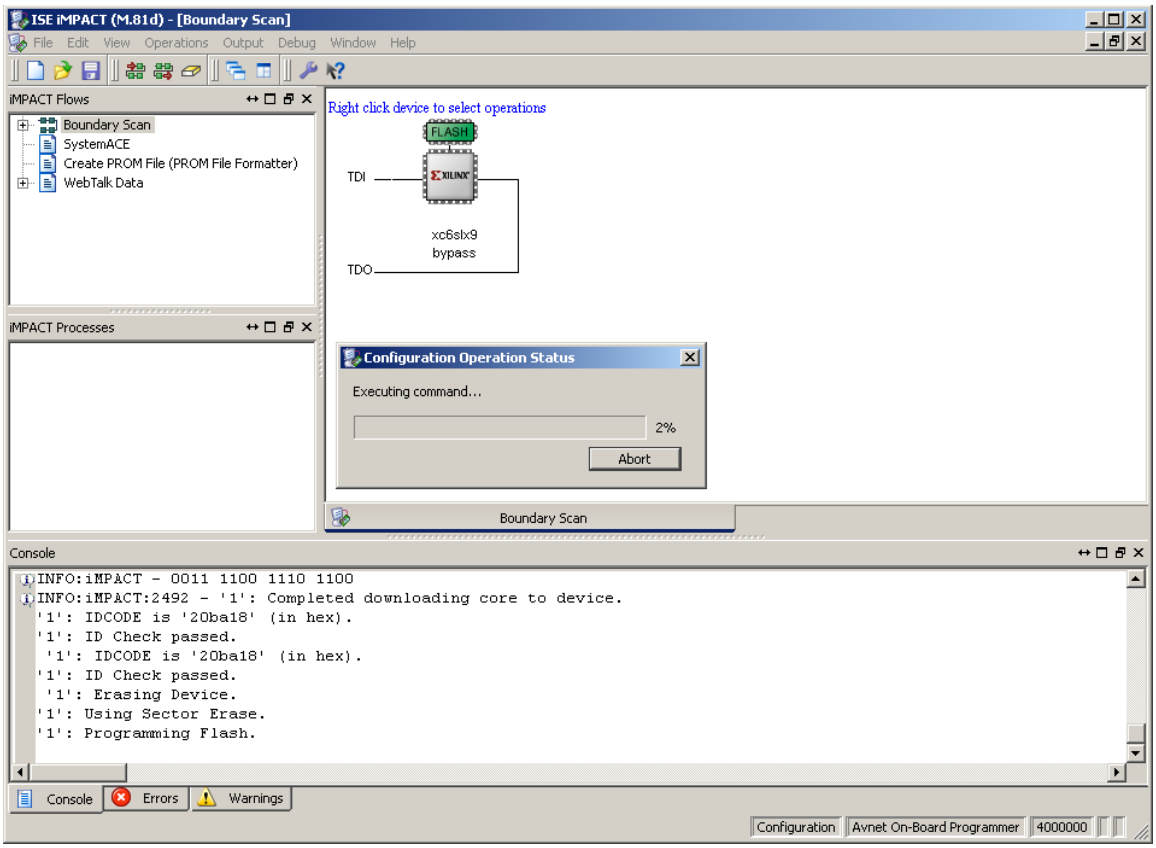

Figure 27 - Device Programming

29. If no errors are encountered, programming will succeed.

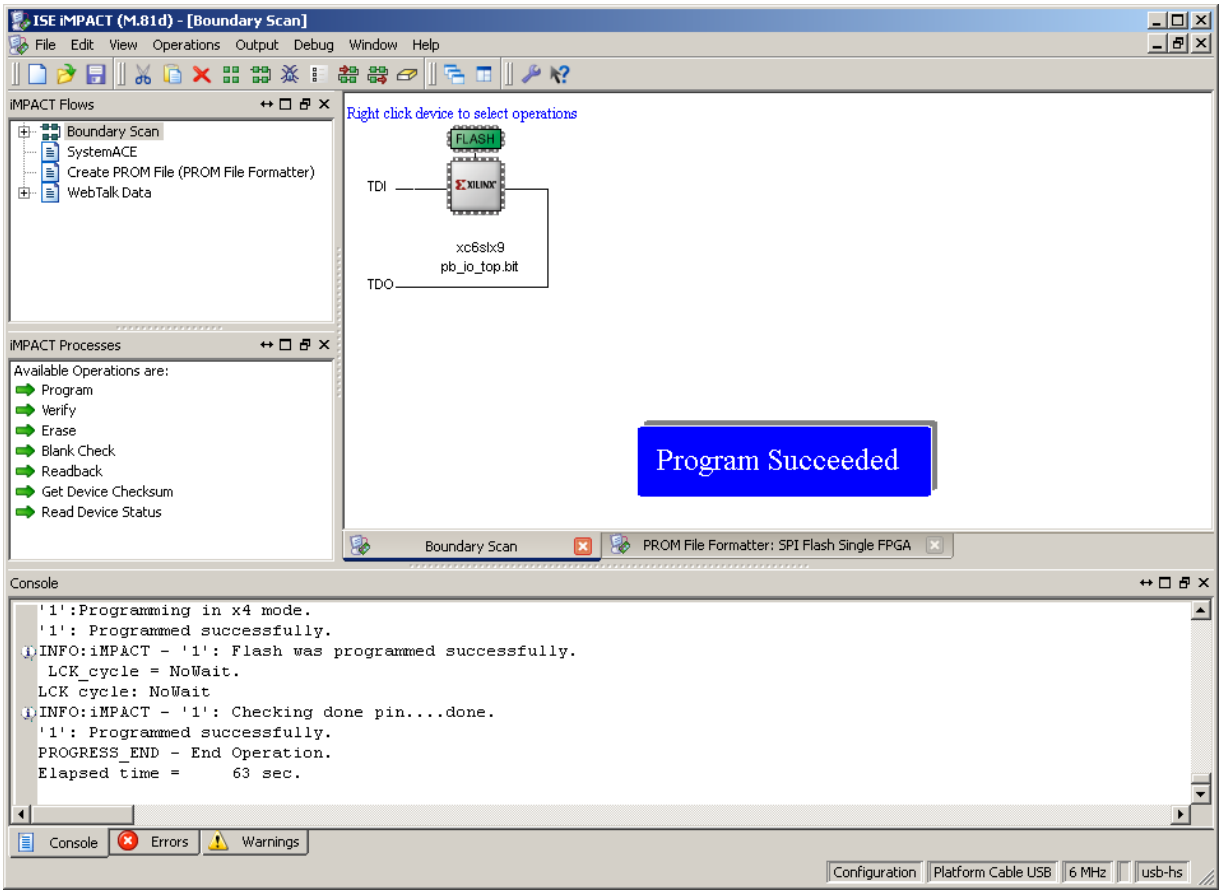

Figure 28 - Programming Succeeded Window

30. This concludes this section. Programming of the serial flash and configuration of the FPGA are completed. For more on configuration using this method, please read the Spartan-6 FPGA Configuration User Guide:

    http://www.xilinx.com/support/documentation/user_guides/ug380.pdf

Conclusion

That completes this guide. As shown in the three procedures above, there are several ways to configure the FPGA and program the attached serial flash on the S6LX9 MicroBoard. For more information please visit the Avnet Design Resource Center or visit Xilinx's Support Website. Additionally, the Xilinx Spartan-6 FPGA Configuration User Guide provides complete documentation for all configuration methods.

Appendix A: Creating a SPI x4 Bitstream and MCS file

This section will show how to create a bitstream and MCS file that supports 4-bit wide SPI configuration. This must be initiated during bitstream creation. The purpose of this is to increase the configuration rate of the FPGA. The steps below guide you through this process.

1. In ISE Project Navigator, assuming the design has been fully implemented without errors, right-click on Generate Programming File and select **Process Properties**.

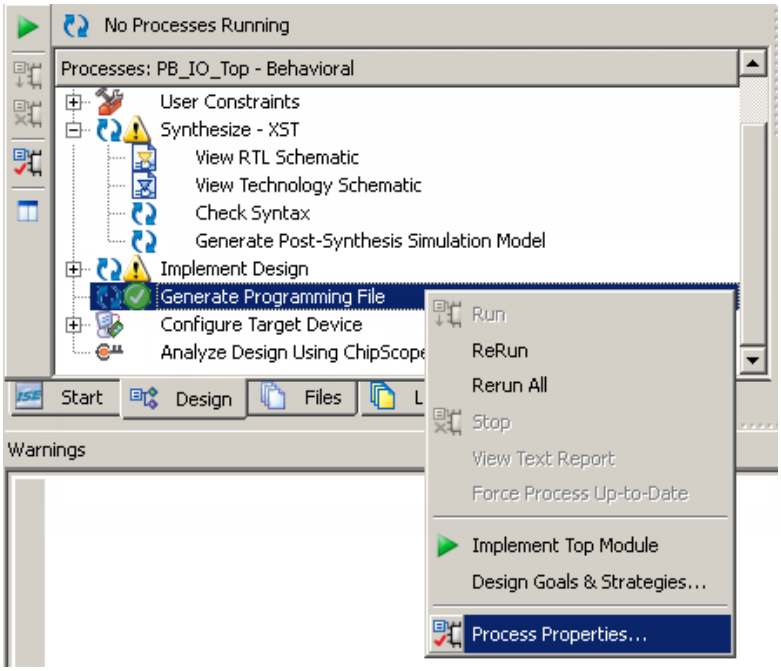

Figure 29 - Select Process Properties under Generate Programming File

2. In the Process Properties – Configuration Options window, select **Configuration Options** and set SPI Configuration Bus Width to **4**. Then Click **OK**. (Note: you must have the Property Display Level set to **Advanced** to see these options.) For increased performance, the configuration rate can be increased. Moreover, the external Master CCLK (40MHz) can be used for maximum performance. Be aware this only applies to the FPGA loading the bitstream from the serial flash.

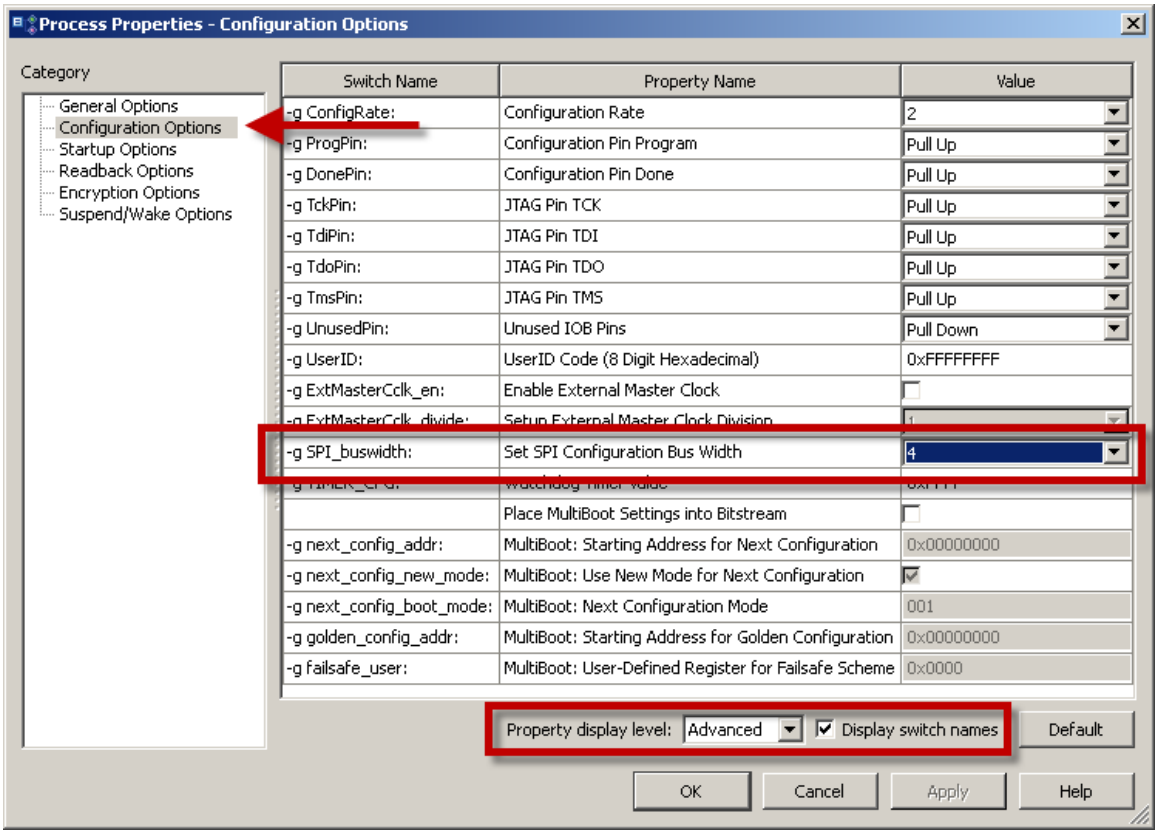

Figure 30 - Configuration Options

3. The dialog box should close and return to ISE Project Navigator. Right-click on **Generate Programming File** and select **Run**.

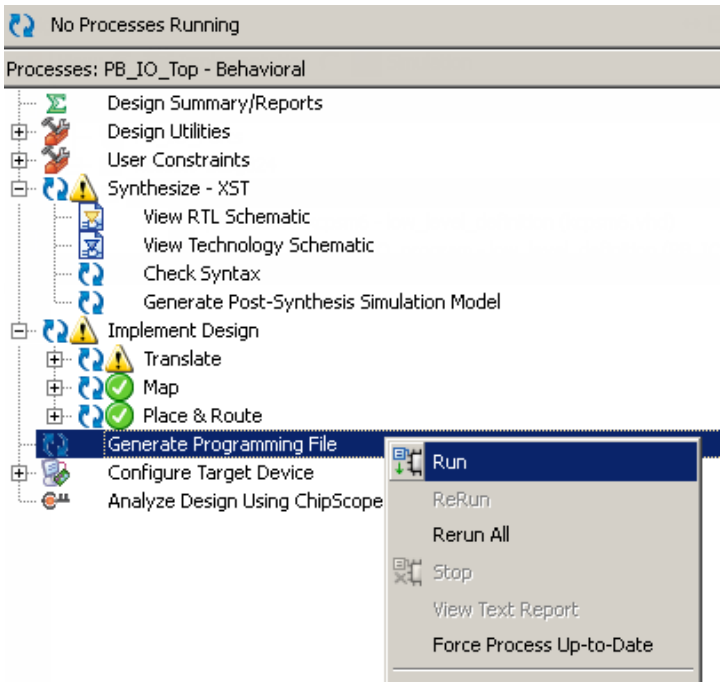

Figure 31 - Generate Programming File

4. Watch the Console window to validate the programming file is created.

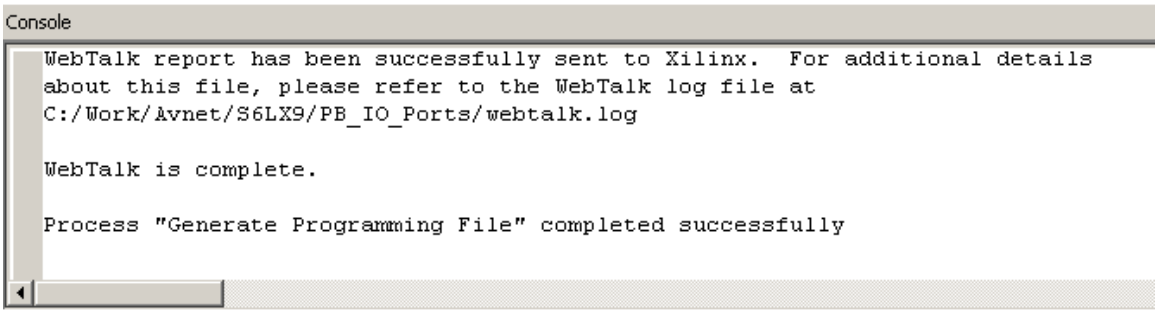

Figure 32 - Bitstream Generation Successful

5. This process only creates a bitstream, .BIT, file used for configuring the FPGA. A .MCS file must be created for programming the attached serial flash. Expand **Configure Target Device** and select **Generate Target PROM/ACE File**. A warning window may pop up, click OK.

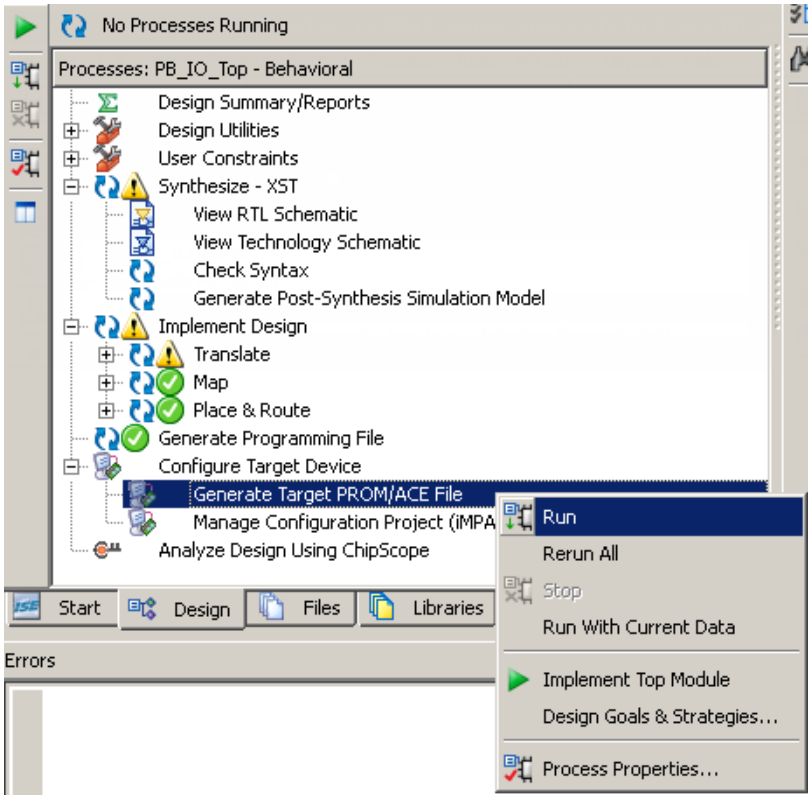

Figure 33 - Generate PROM File

6. Double-click on **Create PROM File (PROM File Formatter).**

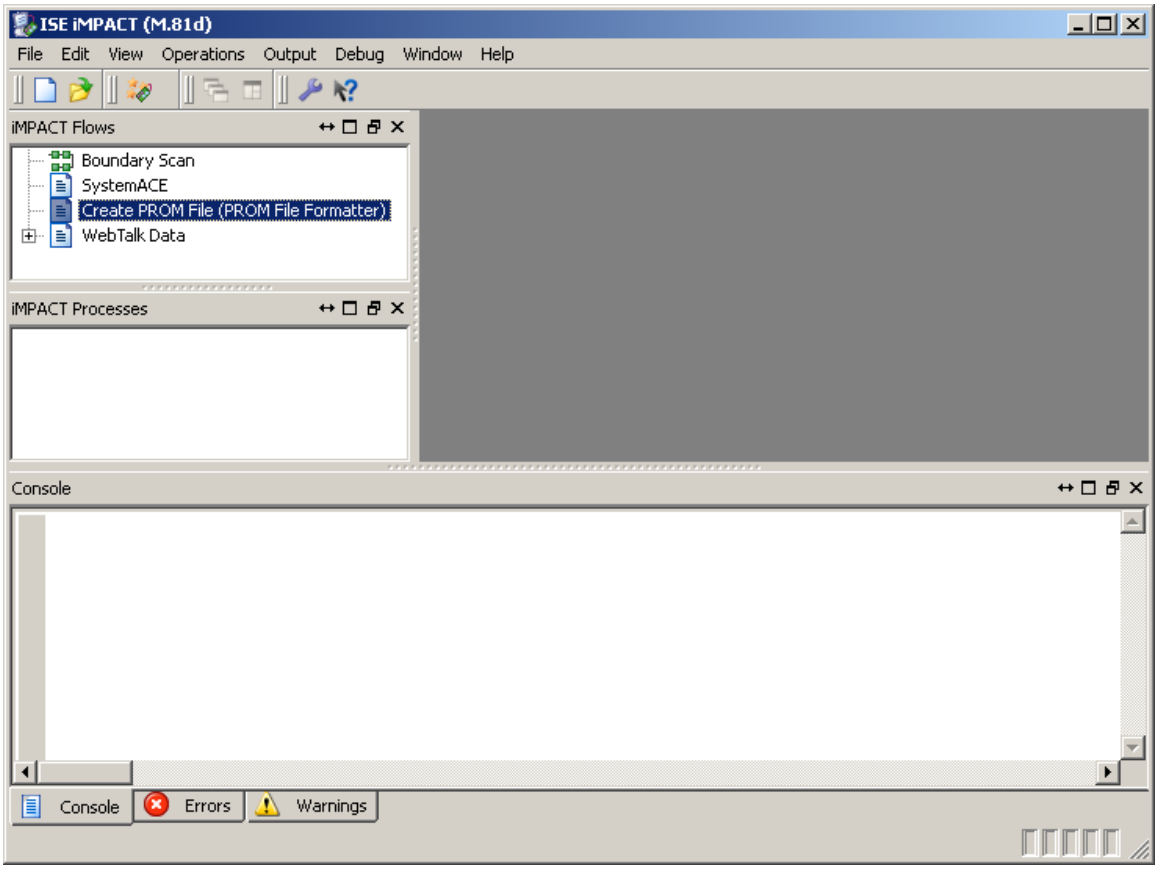

Figure 34 - Select Create PROM File

7. Step through the File Formatter Wizard:
    1. Under SPI Flash, select **Configure Single FPGA**
    2. Click left most green arrow box to continue.
    3. In the **Storage Device (bits)** pull-down, select **128M**.
    4. Click **Add Storage Device** button.
    5. Click right most green arrow box to continue.
    6. Enter Output File Name and Location
    7. Click **OK**

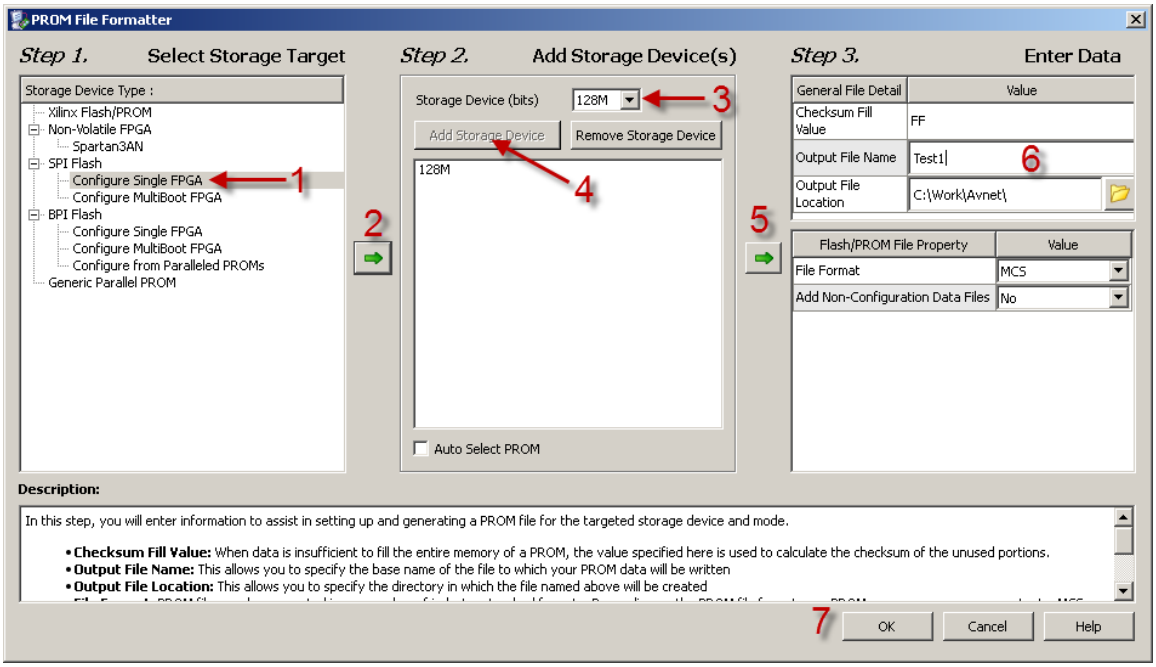

Figure 35 - PROM File Formatter

8. Add Device window will appear, click **OK**. Select the .BIT file created in step 3. This .BIT file will be located in your project directory, unless specified otherwise in the ISE project.

9. When asked to add another device file, click **No**. A pop-up window will appear noting device entry is complete, click **OK**.

10. When returned to the iMPACT window, double-click **Generate File**. A pop-up window will appear stating Generate Succeeded.

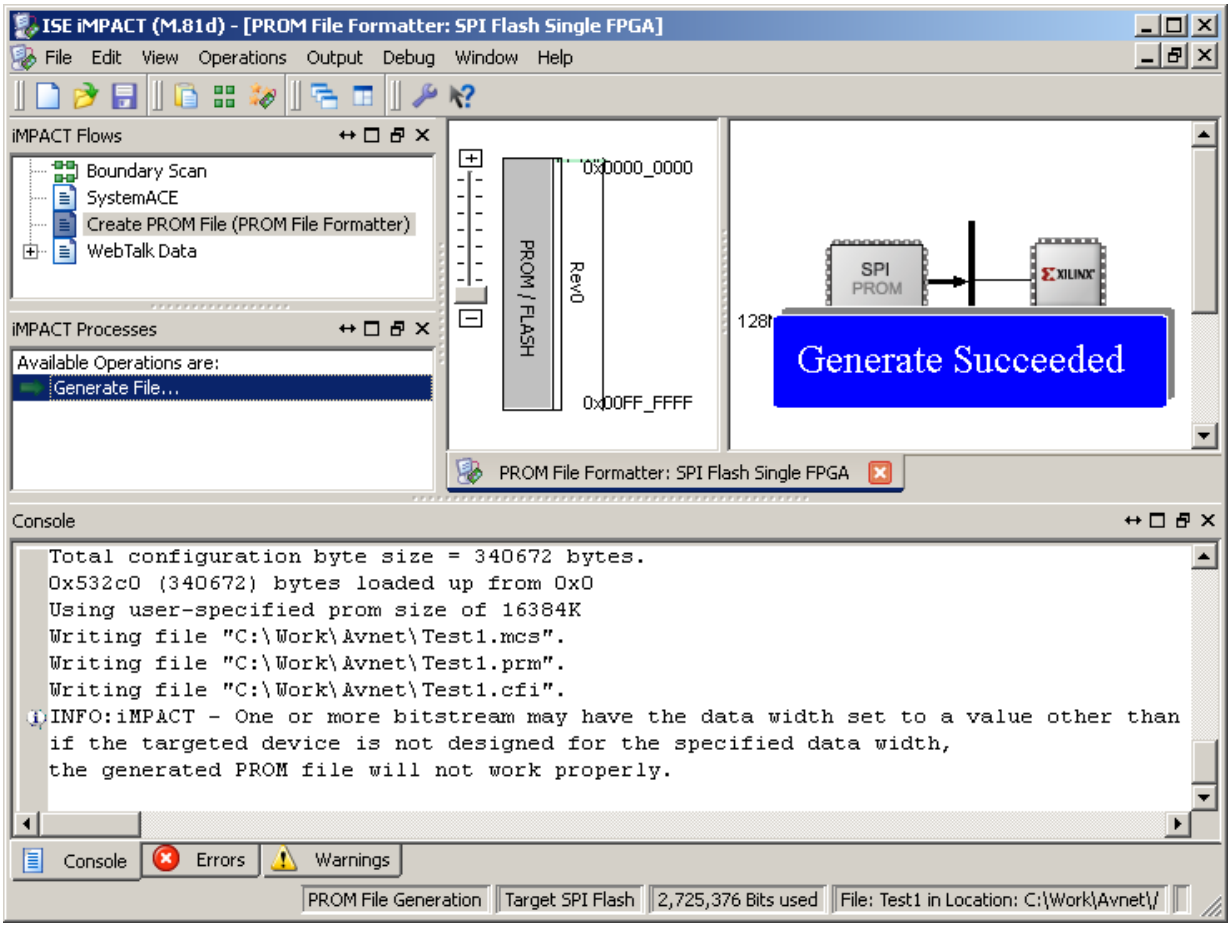

Figure 36 - Successful PROM File Generation

11. This concludes generating a x4 bitstream and MCS programming file.

12. When exiting you will be asked to save your iMPACT project file, you may do so to prevent going through all of these steps again for future builds.

Appendix B: Increasing USB-JTAG Circuitry Performance

Adding a Hi-Speed USB hub to increase USB scheduling rates equals faster downloads

The Spartan-6 LX9 MicroBoard uses an Atmel AT90USB162 full-speed USB microcontroller that is programmed to translate USB commands to JTAG commands. Most computers recognize the S6LX9 MicroBoard as a full-speed device and thus default it to a full-speed USB root hub. This can be seen in Windows Device Manager. When detected as a full-speed device, the Windows host controller enumerates the device into a full-speed scheduler. The full-speed scheduler uses a frame period of one millisecond. Hi-speed devices divide a frame into 8 micro-frames of 125 microseconds.

A trick can be applied to make the Windows PC put the S6LX9 MicroBoard into a hi-speed scheduling mode. When a hi-speed hub is plugged into a USB port, the host controller driver schedules transactions to it using the hi-speed scheduling rules. Thus when data packets are sent to the S6LX9 MicroBoard, they are done on a faster schedule. This results in faster download times. For example, the factory test code that ships with board is a large flash image and when directly plugged into a PC's USB port, download times can take nearly 7 minutes*. However, simply inserting a hi-speed USB hub between the PC and the S6LX9 MicroBoard will reduce this time down to nearly two minutes!

This was tested on a number of hi-speed USB hubs and all had the same performance improvements.

*Procedure 2 was used for this programming test.

Digilent JTAG HS1 Programming Cable

Availability -Americas only

The JTAG-HS1 programming cable is a high-speed programming solution for Xilinx FPGAs. It is compatible with all Xilinx tools, including iMPACT, Chipscope, and EDK. The HS1 attaches to target boards using Digilent's 6-pin, 100-mil spaced programming header, or Xilinx's 2x7, 2mm connector (using the included adaptor).

The JTAG-HS1 is powered from a PC's USB port. The HS1 can be seamlessly driven from Xilinx's iMPACT software or from Digilent's Adept software. It will be recognized as a Digilent programming cable when connected to a PC, whether or not it is attached to the target board. A separate Vdd pin is provided on the HS1 to supply JTAG signal buffers. These high speed, 24mA, three-state buffers allow target boards to use JTAG signal voltages from 1.8V to 5V, with bus speeds of up to 30MBit/sec. The HS1's Vdd pin must be tied to the same voltage supply that drives the JTAG port on the FPGA.

JTAG signals are held in high-impedance except when actively driven during programming, so the JTAG bus can be shared with other devices. The HS1 uses a standard Type-A to Micro-USB cable (included with the HS1) that attaches to the end of the module opposite the system board connector. The HS1 is small and light, allowing it to be held firmly in place by the system board connector.

Note for use with Adept: The JTAG-HS1 requires Adept System 2.8.1 or newer for use in Windows, and Adept Runtime 2.8.2 or newer for use in Linux.

Figure 37 - Digilent JTAG HS1 Programmming Cable

Getting Help and Support

Evaluation Kit home page with Documentation and Reference Designs

http://em.avnet.com/s6microboard

Avnet Spartan-6 LX9 MicroBoard forum:

http://community.em.avnet.com/t5/Spartan-6-LX9-MicroBoard/bd-p/Spartan-6LX9MicroBoard

Xilinx Spartan-6 FPGA Configuration User Guide:

http://www.xilinx.com/support/documentation/user_guides/ug380.pdf

For Xilinx technical support, you may contact your local Avnet/Silica FAE or Xilinx Online Technical Support at www.support.xilinx.com. On this site you will also find the following resources for assistance:

- Software, IP, and Documentation Updates
- Access to Technical Support Web Tools
- Searchable Answer Database with Over 4,000 Solutions
- User Forums
- Training - Select instructor-led classes and recorded e-learning options

Contact Avnet Support for any questions regarding the Spartan-6 LX9 MicroBoard reference designs, kit hardware, or if you are interested in designing any of the kit devices into your next design.

- http://www.em.avnet.com/techsupport

You can also contact your local Avnet/Silica FAE.