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# FPGA Development Platform Hardware Description

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**Rev. 1.0**

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# Revision History

| Rev. | Date | Author | Description |
|---|---|---|---|
| 1.0 | 11/16/08 | Sfielding | Created |
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| | | | |
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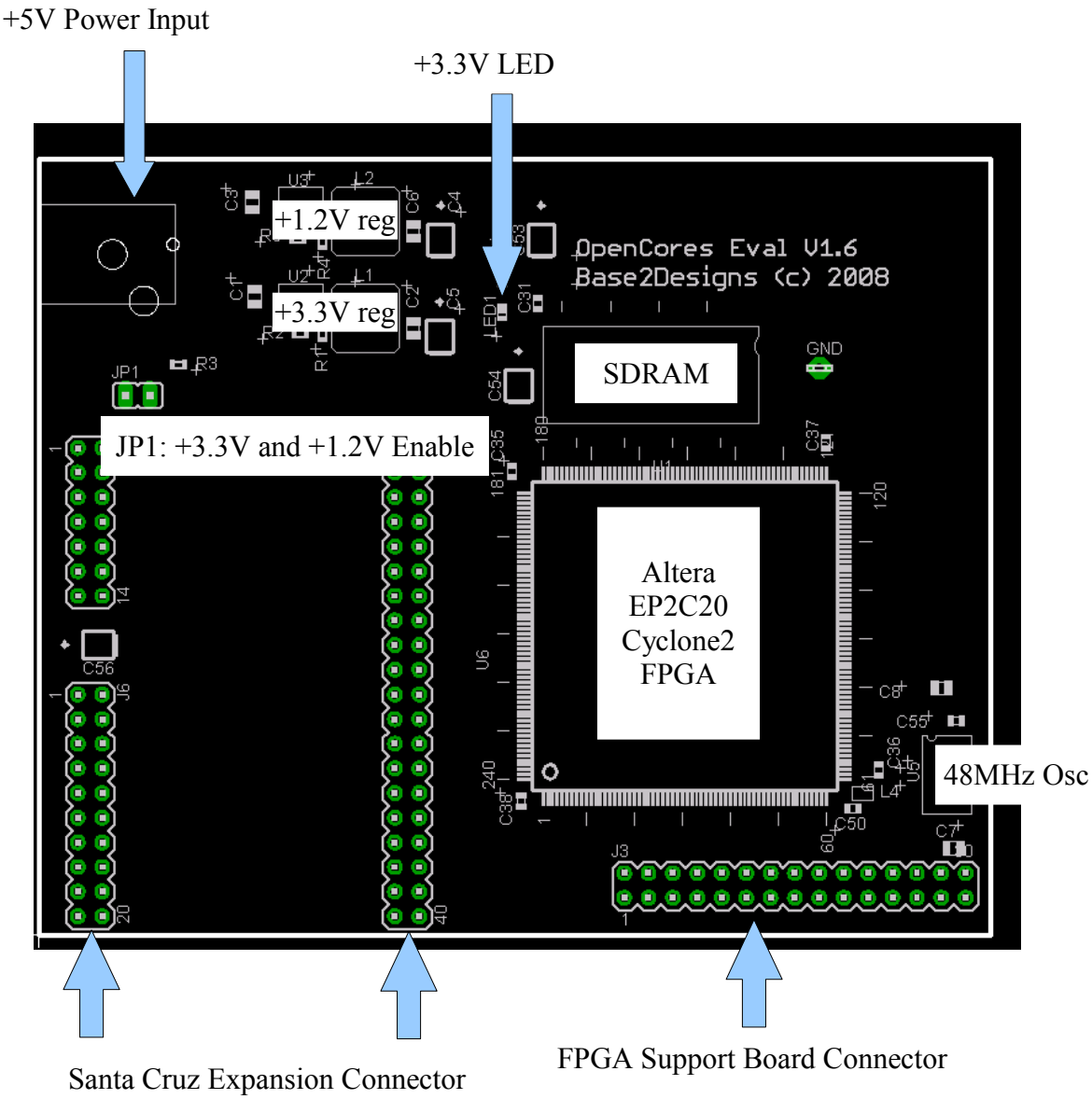
| | | | |

# Contents

# 1

# FPGA Main Board



# 2

# FPGA Support Board

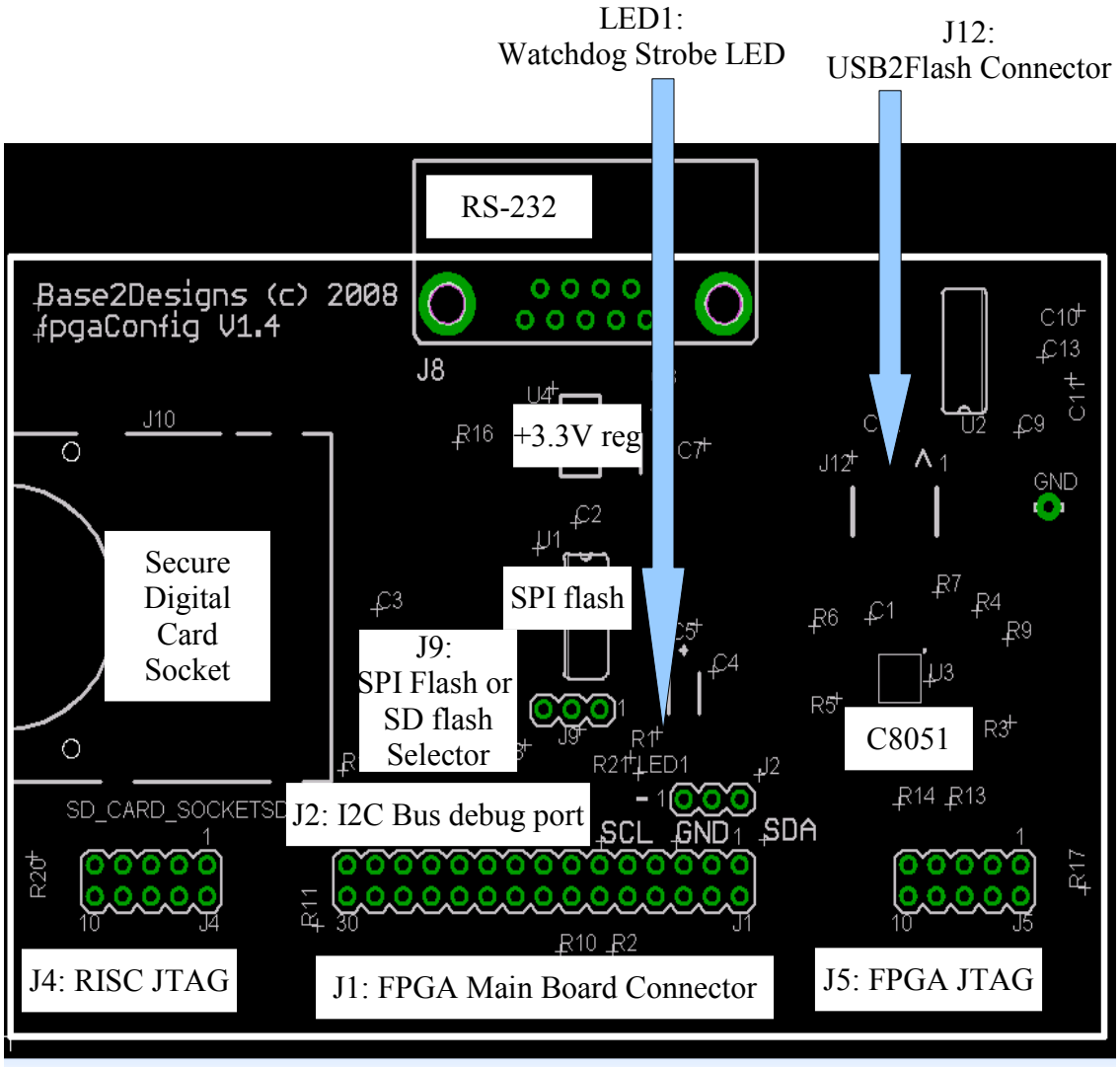
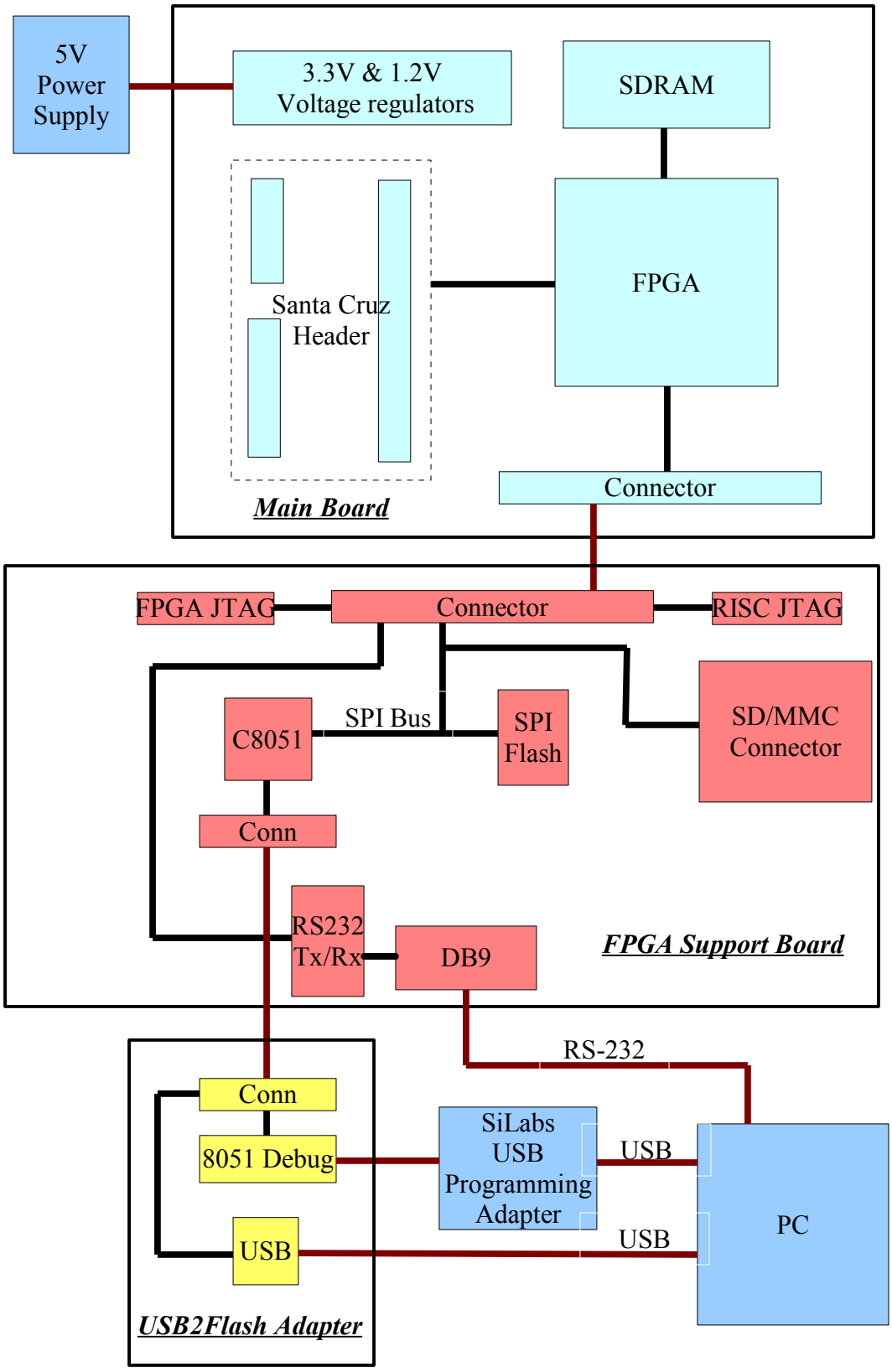


**Figure 2.1 – Hardwdare block diagram**



# 3

# Operation

The Main Board contains a minimal number of components required to support the EP2C20 Cyclone2 FPGA in an OpenRISC application. OpenRISC, is an open source RISC processor, available from OpenCores;

http://www.opencores.org/projects.cgi/web/or1k/overview

A 30-pin ribbon cable connects the Main Board to the FPGA support board. The FPGA Support Board contains all the components required to configure the FPGA using the Base2Designs FPGA configuration scheme. Base2Designs FPGA configuration scheme allows the storage of FPGA configuration files in commodity flash memory, either SPI flash, or SD/MMC flash cards. In addition to storing the FPGA configuration files, the flash memory can be used to store OpenRISC program files. The Support Board also contains a DB9 supporting RS-232 serial communications with the OpenRISC processor, a FPGA JTAG connector useful for running Altera Signal Tap logic analyser, an OpenRISC JTAG connector for OpenRISC software debug, and a USB2Flash connector which supports the Base2Designs USB2Flash Programming adapter.

### Selecting SD flash or SPI flash

As a default the FPGA Support Board is configured for using SD flash cards. If you wish to change to using SPI flash, then you will need to load a new image into the C8051 microcontroller, and change the position of jumper J9. Note, that as of this date the OpenRISC boot loader does not support booting from SPI flash. Never the less, if you have applications that will fit inside FPGA flash memory, you can still use SPI flash. Or if you are not using the OpenRISC then you can also use SPI flash. And since everything is open source, you could modify the boot loader to load from SPI flash.

To select between SPI flash and SD flash you need load the C8051 with an appropriate image, and change the position of jumper J9. You will need a SiLabs Programming adapter in order to re-program the C8051, see the “Base2Designs FPGA Configuration Users Guide” for details. Position the J9 jumper on side closest to the SD flash to use SD flash, and the other side to use SPI flash.

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# Connectors

## Table 1: Main Board Connectors

| Signal | Pin No. | Dir | Description |
|---|---|---|---|
| **Power** | | | |
| +5V | | input | +5V +/- 5% @ 1A. Current consumption is dependent on FPGA usage, but with a typical OpenRISC project loaded, the board consumes ~100mA |
| **JP1 - Regulator Inhibit** | | | |
| | 1 and 2 | | Link the pins to allow the FPGA Support board to control the +1.2V and +3.3V regulator power inhibit pins. Aim is to allow the C8051 to power down the board, thus saving power.<br>Remove the link to default the regulators to on.<br>C8051 feature not implemented, so leave unconnected. |
| **J3 – FPGA Support Board Connector** | | | |
| +5V | 29 | output | +5V from main input connector. |
| +3.3V | 30 | output | +3.3V from regulator. |
| GND | 3, 7, 17, 27, 28 | | Ground |
| MAIN_BRD_PWR_ON | 1 | input | Controls the +1.2V and +3.3V regulator power inhibit pins. High = Power on, low = power off. |
| WATCH_DOG_STROBE | 13 | output | Watchdog strobe output from FPGA. Toggling of output required to prevent C8051 from reseting the system. Details of toggle rate TBD. Currently unimplemented. |
| FPGA JTAG debug port | | | |
| FPGA_TDI | 2 | input | Data in |
| FPGA_TCK | 4 | input | Clock |
| FPGA_TDO | 6 | output | Data out |

| Signal | Pin No. | Dir | Description |
|---|---|---|---|
| FPGA_TMS | 5 | input | Mode select |
| RISC JTAG software debug port | | | |
| RISC_TDI | 22 | input | Data in |
| RISC_TCK | 18 | input | Clock |
| RISC_TDO | 19 | output | Data out |
| RISC_TMS | 20 | input | Mode select |
| RISC_TRST | 21 | input | Reset |
| FPGA Serial Configuration port, and SPI bus | | | |
| FPGA_CONF_CLK | 8 | input | Configuration clock |
| FPGA_CONF_EN_N | 10 | input | Configuration enable. Active low. |
| FPGA_STS_N | 26 | output | Configuration status. Configuration cannot start until this signal is high. |
| FPGA_CONF_DONE | 25 | output | Configuration successfully done. Active high. |
| SPI_MASTER_DOUT | 9 | inout | Configuration data input during FPGA configuration. After FPGA configuration becomes SPI data output from FPGA. Connected to two separate pins on FPGA. DATA0 configuration pin and a regular I/O pin. |
| SPI_MASTER_DIN | 15 | input | SPI data in to FPGA. |
| FLASH_SPI_CLK | 16 | output | SPI clock from FPGA. Tri-state during FPGA configuration. |
| SPI_CS_N | 14 | output | SPI chip select from FPGA. Active low. Tri-state during FPGA configuration. |
| UART | | | |
| UART_TX | 23 | output | Tx data |
| UART_RX | 24 | input | Rx data |
| I2C bus | | | |
| I2C_SCL | 12 | inout | I2C clock signal. Tri-state capable with pull-up on Support board. |
| I2C_SDA | 11 | inout | I2C data signal. Tri-state capable with pull-up on Support board. |
| **J1, J6, J7 - Santa Cruz expansion bus** | | | |
| SC_P_CLK | J6-11 | output | Clock. |
| SC_RST_N | J7-1 | output | Reset |
| SC_CS_N | J7-38 | output | Chip select |
| SC_P[39:0] | See schematic | User defined | User defined |

# Table 2: Support Board Connectors

| Signal | Pin No. | Dir | Description |
|---|---|---|---|
| **J8 - RS-232** | | | |
| TX | 2 | output | Tx data |
| RX | 3 | input | Rx data |
| GND | 5 | | Ground |
| **J4 - OpenRISC JTAG software debug port** | | | |
| +3.3_SW | 7 | output | +3.3V from the main board regulator. Note that this supply will be switched off when the main board regulators are inhibited. |
| GND | 1, 9 | | Ground |
| RISC_TDI | 2 | input | Data in. 1K pull-up |
| RISC_TCK | 10 | input | Clock. 1K pull down. |
| RISC_TDO | 8 | output | Data out |
| RISC_TMS | 6 | input | Mode select. 1K pull-up |
| RISC_TRST | 4 | input | Reset |
| **J5 - FPGA JTAG debug port** | | | |
| +3.3_SW | 4 | output | +3.3V from the main board regulator. Note that this supply will be switched off when the main board regulators are inhibited. |
| GND | 2, 10 | | Ground |
| FPGA_TDI | 9 | input | Data in |
| FPGA_TCK | 1 | input | Clock |
| FPGA_TDO | 3 | output | Data out |
| FPGA_TMS | 5 | input | Mode select |
| **J2 – I2C Debug port** | | | |
| I2C_SCL | 1 | inout | Clock |
| GND | 2 | | Ground |
| I2C_SDA | 3 | inout | Data |
| **J12 – USB2Flash connector for C8051 debug and C8051 UART** | | | |
| UART_RX | 2 | input | C8051 serial receive data in. 3.3V LVTTL logic levels. |
| UART_TX | 4 | output | C8051 serial transmit data out. 3.3V LVTTL logic levels. |
| C2CK | 6 | input | C8051 debug clock |
| C2D | 8 | inout | C8051 debug data |
| NC | 10 | | No connect |
| +3.3V | 1 | output | +3.3V supply from local regulator. Always on. |
| GND | 3, 5, 7, 9 | | Ground |
| **J9 – Flash selection** | | | |
| FLASH_IC_CS_N | 1 | | SI flash chip select |

| Signal | Pin No. | Dir | Description |
|---|---|---|---|
| SPI_CS_N | 2 | | SPI chip select from either C8051 during FGPGA configuration, or FPGA after configuration. Place link between 2 and 1 to select SPI flash, or 2 and 3 to select SD flash. |
| SD_CS_N | 3 | | Secure Digital chip select |
| **J3 – FPGA Main Board Connector** | | | |
| +5V | 29 | input | +5V from Main board input connector. Supply always present. |
| +3.3V_SW | 30 | input | +3.3V from Main board regulator. Supply will be switched off when MAIN_BRD_PWR_ON is low. |
| GND | 3, 7, 17, 27, 28 | | Ground |
| MAIN_BRD_PWR_ON | 1 | output | Controls the +1.2V and +3.3V regulator power inhibit pins. High = Power on, low = power off. |
| WATCH_DOG_STROBE | 13 | input | Watchdog strobe output from FPGA. Toggling of output required to prevent C8051 from reseting the system. Details of toggle rate TBD. Currently unimplemented. |
| *FPGA JTAG debug port* | | | |
| FPGA_TDI | 2 | output | Data in |
| FPGA_TCK | 4 | output | Clock |
| FPGA_TDO | 6 | input | Data out |
| FPGA_TMS | 5 | output | Mode select |
| *RISC JTAG software debug port* | | | |
| RISC_TDI | 22 | output | Data in |
| RISC_TCK | 18 | output | Clock |
| RISC_TDO | 19 | input | Data out |
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| *FPGA Serial Configuration port, and SPI bus* | | | |
| FPGA_CONF_CLK | 8 | output | Configuration clock |
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| FPGA_CONF_DONE | 25 | input | Configuration successfully done. Active high. |
| SPI_MASTER_DOUT | 9 | inout | Configuration data input during FPGA configuration. After FPGA configuration becomes SPI data output from FPGA. Connected to two separate pins on FPGA. DATA0 configuration pin and a regular I/O pin. |
| SPI_MASTER_DIN | 15 | output | SPI data in to FPGA. |

| Signal | Pin No. | Dir | Description |
|---|---|---|---|
| FLASH_SPI_CLK | 16 | input | SPI clock from FPGA. Tri-state during FPGA configuration. |
| SPI_CS_N | 14 | input | SPI chip select from FPGA. Active low. Tri-state during FPGA configuration. |
| *UART* | | | |
| RISC_UART_TX | 23 | input | Tx data |
| RISC_UART_RX | 24 | output | Rx data |
| *I2C bus* | | | |
| I2C_SCL | 12 | inout | I2C clock signal. Tri-state capable with pull-up on Support board. |
| I2C_SDA | 11 | inout | I2C data signal. Tri-state capable with pull-up on Support board. |