0.13µm SoC IP
Fusion Process
Product Overview

Virtual Silicon's Fusion SoC IP is a comprehensive set of library design elements optimized for the UMC L130HS/LL process. Each element is being silicon verified with test chips prior to use in your production design—the result is highly reliable parts. All of the design components adhere to Virtual Silicon's rigorous quality procedures and is process-optimized to achieve the high-density requirements of your designs.

Complex system-on-chip systems can only be achieved with the wide availability of application-specific library components, such as specialized I/O pads and data-path functions. Virtual Silicon's ASIC solution is an "open architecture" that allows interoperability of library components from multiple design sources.

Open Architecture Developers' Kits are available for both in-house development teams and third-party IP providers. Designers can now leverage foundation technology without needing to re-invent the base architecture.

0.13µm WL130 LL/HS 1.2V Fusion Process

Benefits

- **Ability to mix and match high-speed and low leakage IP**
- **Reduces active power by up to 20%**
- **Reduces stand by leaking curent by ½ to 1/1000**
- **Improve stand by battery life by a factor of 4**

Silicon Ready

- **Engineered to foundry's exact process for optimum density and performance**
- **Proven test chips insure first time silicon success**
- **High resolution EDA models assure rapid timing convergence**

*e*Si-Route/9™ Standard Cells

- 1.2 volt and 0.9 volt standard cells
- 550+ function high density standard cells
- Wide choice of combinatorial and sequential functions
- Multiple drive strengths allow optimal gate usage during synthesis
- Hand-crafted layouts Achieves Ultra High Density – Average Cell density up to 220K gates/sq.mm
- Careful choice of routing grid allows dense place and route
- Fully buffered at input and output stages
- Accurate timing and power characterization

*e*Si-Pad™ I/O Functions

- 60+ 1.8v, 70µ Pad Pitch, CMOS/TTL I/O pads
  - Slew rate control, schmitt, pull-up, pull-down, etc.
- 200 + 3.3v, 35 & 70µ Pad Pitch, CMOS/TTL I/O Pads
  - Slew rate control, schmitt, pull-up, pull-down, etc.
- Maximum drive up to 24mA
- ESD and latch-up structures for high reliability
  - Minimum ESD: 4KV HBM, 250V MM
  - Minimum latch-up immunity: 300mA at 100C
- Built-in level shifter for core logic interface

*e*Si-RAM™ and *e*Si-ROM™ Memory Compilers

- Performance optimized high density memory compilers
  - Single port, dual port and diffusion ROM
- Fully static and synchronous design triggered off the rising edge of the clock
- Ram Memory arrays utilizing high-density bit cells
- Byte-write capability on SRAM arrays
- Compiler allows designers to perform architectural tradeoffs for aspect ratios and speed
- Fully automated EDA model generator and licensed physical layout compiler

*e*Si-PLL™ Programmable PLL Compiler

- High speed programmable PLL with user selectable center frequency and duty cycle
- Input Frequency: 24MHz to 200MHz; Output Frequency: 50MHz to 1GHz
- Integrated loop filter and oscillator offers very high stability and noise margin
- Entire module located under AVDD and AVSS pads
- Compiler technology eliminates user error and greatly enhances ease of use

Open Architecture

- Developers kit for standard cells and I/O libraries
- Facilitates users to create compatible standard cell and I/O
- Standard Cell Open Architecture Design Kit
  - Layout architecture, cell naming conventions, characterization conditions, modeling considerations
- I/O Open Architecture Design Kit
  - Layout architecture, power bussing, I/O border cell, cell naming, characterization conditions

EDA Tool Support

Select other EDA tools supported on standard or customer basis.

	Avant!	Cadence	Mentor	Synopsys	Simplex
Logic Synthesis		BuildGates		Design Compiler & Physical Synthesis	
Simulation		NC-Verilog NC-VHDL	ModelSim	VCS	
Timing & Power		Pearl		PrimeTime PrimePower	Voltage Storm
Place & Route	Apollo	Silicon Ensemble			
Extraction & Delay Calc.	Star-RC Star-DC	TLF	xCalibre	Arcadia	Fire & Ice
Physical Verification	Hercules	Dracula	Calibre		
Testability			FastScan	Test Compiler TetraMax	

Worldwide Inquiries

Email:
info@virtual-silicon.com
www.virtual-silicon.com

Continental Europe & Israel

Virtual Silicon Technology
Drève de Corps du Garde 104
7850 Petit Enghien, BELGIUM
Tel: 32 (2) 395-8991
Fax: 32 (2) 395-3856

Virtual Silicon Technology
Engelska Huset, Trappvägen 9
132-42 Saltsjö-Boo, SWEDEN
Tel: 46 (8)747-1741
Fax: 46 (8)747-1745

Virtual SiliconTechnology
Cherry Tree House Station Rd.
Sunningdale, Berkshire
SL5 OQR, UK
Tel: 44 (1)344-624-970
Fax: 44 (1) 344-624-960

Japan

Soliton Systems K.K.
2-4-3 Shinjuku,
Shinjuku-ku, Tokyo 160
Tel: 03-5360-3851
Fax: 03-3356-6440

Company Headquarters

Virtual Silicon Plaxa
1200 Crossman Ave.
Sunnyvale, CA. 94089
Tel: (408) 548-2700
Fax: (408) 548-2750