PCI Express 16-bit VERA Testbench

FEATURES

- 16 bit PIPE Spec PCI Express Testbench
- Link training
- Initial Flow Control
- Packet Classes for easy to build PHY,DLLP and TLP packets
- DLLP 16 bit CRC and TLP LCRC generation
- Sequence Number generation and checking
- ACK TLP packets
- Scrambling

Functional Description and Background

This testbench has been designed to resemble the TI XIO1100 X1 PHY which has a 16 bit 125 MHz PIPE spec interface. This is a great PCI Express starter VERA testbench. It can easily be added to, to get the desired results. The testbench performs link training, initial flow control and TLP generation. The entire packet is built up including starting and ending symbols as well as the correct LCRC values. The testbench can be modified fairly easily to put out 8 bits at a time rather than 16 bits.

Link Training

The testbench looks for a receiver detect sequence and then a power change sequence to put it into operational mode. After the PHY is in operational mode training sets will be sent out. Initially TS1 order sets will be sent by the testbench. The testbench will also receive TS1 order sets and process them. When the device under test sends TS2 order sets the testbench will respond with TS2 order sets. Then the link and lane negotiation will be preformed. After the logical idles the Testbench will indicate link up.
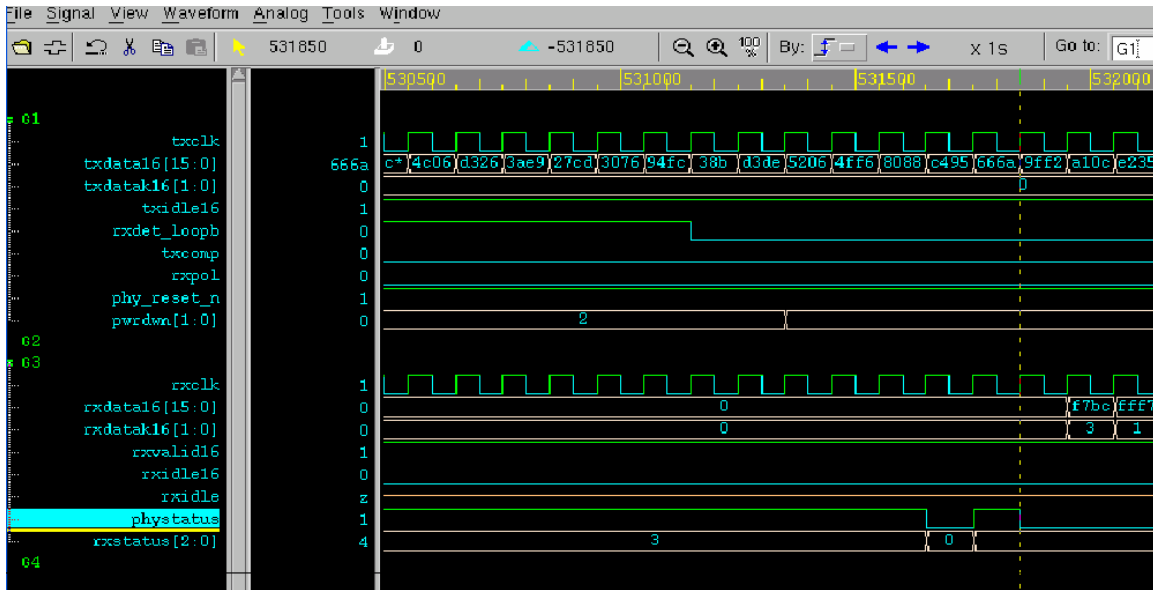
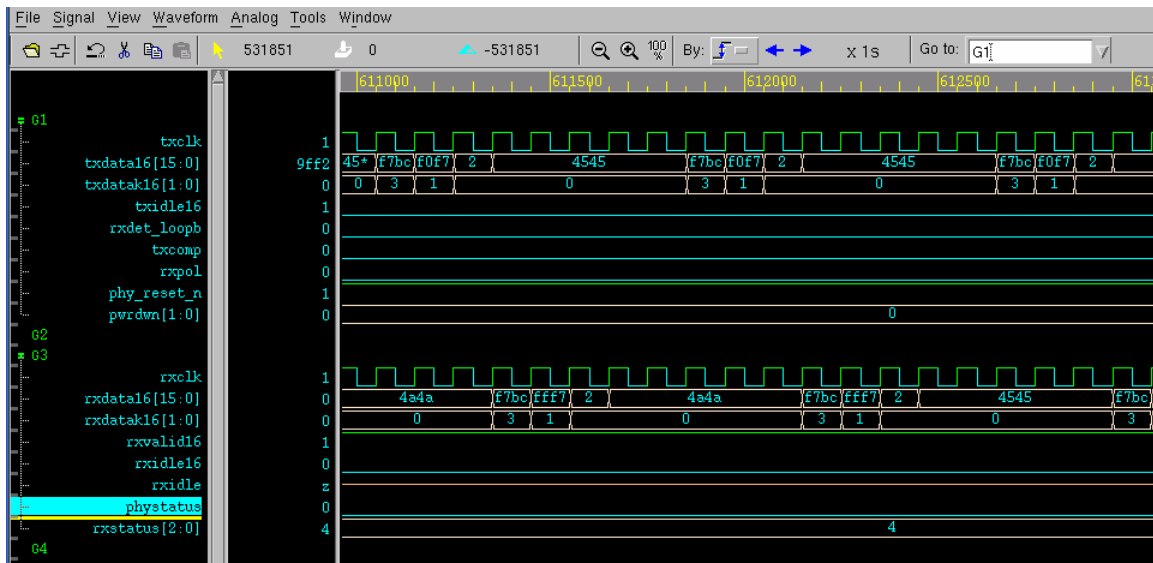Figure 1 Waveform of Receiver Detect and Power change

Figure 2 Waveform of Training Set Transition from TS1 to TS2

Initial Flow Control

After link up the testbench will generate and receive DLLP initial flow control packets. These packets include initial credits for non-posted, posted and completion credits. These are DLLP packets that have the correct LCRC values attached.

The initial flow control credits can be easily changed. Here is a table of there default values.

Type	Value
Non-Posted Credit	4 header credits
Posted Credit	4 header credits, 1k data credit
Completion Credit	4 header credits, 1k data credit

Skip Order Sets

The testbench will send out skip order sets on a regular basis.

TLP Packet Generation

There are built in tasks for CfgWr; CfgRd; MemWr and MemRd packet types. Based on these packets other packet types can easily be made. The sequence number and LCRC values are correctly generated by the Testbench. The tasks accept requestor id, byte enables, length, address, tag etc. to allow many unique packet to be generated.

Data Scrambling/De-scrambling

The testbench scrambles the 16 bits of data based on the PCI express rules. Scrambling can be bypassed in the testbench. Scrambling is applied to Data characters associated with DLLPs and TLPs including logical idles and Data characters TS1 and TS2 ordered sets. K characters are not scrambled and bypass the scramble logic. Compliance pattern related characters are not scrambled. When a COM character exits the scrambler the COM does not get scrambled, but it initializes the LFSR to 16'hFFFF. Similarly on the receive side the COM character initializes the de-scrambler to 16'hFFFF. The LFSR does not advance on SKP characters. Gutz Logic also offers a 16 bit RTL scrambler/descrambler code.

File Description

File	Description
run_vera	This is the command file to run
ti_phy_top.test.top.v	Top level testbench linking Vera with the RTL
ti_phy_top.if.vrh	Interface file
ti_phy_top.v	Top level non-synthesizable RTL file(add your RTL HERE)
receive_packet.vri	VERA file for receiving all PCIe packets 16 bits at a time
send_packet.vri	VERA file for sending all PCIe packets 16 bits at a time
pcie_phy_packet.vri	VERA file class for PHY layer packets
pcie_dllp_packet.vri	VERA file class for DLL layer packets
pcie_tlp_packet.vri	VERA file class for TLP layer packets
link_training.vri	VERA file for Link Training
tlp_gen.vri	VERA file for generating TLP packets
InitFC1.vri	VERA file for Credit Initialization
skip_order_set.vri	VERA file for generating Skip Order Sets
scramble8.vri	VERA file for scrambling and descrambling the data

Additional Tasks to be Added

The testbench currently does not include credit updates and credit control. Additional Packet processing including Messages; IOWR; IORD and completion packets. Error Checking, Data compare functions and NACK generation needs to be added Additional PIPE spec functions such as loopback, electrical idles, Serdes errors.