Using In-System Programming in Boundary-Scan Systems

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Summary

This application note discusses basic design considerations for in-system programming (ISP) of multiple XC9500 devices in a Boundary-Scan chain and shows how to design systems that contain multiple XC9500 devices as well as other IEEE 1149.1-compatible devices.

Note: The "Basic Boundary-Scan Design Guidelines" and "Debugging Boundary-Scan Systems" sections within this application note apply to all Xilinx devices that support Boundary-Scan.

Introduction

The XC9500 family performs both in-system programming and IEEE 1149.1 Boundary-Scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment (ATE) to perform both functions. Xilinx also provides the software that programs and tests XC9500 devices.

XC9500 TAP Characteristics

The AC and DC characteristics of the XC9500 TAP are described below.

TAP Timing

Figure 1 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both Boundary-Scan and ISP operations. The timing for the INPUT-I/O-CLK and I/O signals is relevant to Boundary-Scan operations (such as EXTEST) that activate or strobe the system pins.

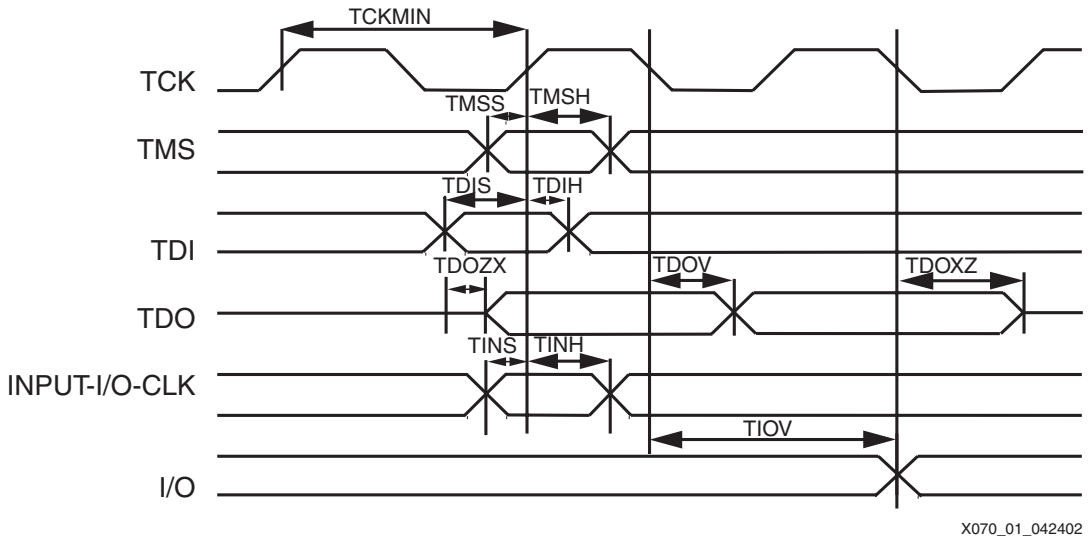

Figure 1: **Test Access Port Timing**

TAP AC Parameters

Table 1 shows the timing parameters for the TAP waveforms shown in Figure 1.

Table 1: **XC9500 Test Access Port Timing Parameters (ns)**

Symbol	Parameter	Min	Max
TCKMIN	TCK Minimum Clock Period	100	
TMSS	TMS Setup Time	10	
TMSH	TMS Hold Time	10	
TDIS	TDI Setup Time	15	
TDIH	TDI Hold Time	25	
TDOZX	TDO Float to Valid Delay		35
TDOXZ	TDI Valid to Float Delay		35
TDOV	TDO Valid Delay		35
TINS	I/O Setup Time	15	
TINH	I/O Hold Time	30	
TIOV	EXTEST Output Valid Delay		55

Terminating TAP Pins

The XC9500 TDI and TMS pins have internal 15-kΩ pull-up resistors required by the IEEE 1149.1 standard. Because these pins are internally terminated, no further termination is required on the TAP connections.

Capacitive Decoupling

Decouple the V_{CC} input with a 0.1 µF capacitor connected to the nearest ground plane (low-inductance surface mount capacitors are recommended). Decouple the printed circuit board power inputs with 0.1 µF ceramic and 100 µF electrolytic capacitors. This helps to provide a stable, noise-free power supply to the ISP parts.

Free Running Oscillators

Boundary-Scan operations often involve the transmission of long streams of data through long and complex paths that traverse the entire system. Often, the presence of active clocks and free running oscillators couple noise onto the Boundary-Scan chain TAP signals. To increase the reliability of Boundary-Scan and ISP operations, equip the system with a clock and oscillator disable. The disable should be activated for all test and program operations when using the download cable, ATE, or third-party systems.

Calculating Maximal Chain Lengths

The XC9500 TAP pins have approximately 5 pF of signal loading. Because each TDI input is driven by only one TDO output (or equivalent single drive), there are no signal limitations related to those connections beyond those of standard board interconnect design rules.

The maximum TDO frequency is one half of the maximum TCK frequency. Because TCK and TMS are parallel driven signals, the maximum number of parts in a single Boundary-Scan chain is determined by the ability of the TCK and TMS drivers to deliver the signals at the appropriate frequencies to the parts in the Boundary-Scan chain. Standard board-layout design rules also apply here.

If the Boundary-Scan chain includes more than six devices, buffered distribution of TMS and TCK are recommended.

Part Enable Ordering

The ISPEX instruction allows the flexibility to enable parts in an arbitrary order. In some systems, the order in which parts are enabled is critical. For instance, if a slave device awakens before its controller, it can enter an error condition from which it cannot exit.

The iMPACT software enables each part immediately after programming. In concurrent mode, the parts are enabled simultaneously.

Creating Boundary-Scan Chains

There are a number of possibilities for creating Boundary-Scan chains, several of which are discussed in the following sections. The single-port serial chain is the recommended topology for in-system programming via Xilinx iMPACT software and cables. Other more complex chain variations are also discussed. However, the Xilinx software does not directly support the more complex chain topologies. Some third-party Boundary-Scan tool vendors support these complex chain configurations. Only Boundary-Scan experts should attempt to use the more complex topologies.

Single-Port Serial Chain

The most simple and widely-used Boundary-Scan configuration is the single port serial chain shown in Figure 2, and only this type of configuration is supported by the iMPACT software. In this configuration, four pins are allocated in the system to facilitate connection of the TCK (clock), TMS (mode), TDI (Test Data Input), and TDO (Test Data Output) signals.

All devices in the chain share the TCK and TMS signals. The system TDI signal is connected to the TDI input of the first device in the Boundary-Scan chain. The TDO signal from that first device is connected to the TDI input of the second device in the chain and so on. The last device in the chain has its TDO output connected to the system TDO pin.

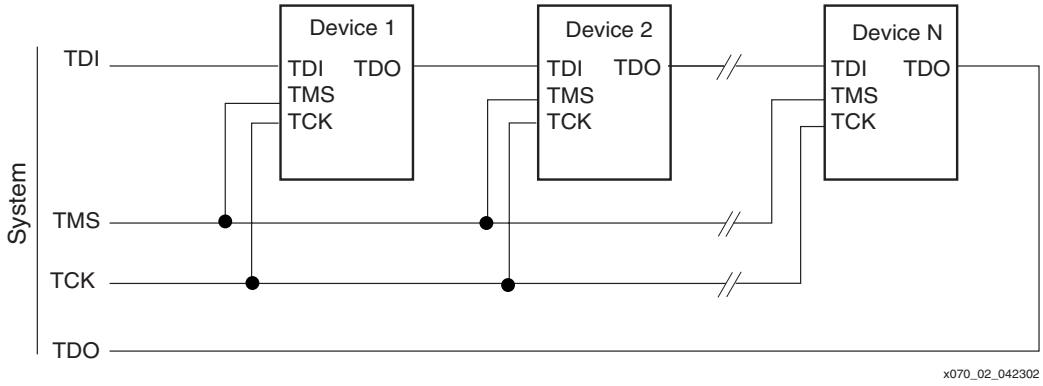

Figure 2: **Single-Port Serial Boundary-Scan Chain**

Star Configuration

The single port serial chain, shown in Figure 3, configuration has a significant limitation due to the possibility that a defect in the backplane wiring or the removal of a board from the system can break the chain. This would make ISP and system testing impossible. In order to overcome this limitation and make the 1149.1 standard practical for very large systems, the standard allows the connection of Boundary-Scan chains in star configuration in which the four pins of the TAP are multiplexed. The costs of this approach are the additional overhead required to switch between scan paths, and the reduced TCK frequency due to TMS routing delays.

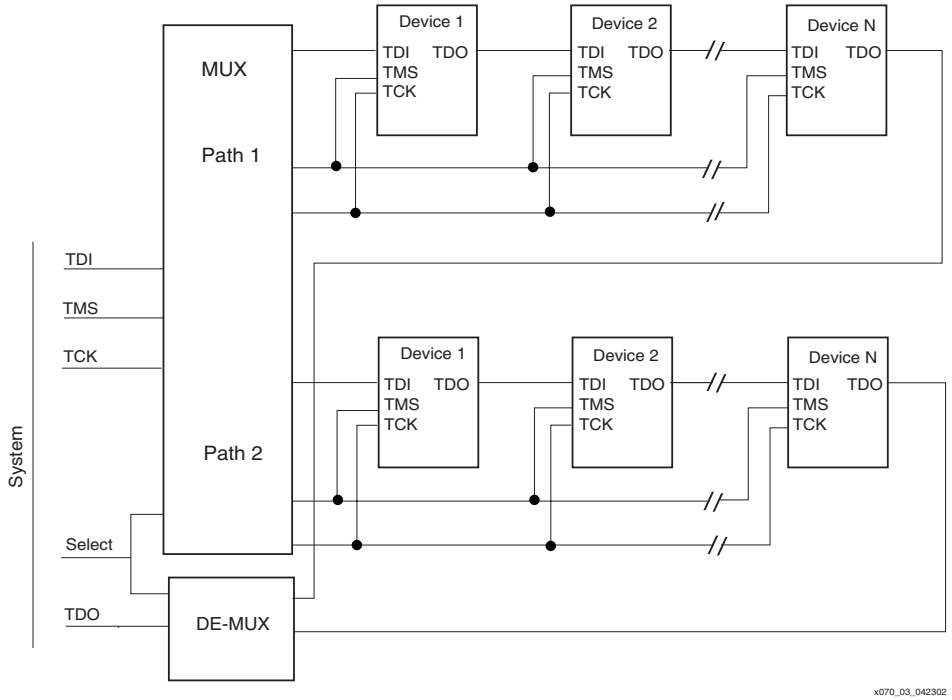

Figure 3: **Star Configuration**

Caution! The external MUX and select hardware must disconnect the primary TMS or TCK from the deselected scan chain to prevent unexpected behavior on the deselected scan chain.

Multiple Independent Paths

In the topology shown in Figure 4, the TDI and TDO paths are independent allowing data to be streamed into and out of the portions of the system independently.

Caution! This topology is not recommended for use with the Xilinx iMPACT software and cables.

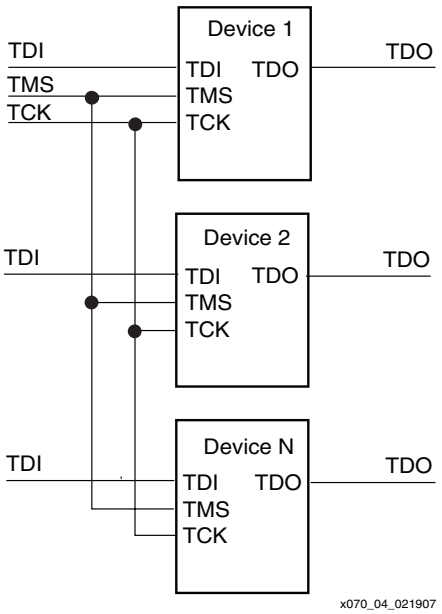

Figure 4: **Multiple Independent Chains**

Parallel Chains

In the topology shown in Figure 5, TDI and TMS inputs are independent but the TDO is shared. This means that although data can be streamed into portions of the system independently, data being streamed out is time multiplexed through TMS control.

Caution! This topology is not recommended for use with the Xilinx iMPACT software and cables.

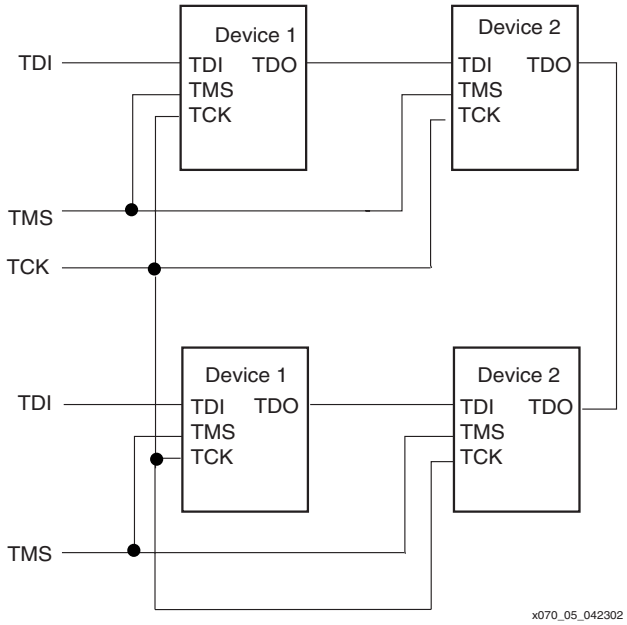

Figure 5: **Parallel Chains**

In-System Programming

Using the Xilinx Download Cables

The iMPACT software can be used with any of the Xilinx download cables including the Parallel Cable IV or Platform Cable USB.

The Xilinx cables can be used on PCs running Microsoft Windows or RedHat Linux operating systems. See the Xilinx Software Manuals for operating system support details.

The cables include port protection and drive circuitry. See the Cable Data Sheets for operating recommendations and specifications.

Concurrent Program and Erase Modes

One operating mode of the iMPACT software performs concurrent erasing and programming. The advantage of this approach is speed; the overall programming time is dictated by the slowest part in the Boundary-Scan chain. Also, the total number of vectors required is optimized. The disadvantage of this approach is that the system must supply a peak operating current equal to that required by all parts being programmed or erased concurrently. For more information on how to use this feature in iMPACT, please see the Xilinx iMPACT Software Manual.

ISP Mode I/O Behavior

The functional pins of the device transition to a high-impedance state when ISP mode is entered using the ISPEN instruction. At the completion of an ISP programming or erase operation, the ISPEX instruction is executed. When leaving ISPEX mode (by shifting in an new Boundary-Scan instruction other than ISPEN), the device initializes to its programmed state; the functional pins take on their selected operations (input, output, or bidirectional) and the device registers take on their pre-selected initial values.

System-Level Design Issues

The normal operating mode of a system or a device in the system is known as mission mode which is different from test mode. When operating a device in Boundary-Scan test mode (such as when using either INTEST or EXTEST) as well as when performing ISP operations, the device is effectively disconnected from the overall system. When the operation is completed, the device is re-connected to the system. This can sometimes result in unpredictable system behavior. Additional discussion regarding this problem can be found in [Ref 3]. Fortunately, the XC9500 family supplies two proprietary Boundary-Scan instructions that serve to alleviate this problem.

XC9500 Mission Mode Exit and Re-Entry Techniques

The XC9500 devices support two Boundary-Scan instructions that can be used to help alleviate the problems associated with exiting and re-entering mission mode. The instructions are ISPEN (ISP enable) and ISPEX (ISP exit).

- **ISPEN** – The ISPEN instruction is used at the beginning of every block of ISP operations attempting to access for alteration or read the device internal program memory (such as program, erase, verify, etc.). When the device is in ISPEN mode, the device I/O pins immediately enter a state in which they are floating with a weak pull-up resistor enabled on each pin. The device pins therefore neither drive nor sense external signal levels.
- **ISPEX** – The ISPEX instruction is used to conclude every block of ISP operations that have either been read from or written to the device internal program memory. As long as the ISPEX instruction remains in the instruction register the functional pins remain in their lightly pulled-up high-impedance state. After the ISPEX instruction is replaced with any other Boundary-Scan instruction (except ISPEN), the device returns to its initial power state with the pins configured to their programmed states (input, output, or bidirectional) and with the device flip-flops taking on their initial states.

The ISPEX operation takes approximately 100 μs to complete. If the ISPEX instruction is held in the instruction register for longer than 100 μs, the ISPEX operation does not take effect until the ISPEX instruction is displaced from the instruction register.

In order to ensure safe operation, all INTEST, EXTEST, and ISP operations involving the XC9500 parts should be bracketed by ISPEN and ISPEX instructions.

The designer must also be careful to select an initial condition that is system-safe so that when the ISPEX instruction is released, the XC9500 part in question safely resumes operation with the rest of the system.

Basic Boundary-Scan Design Guidelines

The following guidelines help ensure a successful design.

- Make certain that all parts in the Boundary-Scan chain have 1149.1 compatible test access ports.
- Use clock buffering techniques for TCK/TMS signals, to ensure signal integrity and to simplify test considerations for the Boundary-Scan TAP. If buffers are used, ensure input termination is present on the buffers such that the TCK/TMS signals are held at fixed logic levels when no cable is connected.
- Do not invert TCK or TMS pathways, to guarantee complete test software compatibility.
- Group similar device families, and have a single level converter interface between them, for TCK, TMS, TDI, TDO, and system pins.
- Check that the mission logic is safe from any possible errors that might arise while the Boundary-Scan data is being shifted through the Boundary-Scan chain. For example, pay close attention to bus enable or chip select signals that might be enabled simultaneously, causing unexpected bus contention.

- Provide the capability for the ATE to disable conventional (non Boundary-Scan) IC's whose run-time node values might introduce conflicts with Boundary-Scan logic values during test operations.
- Verify that the entire system is held in a benign state during Boundary-Scan test operations.
- Verify that the set-up and hold times of TDI and TMS with respect to TCK are met by the system.

Debugging Boundary-Scan Systems

The following guidelines and helpful information help isolate potential problems.

- The iMPACT Initialize Chain operation automatically identifies devices within the Boundary-Scan chain. Devices are identified beginning with the last device in the chain because the IDCODE of the last device is the first to appear on the final TDO output.
  - If the Initialize Chain operation does not identify any devices, then check for proper power to the devices in the Boundary-Scan chain, check the TCK and TMS signals for opens or shorts, and check the final TDO signal path for an open or short.
  - If a fewer than expected number of devices are identified, then check for an open or short on the TDI pin of the first device shown in the iMPACT Boundary-Scan view. The first device in the Boundary-Scan view is the last device for which iMPACT received an IDCODE. A breach in the serial signal path preceding the device prevents iMPACT from identifying further devices.
- The iMPACT Debug menu contains several items that help debug Boundary-Scan issues. The Chain Integrity Testing and IDCODE Looping functions in the Debug menu can help identify signal integrity issues in the Boundary-Scan chain.
- When traversing the IR states, the CAPTURE-IR value specified in the BSDL file is always shifted out on TDO at SHIFT-IR. This fact can be used to test Boundary-Scan chain continuity.
- After exit from Test-Logic-Reset, if the system transitions directly to Shift-DR, the values shifted out on TDO must be either the IDCODE (if implemented) or the BYPASS register contents. If all logic 0s are shifted in at TDI, then the first incidence of a logic 1 on TDO represents the first bit of an IDCODE. This fact can be used for blind interrogation of the Boundary-Scan chain and for further Boundary-Scan chain continuity checks.
- When entering ISP mode via the ISPEN instruction, all XC9500 function pins float to a weakly pulled-up high-impedance state. The pins can easily be tested for this behavior.
- When ISPEX is shifted out of the instruction register, the XC9500 devices should take on their programmed values with the functional pins acting immediately as inputs or outputs, as programmed. The pins can easily be tested for this behavior.
- TDO assumes its defined value at the falling edge of TCK.
- When not in SHIFT-IR or SHIFT-DR, TDO exhibits high-impedance.
- The last valid TDI bit clocks into the TAP with TMS High.
- In BYPASS mode, TDO equals the applied TDI data one TCK pulse earlier.

Conclusion

When designing ISP systems, common-sense rules related to electronic system design and board layout should be adhered to. In order to benefit from the synergies associated with the integration of test and programming operations, the designer must consciously design with the entire system life cycle in mind.

References

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2. Colin Maunder and Rod Tulloss, *The Test Access Port and Boundary-Scan Architecture*, ISBN: 0-8186-9070-4.
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5. Hideo Fujiwara, *Logic Testing and Design for Testability*, ISBN: 0-262-06096-5.
6. M. Montrose, *Printed Circuit Board Design Techniques*, ISBN: 0780311310.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/01/97	1.0	Xilinx initial release.
05/22/02	2.0	Revised release.
02/19/07	2.1	• Updated format. • Removed references to the discontinued MultiLINX cable. • Corrected connection in Figure 4, page 4. • "Basic Boundary-Scan Design Guidelines," page 6 updated.
11/15/07	2.1.1	• Updated URLs. • Updated template.

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