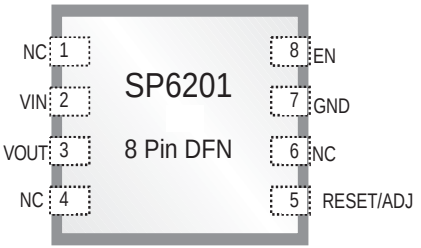
SP6200/6201

Micropower, 100mA and 200mA CMOS LDO Regulators

FEATURES

- Low Dropout Voltage: 160mV @ 100mA
- High Output Voltage Accuracy: 2%
- Ultra Low Shutdown Current: 1μA Max
- Ultra Low GND Current:
  - 200μA @ 200mA Load
  - 28μA @ 100μA Load
- Extremely Tight Load and Line Regulation
- Current and Thermal Limiting
- RESET Output (V_{OUT} good)
- Logic-Controlled Electronic Enable
- Unconditionally Stable with 1μF Ceramic
- Fixed Outputs:
  - 1.5V, 1.8V, 2.5V, 2.7V, 2.85V, 3.0V, 3.3V, 3.5V, 5V
- Adjustable Output Available
- Tiny DFN Package (2mmX3mm) or SOT23-5

Now Available in Lead Free Packaging



APPLICATIONS

- Cellular Telephones
- Laptop, Notebooks and Palmtop Computers
- Battery-Powered Equipment
- Consumer/ Personal Electronics
- SMPS Post-Regulator
- DC-to-DC Modules
- Medical Devices
- Data Cable
- Pagers

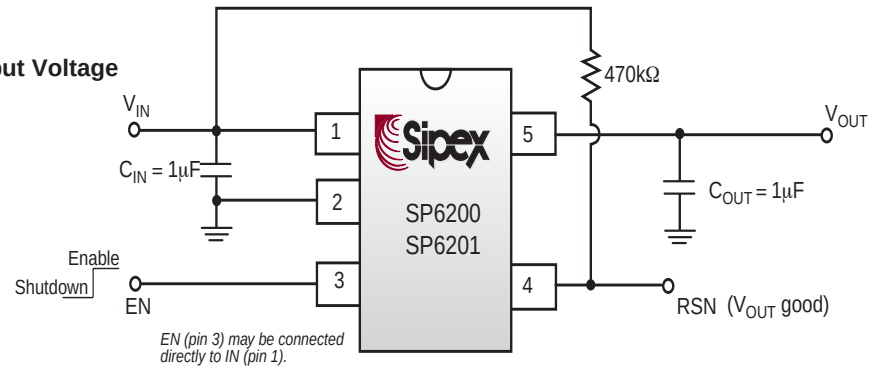
DESCRIPTION

The SP6200 and SP6201 are CMOS Low Dropout (LDO) regulators designed to meet a broad range of applications that require accuracy, speed and ease of use. These LDOs offer extremely low quiescent current which only increases slightly under load, thus providing advantages in ground current performance over bipolar LDOs. The LDOs handle an extremely wide load range and guarantee stability with a 1μF ceramic output capacitor. They have excellent low frequency Power Supply Rejection Ratio (PSRR), not found in other CMOS LDOs and thus offer exceptional Line Regulation. High frequency PSRR is better than 40dB up to 400kHz. Load Regulation is excellent and temperature stability is comparable to bipolar LDOs. An enable feature is provided on all versions.

The SP6200/6201 is available in fixed and adjustable output voltage versions in tiny DFN and small SOT-23-5 packages. A V_{OUT} good indicator is provided on all fixed output versions.

TYPICAL APPLICATION CIRCUIT

Fixed Output Voltage



ABSOLUTE MAXIMUM RATINGS, NOTE 1

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Input Voltage (V_{IN}) ..... -2V to 7V
Output Voltage (V_{OUT}) ..... -0.6 to (V_{IN} +1V)
Enable Input Voltage (V_{EN}) ..... -2V to 7V
Power Dissipation (P_D) ..... Internally Limited, Note 3
Lead Temperature (soldering 5s) ..... 260°C
Storage Temperature ..... -65˚C to +150˚C

OPERATING RATINGS, NOTE 2

Input Voltage (V_{IN}).....+2.5V to +6V
Enable Input Voltage (V_{EN}).....0V to +6V
Junction Temperature (T_J).....-40˚C to +125˚C
Thermal Resistance (See Note 3):
SOT-23-5 (θ_{JA}).....191˚C/W
8 Pin DFN (θ_{JA})..... .....59˚C/W
(See Note 3)

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{OUT} +1V, V_O = 5V for ADJ, I_L = 100µA, C_{IN} = 1.0µF, C_{OUT} = 1.0µF, T_J = 25˚C , unless otherwise specified. The ♦ denotes the specifications which apply over the full operating temperature range, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNIT	♦	CONDITIONS
Output Voltage Accuracy, (V_O)	-2 -3		2 3	% %	 ♦	Variation from specified V_{OUT}
Reference Voltage	1.213	1.250	1.287	V	♦	Adjustable version only
Output Voltage Temperature Coefficient, Note 4, ($\Delta V_O/\Delta T$)		60		ppm/ °C		
Minimum Supply Voltage		2.50 2.55 2.70 3.00	2.70 2.80 2.95 3.50	V V V V		I_L = 100µA I_L = 50mA I_L = 100mA I_C = 200mA
Line Regulation, (ΔV_O/ V_{IN})		0.03	0.2	%/ V	♦	V_{IN} = (V_{OUT} + 1V) to 6V
Load Regulation, Note 5, (ΔV_O / V_O)		0.07 0.14	0.25 0.50	% %	♦ ♦	I_L = 0.1mA to 100mA, SP6200 I_L = 0.1mA to 200mA, SP6201
SP6200-1.5V & 1.8 Load Regulation SP6201-1.5V & 1.8 Load Regulation		0.3 0.3	1 1	% %		I_L = 0.1mA to 100mA, V_{IN} = 2.95V I_L = 0.1mA to 200mA, V_{IN} = 3.5V
Dropout Voltage, Note 6, (V_{IN} – V_O) (Not applicable to voltage options below		0.2	4 7	mV mV	 ♦	I_L = 100µA
2.7V)		70	120 160	mV mV	 ♦	I_L = 50mA
		160	250 300	mV mV	 ♦	I_L = 100mA
		320	400 500	mV mV	 ♦	I_L = 200mA, SP6201 Only
Shutdown Quiescent Current, (I_{GND})		0.01	1	µA	♦	V_{EN} ≥ 0.4V
Ground Pin Current, Note 7, (I_{GND})		28	40 45	µA µA	 ♦	V_{EN} ≥ 2.0V, I_L = 100µA
		110	200 250	µA µA	 ♦	V_{EN} ≥2.0V, I_L = 100mA, SP6200 only (for 1.5 & 1.8, V_{IN} = 2.95)
		200	400 500	µA µA	 ♦	V_{EN} ≥2.0V, I_L = 200mA, SP6201 Only (for 1.5 & 1.8, V_{IN} = 3.5)
Power Supply Rejection Ratio, (PSRR)		78 40		dB		Frequency =100Hz, I_L =10mA Frequency = 400Hz, I_L =10mA
Current Limit, (I_{CL})	100 300	140 420	200 600	mA mA	♦ ♦	SP6200 SP6201
Thermal Limit		162 147		°C °C		Turns On Turns Off

ELECTRICAL CHARACTERISTICS: Continued

$V_{IN} = V_{OUT}$ +1V, V_O = 5V for ADJ, I_L = 100µA, C_{IN} = 1.0µF, C_{OUT} = 1.0µF, T_J = 25°C , unless otherwise specified. The ♦ denotes the specifications which apply over the full operating temperature range, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
Thermal Regulation, Note 8, ($\Delta V_O/\Delta P_D$)		0.05		%/W		
Output Noise, (e_{no})		150		µVrms		I_L = 50mA, C_L = 1µF 0.1µF from V_{OUT} to Adj. 10Hz to 100kHz
ENABLE INPUT						
Enable Input Logic-Low Voltage, (V_{IL})			0.4	V	♦	Regulator Shutdown
Enable Input Logic-High Voltage, (V_{IH})	1.6			V	♦	Regulator Enabled
Enable Input Current, (I_{IL}), (I_{IH})		0.01	1	µA	♦	V_{IL} < 0.4V
		0.01	1	µA	♦	V_{IH} > 2.0V
Reset Not Output	-2	-4	-6	%		Threshold

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D\,(MAX)} = (T_{J\,(MAX)} - T_A) / \theta_{\theta A}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The θ_{JA} of the SP6200/6201 (all versions) is 191°C/W for the SOT-23-5 and 59°C/W for the DFN package on a standard 4 layer board (see "Thermal Considerations" section for further details).

Note 4. Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 5. Load Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range; from 0.1mA to 100mA, SP6200; from 0.1mA to 200mA, SP6201. Changes in output voltage due to heating effects are covered by the thermal regulation specification. Not applicable to output voltages less than 2.5V.

Note 6. Dropout Voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential. Not applicable to output voltages less than 2.7V.

Note 7. Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

Note 8. Thermal regulation is defined as the change in output voltage at a time "t" after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 100mA load pulse at V_{IN} = 6V for t = 10ms.

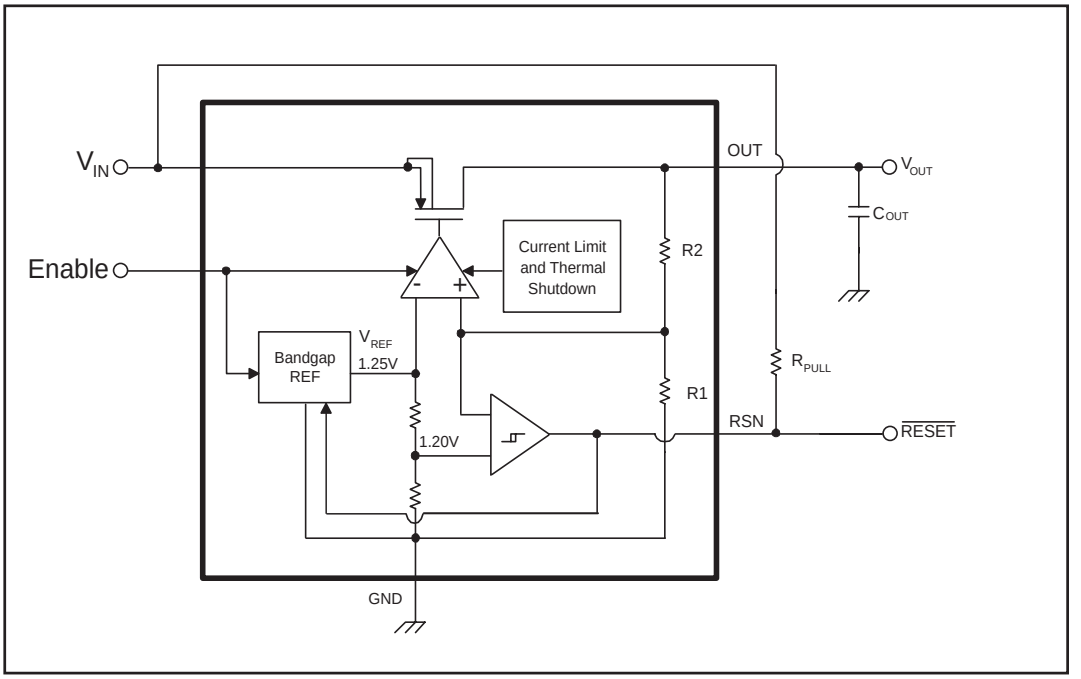


Figure 1. Fixed Voltage Regulator

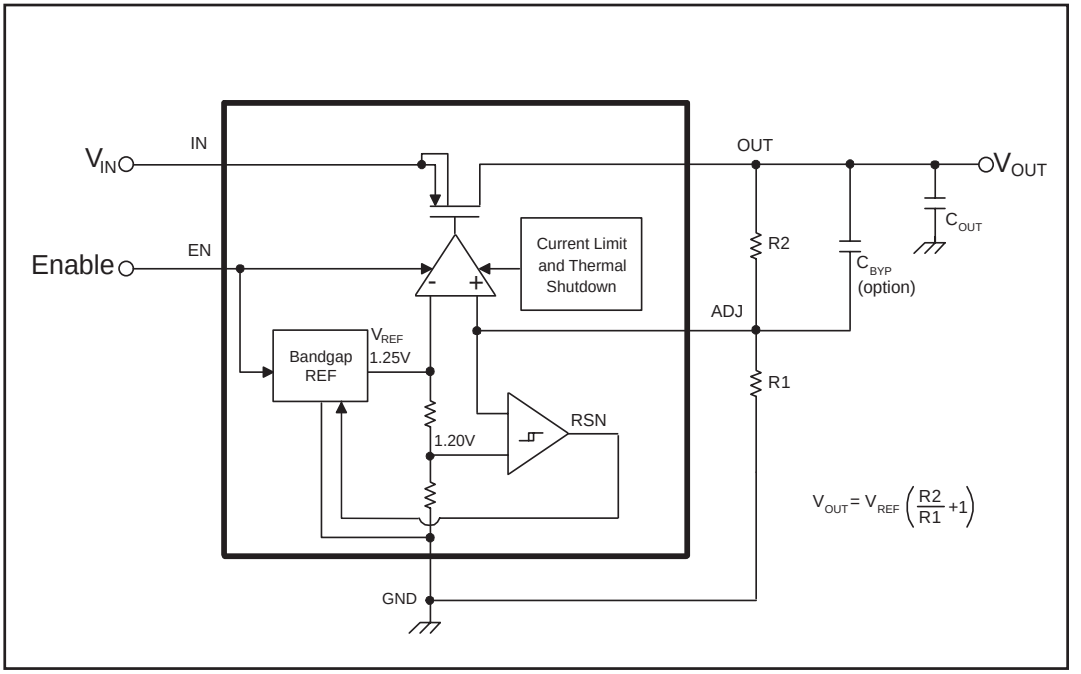


Figure 2. Adjustable Voltage Regulator

SOT 23-5 PIN CONFIGURATION		
PIN NUMBER	NAME	FUNCTION
1	IN	Supply Input
2	GND	Ground
3	EN	Enable/Shutdown (Input): CMOS or TTL compatible input. Logic high = enable, logic low = shutdown
4	RSN (Reset Not)	Open drain indicating that V_{OUT} is good
4	ADJ	Adjustable (Input): Adjustable regulator feedback input. Connect resistor voltage divider.
5	OUT	Regulator Output

8 PIN DFN PIN CONFIGURATION		
PIN NUMBER	NAME	FUNCTION
1	NC	No Connect
2	VIN	Supply Input
3	VOUT	Regulator Input
4	NC	No Connect
5 (Fixed)	RSN	Open drain indicating that V_{OUT} is good
5 (Adj.)	ADJ	Adjustable (Input): Adjustable regulator feedback input. Connect resistor voltage divider.
6	NC	No Connect
7	GND	Ground
8	EN	Enable/Shutdown (Input): CMOS or TTL compatible input. Logic high = enable, logic low = shutdown

General Overview

The SP6200 and SP6201 are CMOS LDOs designed to meet a broad range of applications that require accuracy, speed and ease of use. These LDOs offer extremely low quiescent current which only increases slightly under load, thus providing advantages in ground current performance over bipolar LDOs. The LDOs handle an extremely wide load range and guarantee stability with a 1µF ceramic output capacitor. They have excellent low frequency PSRR, not found in other CMOS LDOs and thus offer exceptional Line Regulation. High frequency PSRR is better than 40dB up to 400kHz. Load Regulation is excellent and temperature stability is comparable to bipolar LDOs. Thus, overall system accuracy is maintained under all DC and AC conditions. Enable feature is provided on all versions. A Vout good indicator (RSN pin) is provided in all the fixed output voltage devices. An adjustable output version is also available. Current Limit and Thermal protection is provided internally and is well controlled.

Architecture

The SP6200 and SP6201 are only different in their current limit threshold. The SP6200 has a current limit of 140mA, while the SP6201 current limit is 420mA. The SP6201 can provide pulsed load current of 300mA. The LDOs have a two stage amplifier which handles an extremely wide load range (10µA to 300mA) and guarantees stability with a 1µF ceramic load capacitor. The LDO amplifier has excellent gain and thus touts PSRR performance not found in other CMOS LDOs. The amplifier guarantees no overshoot on power up or while enabled through the EN pin. The amplifier also contains an active pull down, so that when the load is removed quickly the output voltage transient is minimal; thus output deviation due to load transient is small and fairly well matched when connecting and disconnecting the load.

An accurate 1.250V bandgap reference is bootstrapped to the output in fixed output versions of 2.7V and higher. This increases both the low frequency and high frequency PSRR. The adjustable version also has the bandgap reference bootstrapped to the output, thus the lowest externally programmable output voltage is 2.7V. The 2.5V fixed output version has the bandgap always connected to the Vin pin. Unlike many LDOs, the bandgap reference is not brought out for filtering by the user. This tradeoff was maid to maintain good PSRR at high frequency (PSRR can be degraded in a system due to switching noise coupling into this pin). Also, often leakages of the bypass capacitor or other components cause an error on this high impedance bandgap node. Thus, this tradeoff has been made with "ease of use" in mind.

Protection

Current limit behavior is very well controlled, providing less than 10% variation in the current limit threshold over the entire temperature range for both SP6200 and SP6201. The SP6200 has a current limit of 140mA, while the SP6201 has a current limit of 420mA. Thermal shutdown activates at 162°C and deactivates at 147°C. Thermal shutdown is very repeatable with only a 2 to 3 degree variation from device to device. Thermal shutdown changes by only 1 to 2 degrees with Vin change from 4V to 7V.

Enable (Shutdown Not) Input

The LDOs are turned off by pulling the EN pin low and turned on by pulling it high. If it is not necessary to shut down the LDO, the EN (pin 3) should be tied to IN (pin 1) to keep the regulator output on at all time. The enable threshold is 0.9V and does not change more than 100mV over the entire temperature and Vin voltage range. The lot to lot variations in Enable Threshold is also within 100mV. Shutdown current is guaranteed to be <1uA without requiring the user to pull enable all the way to 0V. Standard TTL or CMOS levels will transition the device from totally on to totally off.

Reset Not (VOUT good) Output

An accurate Vout good indicator is provided on all the fixed output version devices, pin 4 (RSN), Figure 1. This is an open drain, logic output that can be used to hold a microprocessor or microcontroller in a RESET condition when it's power supplied by Vout is 4% out of nominal regulation. A 1% hysteresis is included in the Reset Not function, so that false alarms are not issued as a result of LDO's output noise. The Reset Not function reacts in 10 to 50µs.

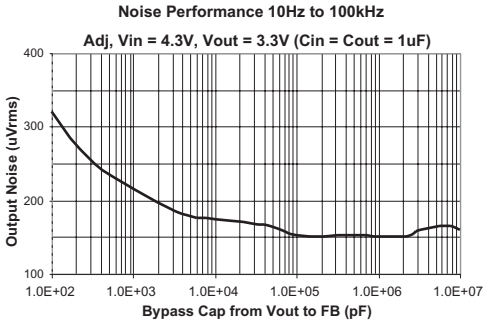
Adjustable Output Version

The adjustable version can be programmed to any voltage from 2.7V to 6V for the industrial temperature range; 2.5V to 6V for the commercial temperature range. The output can not be programmed below 2.5V due a headroom restriction. Since the bandgap is bootstrapped to the output, the output voltage must be above the minimum bandgap supply voltage. The bandgap requires 2.7V or greater at -40°C and requires 2.5V or greater at 0°C.

The regulator's output can be adjusted to a specific output voltage by using two external resistors, Figure 2. The resistor's set the output voltage based on the following equation:

$$V_{OUT} = 1.25\ (R2/R1 + 1)$$

Resistor values are not critical because the ADJ node has a high input impedance, but for best results use resistors of 470kΩ or less. A capacitor from ADJ to Vout pin provides improved noise performance as is shown in the following plot.



Input Capacitor

A small capacitor, 1µF or higher, is required from V_{IN} to GND to create a high frequency bypass for the LDO amplifier. Any ceramic or tantalum capacitor may be used at the input. Capacitor ESR (effective series resistance) should be smaller than 3Ω.

Output Capacitor

An output capacitor is required between V_{OUT} and GND to prevent oscillation. A capacitance as low as 0.22µF can fulfill stability requirements in most applications. A 1µF capacitor will ensure unconditional stability from no load to full load over the entire input voltage, output voltage and temperature range. Larger capacitor values improve the regulator's transient response. The output capacitor value may be increased without limit. The output capacitor should have an ESR (effective series resistance) below 5Ω and a resonant frequency above 1MHz.

No Load Stability

The SP6200/6201 will remain stable and in regulation with no external load (other than the internal voltage driver) unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

Thermal Considerations

The SP6200 is designed to provide 100mA of continuous current, while the SP6201 will provide 200mA of continuous current. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. To determine the maximum power dissipation in the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

$$P_D = \frac{(T_{J(max)} - T_A)}{\theta_{JA}}$$

$T_{J(max)}$ is the maximum junction temperature of the die and is 125°C. T_A is the ambient operating. θ_{JA} is the junction-to-ambient thermal resistance for the regulator and is layout dependent.

The actual power dissipation of the regulator circuit can be determined using one simple

equation:

$$P_D = (V_{IN} - V_{OUT})*I_{OUT} + V_{IN}*I_{GND}$$
$$\cong (V_{IN} - V_{OUT}) * I_{OUT}$$

Substituting $P_{D(max)}$ for P_D and solving for the operating conditions that are critical to the application will give the maximum operating conditions for the regulator circuit. For example, if we are operating the SP6201- 3.0V at room temperature, with a SOT-23-5 package on a 4 layer standard board we can determine the maximum input voltage for a set output current.

$$P_{D(max)} = \frac{(125°C - 25°C)}{(191°C/W)} = 0.52W$$

To prevent the device from entering thermal shutdown, maximum power dissipation can not be exceeded. Using the output voltage of 3.0V and an output current of 200 mA, the maximum input voltage can be determined. Ground pin current can be taken from the electrical spec's-table (I_{GND}=200uA at I_{OUT}=200mA). The maximum input voltage is determined as follows:

$$0.52W = (V_{IN} – 3.0V)*200mA + V_{IN}*0.2mA$$

Solving for V_{IN}, we get:

$$V_{IN} = \frac{(0.52W + 0.6W)}{200.2mA}$$

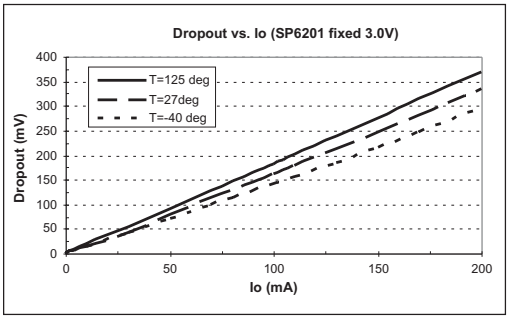
After calculations, we find that the maximum input voltage of a 3.0V application at 200mA of output current in an SOT-23-5 package is 5.59V.

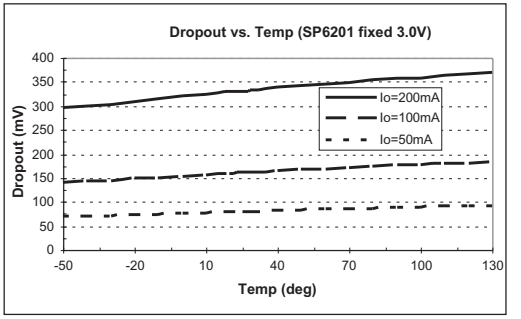
Dual-Supply Operation

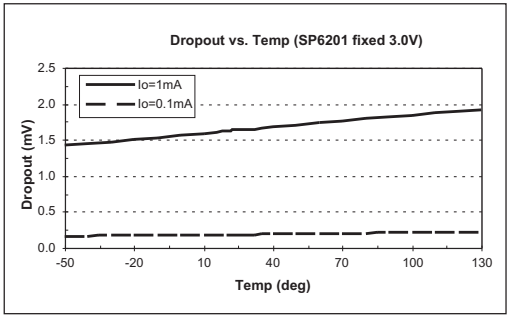
When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

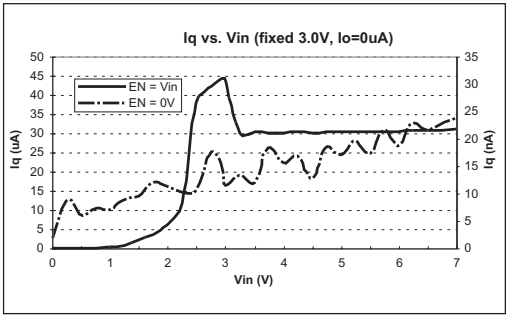
TYPICAL CHARACTERISTICS

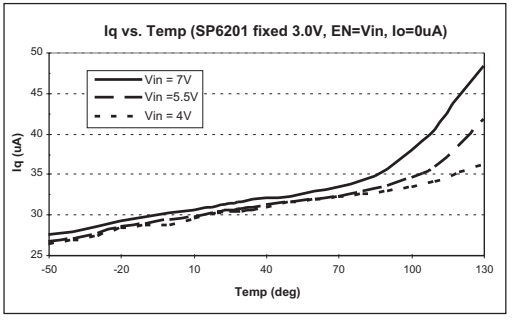
27°C, V_{IN} = 5.5V, I_O = 0.1mA, C_{IN} = C_{OUT} = 1µF unless otherwise specified.

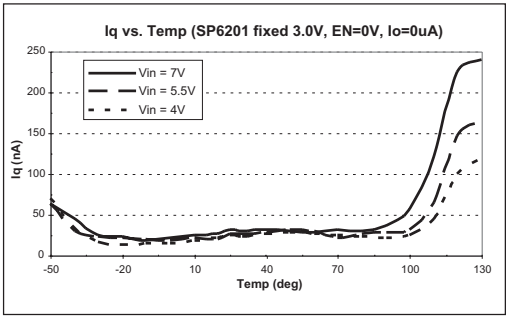


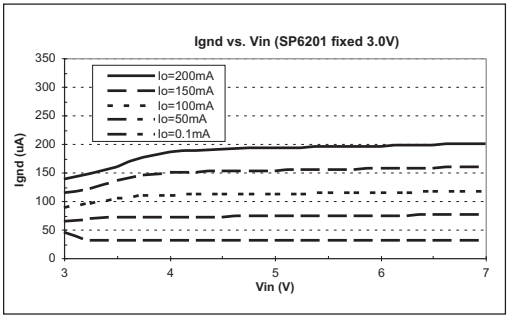


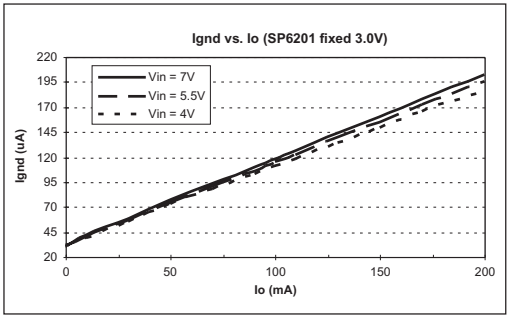












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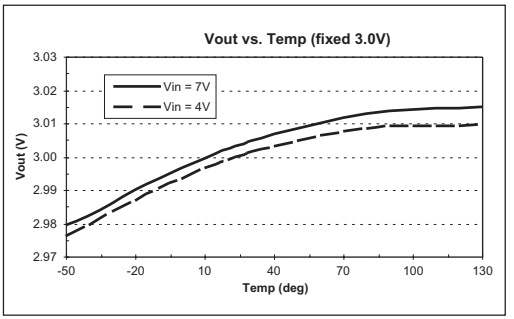

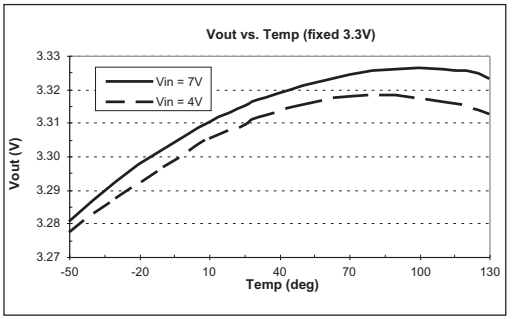

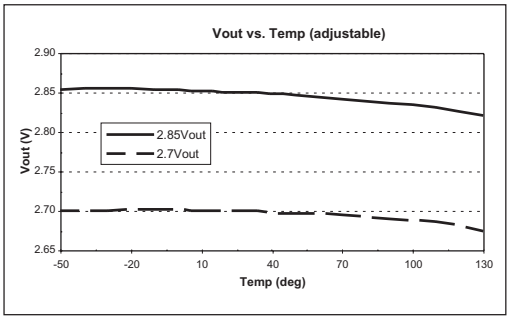

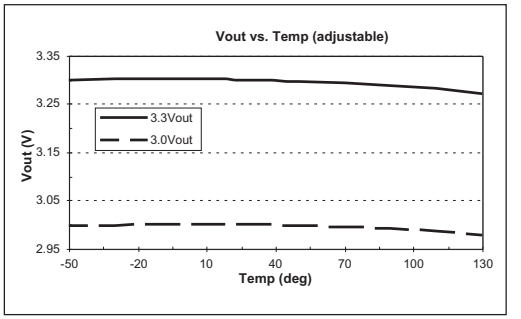

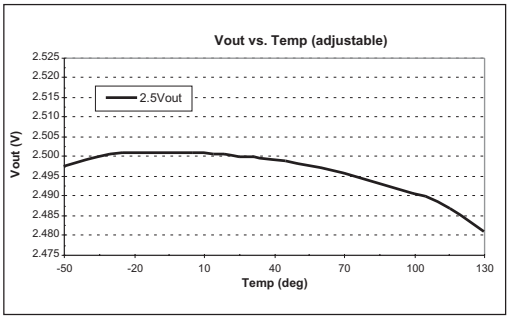

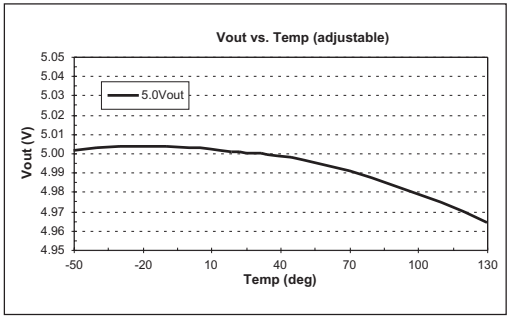

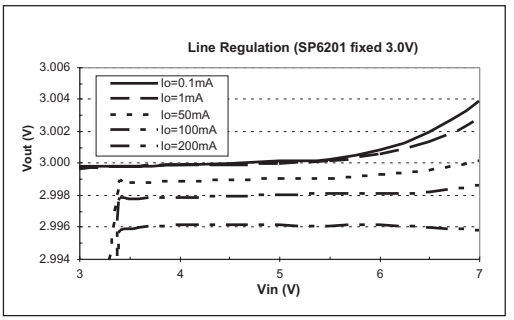

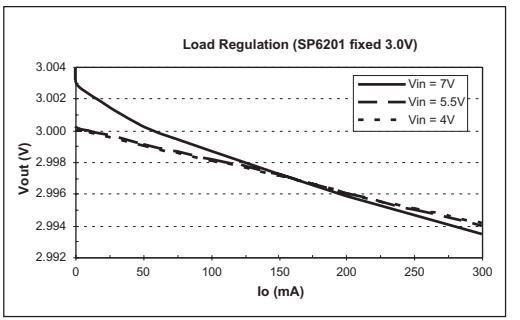

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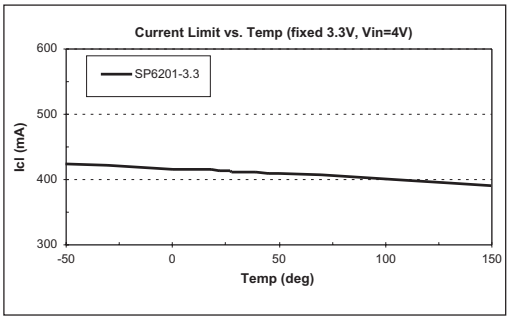
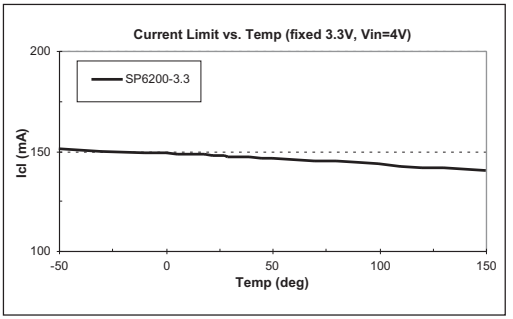
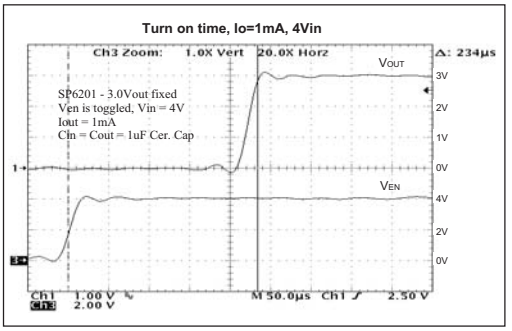
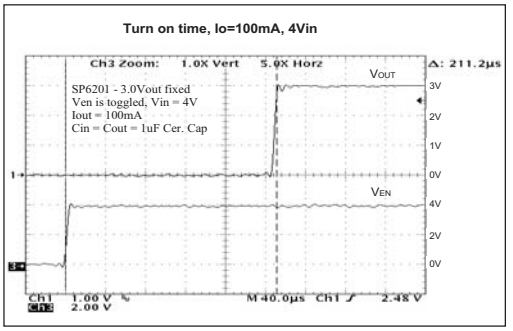
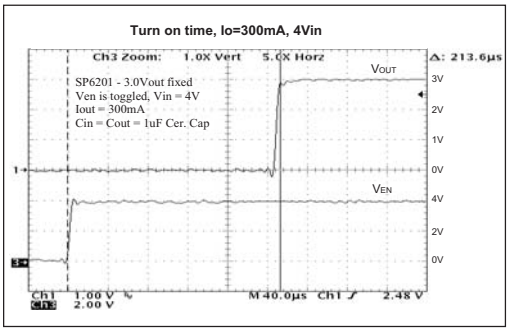
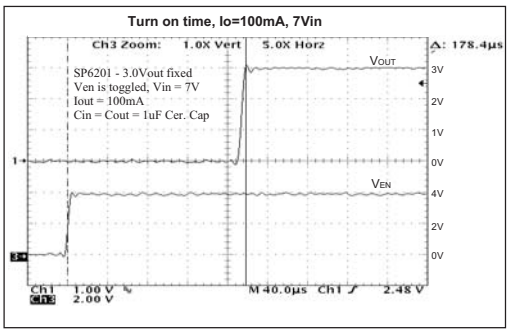


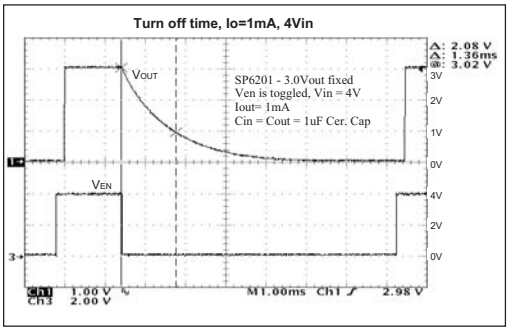


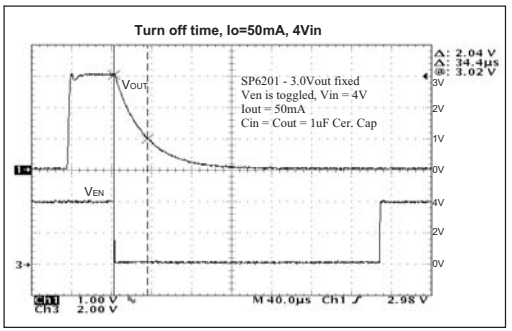




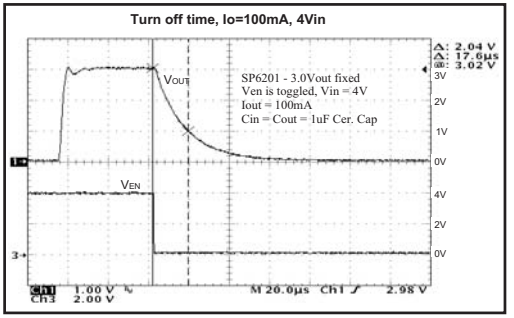


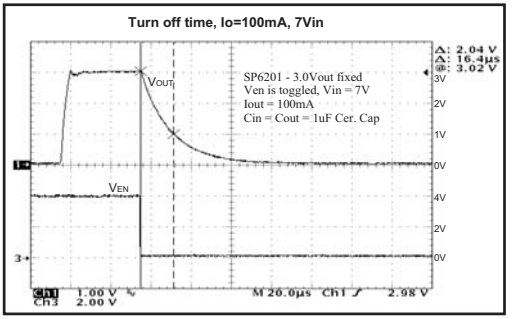


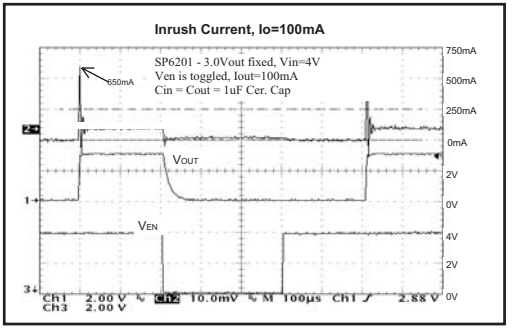


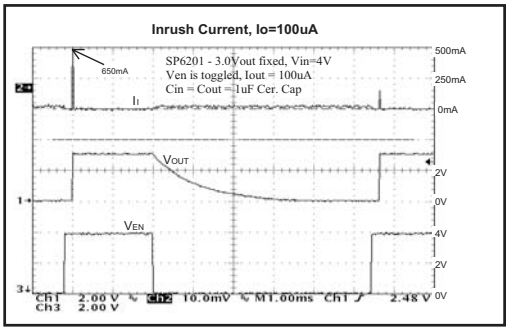


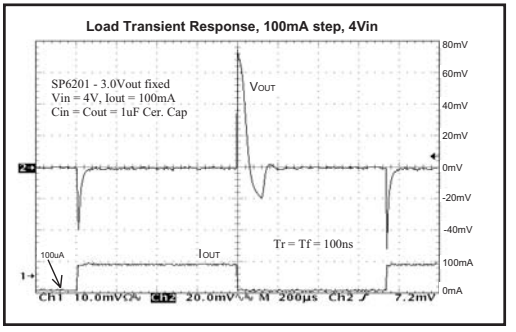
27°C, V_{IN} = 5.5V, I_O = 0.1mA, C_{IN} = C_{OUT} = 1µF unless otherwise specified.

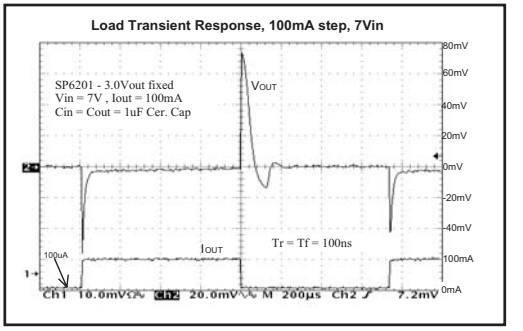


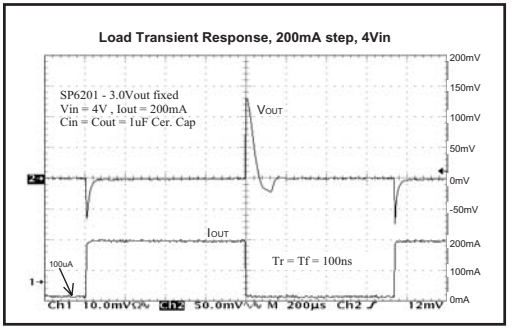


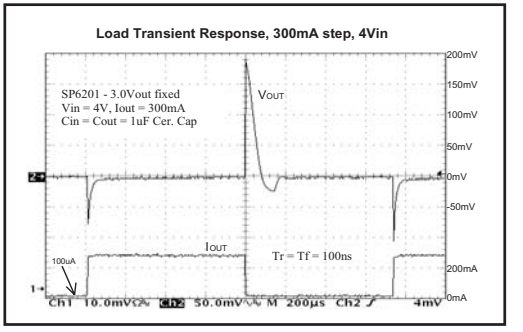




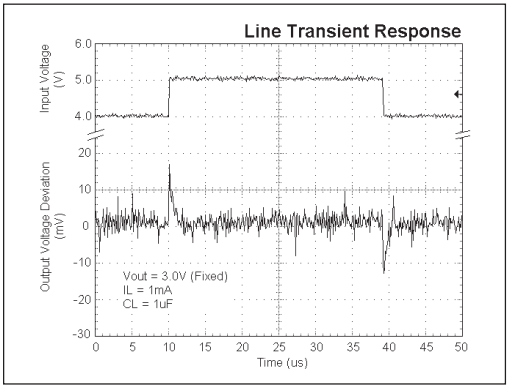


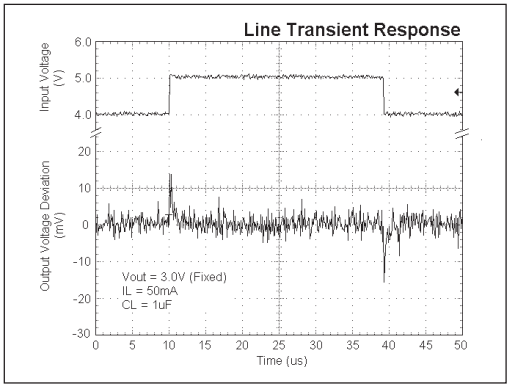


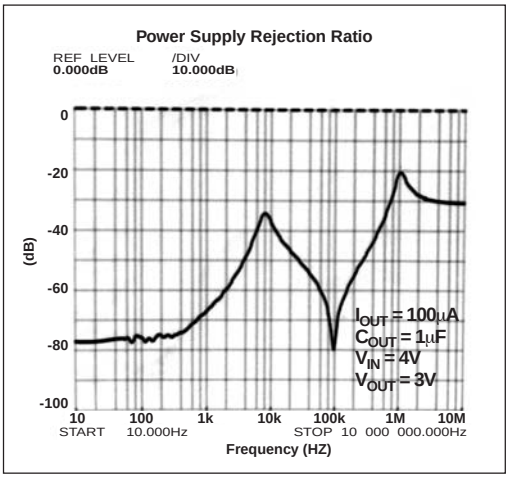


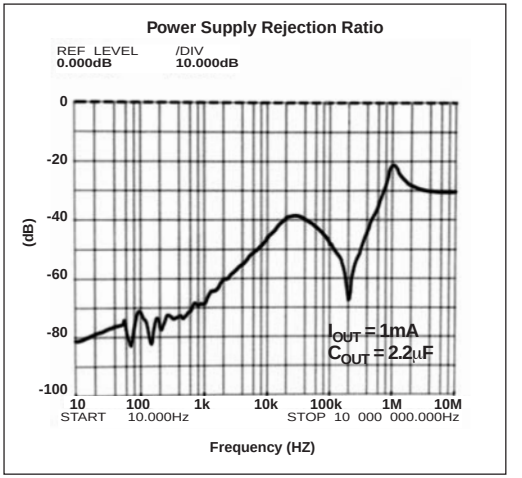


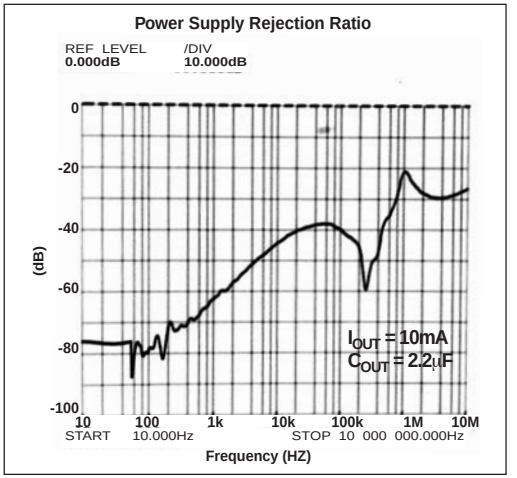
27°C, V_{IN} = 5.5V, I_O = 0.1mA, C_{IN} = C_{OUT} = 1µF unless otherwise specified.

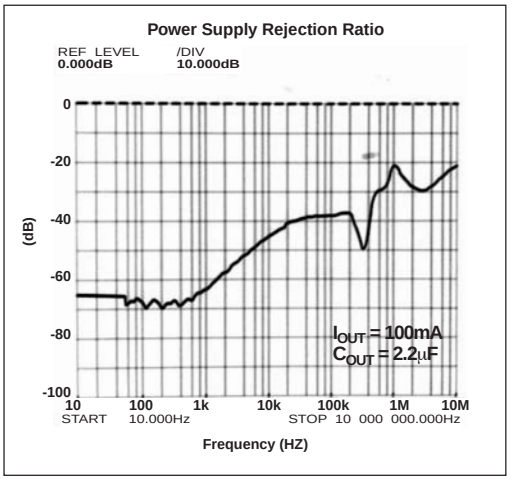


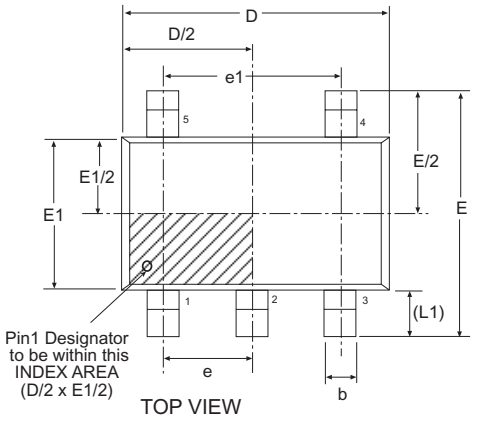


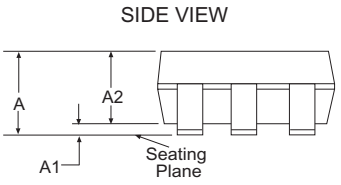


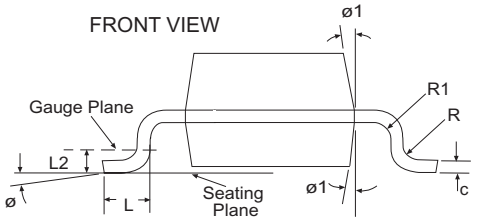




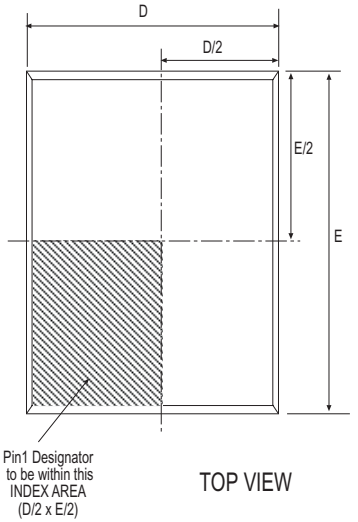




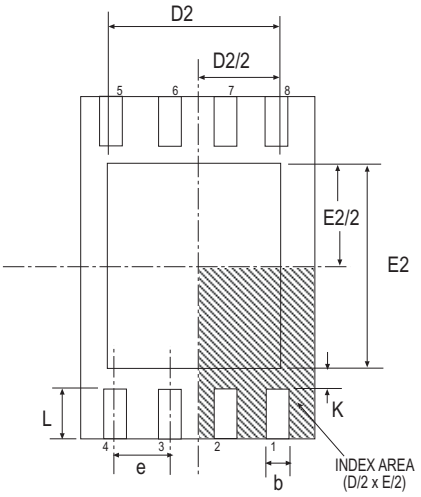




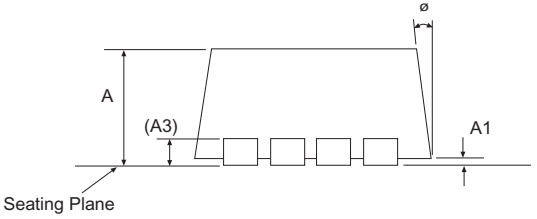
5 Pin SOT-23 JEDEC MO-178 Variation AA						
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.45	-	-	0.057
A1	0.00	-	0.15	0.000	-	0.006
A2	0.90	1.15	1.30	0.036	0.045	0.051
c	0.08	-	0.22	0.004	-	0.009
D	2.90 BSC			0.115 BSC		
E	2.80 BSC			0.111 BSC		
E1	1.60 BSC			0.063 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
R1	0.10	-	0.25	0.004	-	0.010
Ø	0º	4º	8º	0º	4º	8º
ø1	5º	10º	15º	5º	10º	15º
b	0.30	-	0.50	0.012	-	0.020
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
SIPEX Pkg Signoff Date/Rev:				JL Oct3-05 / Rev A		



TOP VIEW



BOTTOM VIEW



SIDE VIEW

2x3 8 Pin DFN	JEDEC MO-229			VARIATION VCED-2		
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.036	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
K	0.20	-	-	0.008	-	-
ø	0º	-	14º	0º	-	14º
b	0.18	0.25	0.30	0.008	0.010	0.012
D		2.00 BSC			0.079 BSC	
D2	1.50	-	1.75	0.059	-	0.069
E		3.00 BSC			0.118 BSC	
E2	1.60	-	1.90	0.063	-	0.075
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
SIPEX Pkg Signoff Date/Rev:				JL Aug18-05 / RevA		

Part Number	Top Mark	Temperature Range	Voltage Option	Package Type
SP6200EM5	EADJ	-40˚C to +125˚C	ADJ	5 Pin SOT-23
SP6200EM5/TR	EADJ	-40˚C to +125˚C	ADJ	5 Pin SOT-23
SP6200EM5-1-5	E15	-40˚C to +125˚C	1.5V	5 Pin SOT-23
SP6200EM5-1-5/TR	E15	-40˚C to +125˚C	1.5V	5 Pin SOT-23
SP6200EM5-1-8	E18	-40˚C to +125˚C	1.8V	5 Pin SOT-23
SP6200EM5-1-8/TR	E18	-40˚C to +125˚C	1.8V	5 Pin SOT-23
SP6200EM5-2-5	E25	-40˚C to +125˚C	2.5V	5 Pin SOT-23
SP6200EM5-2-5/TR	E25	-40˚C to +125˚C	2.5V	5 Pin SOT-23
SP6200EM5-2-7	E27	-40˚C to +125˚C	2.7V	5 Pin SOT-23
SP6200EM5-2-7/TR	E27	-40˚C to +125˚C	2.5V	5 Pin SOT-23
SP6200EM5-2-85	E285	-40˚C to +125˚C	2.85V	5 Pin SOT-23
SP6200EM5-2-85/TR	E285	-40˚C to +125˚C	2.85V	5 Pin SOT-23
SP6200EM5-3-0	E30	-40˚C to +125˚C	3.0V	5 Pin SOT-23
SP6200EM5-3-0/TR	E30	-40˚C to +125˚C	3.0V	5 Pin SOT-23
SP6200EM5-3-3	E33	-40˚C to +125˚C	3.3V	5 Pin SOT-23
SP6200EM5-3-3/TR	E33	-40˚C to +125˚C	3.3V	5 Pin SOT-23
SP6200EM5-3-5	E35	-40˚C to +125˚C	3.5V	5 Pin SOT-23
SP6200EM5-3-5/TR	E35	-40˚C to +125˚C	3.5V	5 Pin SOT-23
SP6200EM5-5-0	E50	-40˚C to +125˚C	5.0V	5 Pin SOT-23
SP6200EM5-5-0/TR	E50	-40˚C to +125˚C	5.0V	5 Pin SOT-23
SP6201EM5	FADJ	-40˚C to +125˚C	ADJ	5 Pin SOT-23
SP6201EM5/TR	FADJ	-40˚C to +125˚C	ADJ	5 Pin SOT-23
SP6201EM5-1-5	F15	-40˚C to +125˚C	1.5V	5 Pin SOT-23
SP6201EM5-1-5/TR	F15	-40˚C to +125˚C	1.5V	5 Pin SOT-23
SP6201EM5-1-8	F18	-40˚C to +125˚C	1.8V	5 Pin SOT-23
SP6201EM5-1-8/TR	F18	-40˚C to +125˚C	1.8V	5 Pin SOT-23
SP6201EM5-2-5	F25	-40˚C to +125˚C	2.5V	5 Pin SOT-23
SP6201EM5-2-5/TR	F25	-40˚C to +125˚C	2.5V	5 Pin SOT-23
SP6201EM5-2-7	F27	-40˚C to +125˚C	2.7V	5 Pin SOT-23
SP6201EM5-2-7/TR	F27	-40˚C to +125˚C	2.5V	5 Pin SOT-23
SP6201EM5-2-85	F285	-40˚C to +125˚C	2.85V	5 Pin SOT-23
SP6201EM5-2-85/TR	F285	-40˚C to +125˚C	2.85V	5 Pin SOT-23
SP6201EM5-3-0	F30	-40˚C to +125˚C	3.0V	5 Pin SOT-23
SP6201EM5-3-0/TR	F30	-40˚C to +125˚C	3.0V	5 Pin SOT-23
SP6201EM5-3-3	F33	-40˚C to +125˚C	3.3V	5 Pin SOT-23
SP6201EM5-3-3/TR	F33	-40˚C to +125˚C	3.3V	5 Pin SOT-23
SP6201EM5-3-5	F35	-40˚C to +125˚C	3.5V	5 Pin SOT-23
SP6201EM5-3-5/TR	F35	-40˚C to +125˚C	3.5V	5 Pin SOT-23
SP6201EM5-5-0	F50	-40˚C to +125˚C	5.0V	5 Pin SOT-23
SP6201EM5-5-0/TR	F50	-40˚C to +125˚C	5.0V	5 Pin SOT-23

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP6200EM5-1-5/TR = standard; SP6200EM5-L-1-5/TR = lead free. Lead Free SOT-23 packages can be identified by a Bar "|" to the left of the standard Top Marking.

/TR = Tape and Reel. Pack quantity is 2500 for SOT-23.

Sipex Corporation

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FAX: (408) 935-7600

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Part Number	Top Mark	Temperature Range	Voltage Option	Package Type
SP6200ER	620-0ER	-40˚C to +125˚C	ADJ	8 Pin DFN
SP6200ER/TR	620-0ER	-40˚C to +125˚C	ADJ	8 Pin DFN
SP6200ER-1-5	620-015	-40˚C to +125˚C	1.5V	8 Pin DFN
SP6200ER-1-5/TR	620-015	-40˚C to +125˚C	1.5V	8 Pin DFN
SP6200ER-1-8	620-018	-40˚C to +125˚C	1.8V	8 Pin DFN
SP6200ER-1-8/TR	620-018	-40˚C to +125˚C	1.8V	8 Pin DFN
SP6200ER-2-5	620-025	-40˚C to +125˚C	2.5V	8 Pin DFN
SP6200ER-2-5/TR	620-025	-40˚C to +125˚C	2.5V	8 Pin DFN
SP6200ER-2-7	620-027	-40˚C to +125˚C	2.7V	8 Pin DFN
SP6200ER-2-7/TR	620-027	-40˚C to +125˚C	2.5V	8 Pin DFN
SP6200ER-2-85	620-0285	-40˚C to +125˚C	2.85V	8 Pin DFN
SP6200ER-2-85/TR	620-0285	-40˚C to +125˚C	2.85V	8 Pin DFN
SP6200ER-3-0	620-030	-40˚C to +125˚C	3.0V	8 Pin DFN
SP6200ER-3-0/TR	620-030	-40˚C to +125˚C	3.0V	8 Pin DFN
SP6200ER-3-3	620-033	-40˚C to +125˚C	3.3V	8 Pin DFN
SP6200ER-3-3/TR	620-033	-40˚C to +125˚C	3.3V	8 Pin DFN
SP6200ER-3-5	620-035	-40˚C to +125˚C	3.5V	8 Pin DFN
SP6200ER-3-5/TR	620-035	-40˚C to +125˚C	3.5V	8 Pin DFN
SP6200ER-5-0	620-050	-40˚C to +125˚C	5.0V	8 Pin DFN
SP6200ER-5-0/TR	620-050	-40˚C to +125˚C	5.0V	8 Pin DFN
SP6201ER	620-1ER	-40˚C to +125˚C	ADJ	8 Pin DFN
SP6201ER/TR	620-1ER	-40˚C to +125˚C	ADJ	8 Pin DFN
SP6201ER-1-5	620-115	-40˚C to +125˚C	1.5V	8 Pin DFN
SP6201ER-1-5/TR	620-115	-40˚C to +125˚C	1.5V	8 Pin DFN
SP6201ER-1-8	620-118	-40˚C to +125˚C	1.8V	8 Pin DFN
SP6201ER-1-8/TR	620-118	-40˚C to +125˚C	1.8V	8 Pin DFN
SP6201ER-2-5	620-125	-40˚C to +125˚C	2.5V	8 Pin DFN
SP6201ER-2-5/TR	620-125	-40˚C to +125˚C	2.5V	8 Pin DFN
SP6201ER-2-7	620-127	-40˚C to +125˚C	2.7V	8 Pin DFN
SP6201ER-2-7/TR	620-127	-40˚C to +125˚C	2.5V	8 Pin DFN
SP6201ER-2-85	620-1285	-40˚C to +125˚C	2.85V	8 Pin DFN
SP6201ER-2-85/TR	620-1285	-40˚C to +125˚C	2.85V	8 Pin DFN
SP6201ER-3-0	620-130	-40˚C to +125˚C	3.0V	8 Pin DFN
SP6201ER-3-0/TR	620-130	-40˚C to +125˚C	3.0V	8 Pin DFN
SP6201ER-3-3	620-133	-40˚C to +125˚C	3.3V	8 Pin DFN
SP6201ER-3-3/TR	620-133	-40˚C to +125˚C	3.3V	8 Pin DFN
SP6201ER-3-5	620-135	-40˚C to +125˚C	3.5V	8 Pin DFN
SP6201ER-3-5/TR	620-135	-40˚C to +125˚C	3.5V	8 Pin DFN
SP6201ER-5-0	620-150	-40˚C to +125˚C	5.0V	8 Pin DFN
SP6201ER-5-0/TR	620-150	-40˚C to +125˚C	5.0V	8 Pin DFN

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP6200ER-1-5/TR = standard; SP6200ER-L-1-5/TR = lead free.

Lead Free DFN packages can be identified by a Bar "__" under the standard Top Marking.

/TR = Tape and Reel. Pack quantity is 3,000 for DFN.

Solved by Sipex

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