Virtex-5QV FPGA Packaging and Pinout Specification

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/16/10	1.0	Initial Xilinx release.
09/22/10	1.1	Removed note in “Pin Definitions,” page 11 indicating that RocketIO transceivers are not supported for Virtex-5QV FPGAs. Removed No Connect (NC) indication in Table 2-1 and in Table 8-1 for multiple device pins. Added parenthetical note describing connection for AVDD_0 and AVSS_0 on page 15 and page 106.
07/19/11	1.2	Changed document from “Advance” to “Preliminary” specification. Revised “Introduction,” page 11. Updated pin definitions and table footnotes in Table 1-1, page 11. Added footnotes and footnote references to all clock capable and global clock pins in Table 2-1. Revised super-set footprint pin names for V31 and AF30 names in Table 8-1. Updated the mass value in Table 6-1, page 80. Removed references to “ES” in Figure 9-1, page 135 and Table 9-1, page 135.
01/17/12	1.3	Removed “Preliminary Specification” from document title. Changed pin name of temperature sensing diode pins in Table 1-1, page 11 from TDP_0, TDN_0 to DXP_0, DXN_0.

Date	Version	Revision
06/08/12	1.4	Added Chapter 10, "Guidelines for Xilinx CF Package Handling and Assembly".
07/26/13	1.5	In Figure 3-1, changed pins D29, G30, C32, BA28, AU30, AY31, AV7, AP9, AU10, AW16, AY16, C15, and D15 to NC. Added XCN12020, *Virtex-4 and Virtex-5 QV FPGA CF Package Product Lid Size Change* and XCN13005, *Virtex-4 and Virtex-5 QV FPGA CF Package Assembly Location Change* to Chapter 4, "Mechanical Drawings." Updated Figure 4-1 and added Figure 4-2. Updated introductory paragraph of "Pad Land Dimensions." Removed note from Table 5-1. Corrected CF1752 package in title of Figure 5-2. Added new CF1752 package to Table 6-1 and as Figure 6-1. Removed paragraph about device capacitors from Chapter 7, "Reflow Soldering Process Guidelines." Replaced NOPAD and UNCONNECTED with UNPOPULATED and UNUSED, respectively, in second paragraph of Chapter 8, "Pin Cross-Reference for PCB Prototyping with a Commercial Part." Removed discussion about chip capacitors in "Product Handling and Inspection." Updated first paragraph in "Board Level Mounting."

Table of Contents

About This Guide

This document provides complete packaging information for the radiation-hardened Virtex®-5QV FPGA which is provided exclusively in a 1.00 mm pitch ceramic flip-chip column grid array (CF) package. The CF package is optimally designed for improved thermal cycle reliability.

Guide Contents

This document is comprised of the following chapters:

- Chapter 1, "Device Packaging Overview"

  Provides an introduction to the radiation-hardened Virtex-5QV FPGA. This chapter also includes a table with pin definitions.
- Chapter 2, "Pinout Tables"

  Provides pinout information for the Virtex-5QV FPGA.
- Chapter 3, "Pinout Diagrams"

  Provides the pinout diagrams for the Virtex-5QV FPGA in the CF1752 package.
- Chapter 4, "Mechanical Drawings"

  Provides the mechanical drawing and specifications for the Virtex-5QV FPGA in the CF1752 package.
- Chapter 5, "Recommended PCB Design Rules"

  Provides PCB design rules for the Virtex-5QV FPGA in the CF1752 package.
- Chapter 6, "Thermal Specifications"

  Provides thermal data for the Virtex-5QV FPGA packaging. It discusses Virtex-5QV FPGA power management strategy and thermal management options.
- Chapter 7, "Reflow Soldering Process Guidelines"

  Provides process guidelines for the Virtex-5QV FPGA in the CF1752 package.
- Chapter 8, "Pin Cross-Reference for PCB Prototyping with a Commercial Part,"

  Provides a pin cross-reference between a commercial version of the Virtex-5 FPGA and the Virtex-5QV FPGA. The commercial Virtex-5 FPGA can be substituted in place of the Virtex-5QV FPGA for development purposes.
- Chapter 9, "Package Marking"

  Provides a description of the marking on top of the device package.

Related Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5QV Product Overview or the Virtex-5Q Family Overview
  - The features and product selection of the Virtex-5 family are outlined in this overview.
- Virtex-5 FPGA User Guide

  This guide includes chapters on:
  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources
- Virtex-5QV FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5QV family.
- Virtex-5 FPGA RocketIO GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 TXT and FXT platforms.
- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, TXT and FXT platform.
- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, TXT and FXT platforms used for PCI Express® designs.
- Virtex-5 FPGA XtremeDSP Design Considerations

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E slice.
- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.
- Virtex-5 FPGA PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

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Chapter 1

Device Packaging Overview

Introduction

This chapter provides the pin definitions for the radiation-hardened Virtex®-5QV FPGA which is provided exclusively in a 1.00 mm pitch ceramic flip-chip column grid array (CF) packages. CF packages are optimally designed for improved thermal cycle reliability.

The device is split into 24 I/O banks to allow for flexibility in the choice of I/O standards (see UG190, *Virtex-5 FPGA User Guide*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 1-1 provides the definitions for all pin types. The CF1752 package is compatible with the FF1738 for the FX130T device. Chapter 8, "Pin Cross-Reference for PCB Prototyping with a Commercial Part" provides a super-set PCB pinout that allows the placement of both the commercial version and space grade devices.

Pin Definitions

Table 1-1 provides a description of each pin type listed in Virtex-5QV FPGA pinout tables. The "_#" suffix appended to some pin descriptions indicates the bank in which that pin resides. Pins without this suffix appended are not associated with any particular bank.

Table 1-1: **Virtex-5QV FPGA Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output	All user I/O pins are capable of differential signaling and can implement pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = [P|N]** for the positive/negative sides of the differential pair.
Multi-Function Pins		
IO_LXXY_ZZZ_#		Multi-function pins are labelled "**IO_LXXY_ZZZ_#**", where **ZZZ** represents one or more of the following functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.
Dn	Input/Output	In SelectMAP mode, D0 through D31 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained.

Table 1-1: **Virtex-5QV FPGA Pin Definitions *(Continued)***

Pin Name	Direction	Description
CC	Input/Output	These clock pins connect to Clock Capable I/Os. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. Clock capable I/Os in the center column can not drive BUFRs.
GC	Input/Output	These clock pins connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential GC pair of pins, it must be connected to the positive (P) side of the pair.
SMnP/SMnN	Input/Output	System Monitor analog inputs are not supported for this device.
VREF	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
VRN	N/A	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).
VRP	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).
Dedicated Configuration Pins (1)		
CCLK_0	Input/Output	Configuration clock. Output and input in Master mode or Input in Slave mode.
CS_B_0	Input	In SelectMAP mode, this is the active-low Chip Select signal.
D_IN_0	Input	In bit-serial modes, D_IN is the single-data input.
DONE_0	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
DOUT_BUSY_0	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. In bit-serial modes, DOUT gives preamble and configuration data to down-stream devices in a daisy chain.
HSWAPEN	Input	Enable I/O pull-ups during configuration
INIT_B_0	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred.
M0_0, M1_0, M2_0	Input	Configuration mode selection
PROGRAM_B_0	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
RDWR_B_0	Input	In SelectMAP mode, this is the active-low Write Enable signal.
TCK_0	Input	Boundary-Scan Clock
TDI_0	Input	Boundary-Scan Data Input

Table 1-1: **Virtex-5QV FPGA Pin Definitions *(Continued)***

Pin Name	Direction	Description
TDO_0	Output	Boundary-Scan Data Output
TMS_0	Input	Boundary-Scan Mode Select
DXP_0, DXN_0	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
Reserved Pins		
RSVD(4)	N/A	Reserved pin—must be tied to ground.
FLOAT(4)	N/A	Do not connect this pin to the board. Leave floating.
Other Pins		
GND	N/A	Ground.
VBATT_0	N/A	Decryptor key memory backup supply. If unused, this pin should be tied to VCC or GND.
VCCAUX	N/A	Power-supply pins for auxiliary circuits
VCCINT	N/A	Power-supply pins for the internal core logic
VCCO_#	N/A	Power-supply pins for the output drivers (per bank)
RocketIO GTX Transceiver Pins		
MGTAVCC	N/A	Power-supply pin for transceiver mixed-signal circuitry.
MGTAVCCPLL	N/A	Power-supply pin for PLL.
MGTAVTTRX	N/A	Power-supply pin for RX circuitry.
MGTAVTTRXC	N/A	Power-supply pin for the resistor calibration circuit.
MGTAVTTTX	N/A	Power-supply pin for TX circuitry.
MGTREFCLKP	Input	Positive differential reference clock.
MGTREFCLKN	Input	Negative differential reference clock (negative).
MGTRREF	Input	Precision reference resistor pin for internal calibration termination.
MGTRXP	Input	Positive differential receive port.
MGTRXN	Input	Negative differential receive port.
MGTTXP	Output	Positive differential transmit port.
MGTTXN	Output	Negative differential transmit port.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CC_CONFIG}.
2. For more information on lower capacitance pins, see UG190, *Virtex-5 FPGA User Guide*.
3. For more information on RocketIO transceiver pins, see UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.
4. Connect to ground.

Chapter 2

Pinout Tables

Table 2-1 provides pinout information for the Virtex-5QV XQR5VFX130 in the CF1752 ceramic flip-chip column grid array package. The column labeled No Connect in Table 2-1 lists the pins that are not available for this footprint.

Note: All FPGA pins having no connection (listed as UNBONDED or NC in Table 2-1 must be connected to GND for space flight compatibility. R_FUSE_0 and VFS_0 must also be connected to GND.

Table 2-1: **CF1752 Package Pinout (XQR5VFX130)**

Bank	Pin Description	Pin Number	No Connect (NC)
0	AVDD_0 (connect to VCCAUX)	Y22	
0	AVSS_0 (connect to GND)	Y21	
0	CCLK_0	AH14	
0	CS_B_0	T30	
0	D_IN_0	R15	
0	D_OUT_BUSY_0	AJ16	
0	DONE_0	R14	
0	DXN_0	AC21	
0	DXP_0	AC22	
0	HSWAPEN_0	P15	
0	INIT_B_0	T14	
0	M0_0	AH29	
0	M1_0	AH30	
0	M2_0	AJ28	
0	PROGRAM_B_0	R29	
0	R_FUSE_0	AF30	NC
0	RDWR_B_0	R30	
0	TCK_0	AG29	
0	TDI_0	AH16	
0	TDO_0	AJ15	
0	TMS_0	AH15	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
0	VBATT_0	P30	
0	VCCO_0	AG30	
0	VCCO_0	AL28	
0	VFS_0	V31	NC
0	VN_0	AB21	NC
0	VP_0	AA22	NC
0	VREFN_0	AA21	NC
0	VREFP_0	AB22	NC
1	IO_L0N_A18_1	P25	
1	IO_L0P_A19_1	N25	
1	IO_L1N_A16_1	P17	
1	IO_L1P_A17_1	P18	
1	IO_L2N_A14_D30_1	N26	
1	IO_L2P_A15_D31_1	P26	
1	IO_L3N_A12_D28_1	N16	
1	IO_L3P_A13_D29_1	M16	
1	IO_L4N_VREF_A10_D26_1	P28	
1	IO_L4P_A11_D27_1	P27	
1	IO_L5N_A8_D24_1	N14	
1	IO_L5P_A9_D25_1	N15	
1	IO_L6N_A6_D22_1	N29	
1	IO_L6P_A7_D23_1	N28	
1	IO_L7N_A4_D20_1	M13	
1	IO_L7P_A5_D21_1	M14	
1	IO_L8N_CC_A2_D18_1(1)	M29	
1	IO_L8P_CC_A3_D19_1(1)	N30	
1	IO_L9N_CC_A0_D16_1(1)	P13	
1	IO_L9P_CC_A1_D17_1(1)	N13	
1	VCCO_1	F13	
1	VCCO_1	J14	
2	IO_L0N_CC_RS0_2(1)	AK13	
2	IO_L0P_CC_RS1_2(1)	AK12	
2	IO_L1N_CC_A24_2(1)	AK30	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
2	IO_L1P_CC_A25_2(1)	AJ30	
2	IO_L2N_A22_2	AK14	
2	IO_L2P_A23_2	AK15	
2	IO_L3N_A20_2	AM29	
2	IO_L3P_A21_2	AL30	
2	IO_L4N_VREF_FOE_B_MOSI_2	AM13	
2	IO_L4P_FCS_B_2	AL14	
2	IO_L5N_CSO_B_2	AL29	
2	IO_L5P_FWE_B_2	AM28	
2	IO_L6N_D6_2	AP13	
2	IO_L6P_D7_2	AN13	
2	IO_L7N_D4_2	AK29	
2	IO_L7P_D5_2	AK28	
2	IO_L8N_D2_FS2_2	AM14	
2	IO_L8P_D3_2	AN14	
2	IO_L9N_D0_FS0_2	AJ26	
2	IO_L9P_D1_FS1_2	AK27	
2	VCCO_2	AR26	
2	VCCO_2	AV27	
3	IO_L0N_CC_GC_3(1)	J15	
3	IO_L0P_CC_GC_3(1)	J16	
3	IO_L1N_CC_GC_3(1)	L27	
3	IO_L1P_CC_GC_3(1)	M26	
3	IO_L2N_GC_VRP_3	K17	
3	IO_L2P_GC_VRN_3	J17	
3	IO_L3N_GC_3	M28	
3	IO_L3P_GC_3	M27	
3	IO_L4N_GC_VREF_3	M17	
3	IO_L4P_GC_3	L17	
3	IO_L5N_GC_3	K28	
3	IO_L5P_GC_3	L29	
3	IO_L6N_GC_3	L15	
3	IO_L6P_GC_3	L16	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
3	IO_L7N_GC_3	J30	
3	IO_L7P_GC_3	K29	
3	IO_L8N_GC_3	K15	
3	IO_L8P_GC_3	L14	
3	IO_L9N_GC_3	L30	
3	IO_L9P_GC_3	K30	
3	VCCO_3	E26	
3	VCCO_3	H27	
4	IO_L0N_GC_D14_4	AP30	
4	IO_L0P_GC_D15_4	AN30	
4	IO_L1N_GC_D12_4	AL17	
4	IO_L1P_GC_D13_4	AK17	
4	IO_L2N_GC_D10_4	AP28	
4	IO_L2P_GC_D11_4	AN29	
4	IO_L3N_GC_D8_4	AL16	
4	IO_L3P_GC_D9_4	AL15	
4	IO_L4N_GC_VREF_4	AN28	
4	IO_L4P_GC_4	AP27	
4	IO_L5N_GC_4	AM17	
4	IO_L5P_GC_4	AM16	
4	IO_L6N_GC_4	AM26	
4	IO_L6P_GC_4	AM27	
4	IO_L7N_GC_VRP_4	AN16	
4	IO_L7P_GC_VRN_4	AN15	
4	IO_L8N_CC_GC_4(1)	AL26	
4	IO_L8P_CC_GC_4(1)	AL27	
4	IO_L9N_CC_GC_4(1)	AP15	
4	IO_L9P_CC_GC_4(1)	AP16	
4	VCCO_4	AR16	
4	VCCO_4	AT13	
5	IO_L0N_5	M24	
5	IO_L0P_5	L24	
5	IO_L10N_CC_5(1)	K19	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L10P_CC_5(1)	K18	
5	IO_L11N_CC_5(1)	L26	
5	IO_L11P_CC_5(1)	K27	
5	IO_L12N_VRP_5	P20	
5	IO_L12P_VRN_5	N20	
5	IO_L13N_5	F27	
5	IO_L13P_5	G27	
5	IO_L14N_VREF_5	N19	
5	IO_L14P_5	M19	
5	IO_L15N_5	H28	
5	IO_L15P_5	G28	
5	IO_L16N_5	N18	
5	IO_L16P_5	M18	
5	IO_L17N_5	F29	
5	IO_L17P_5	G29	
5	IO_L18N_5	L19	
5	IO_L18P_5	L20	
5	IO_L19N_5	H30	
5	IO_L19P_5	H29	
5	IO_L1N_5	E17	
5	IO_L1P_5	E18	
5	IO_L2N_5	L25	
5	IO_L2P_5	K24	
5	IO_L3N_5	F17	
5	IO_L3P_5	F16	
5	IO_L4N_VREF_5	J25	
5	IO_L4P_5	K25	
5	IO_L5N_5	H16	
5	IO_L5P_5	G16	
5	IO_L6N_5	J26	
5	IO_L6P_5	H26	
5	IO_L7N_5	G17	
5	IO_L7P_5	G18	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
5	IO_L8N_CC_5(1)	J27	
5	IO_L8P_CC_5(1)	J28	
5	IO_L9N_CC_5(1)	H18	
5	IO_L9P_CC_5(1)	J18	
5	VCCO_5	B25	
5	VCCO_5	C22	
5	VCCO_5	F23	
6	IO_L0N_6	AR28	
6	IO_L0P_6	AR29	
6	IO_L10N_CC_6(1)	AM18	
6	IO_L10P_CC_6(1)	AN18	
6	IO_L11N_CC_6(1)	AP26	
6	IO_L11P_CC_6(1)	AN26	
6	IO_L12N_VRP_6	AP18	
6	IO_L12P_VRN_6	AR18	
6	IO_L13N_6	AP25	
6	IO_L13P_6	AN25	
6	IO_L14N_VREF_6	AR19	
6	IO_L14P_6	AT19	
6	IO_L15N_6	AN24	
6	IO_L15P_6	AM24	
6	IO_L16N_6	AK19	
6	IO_L16P_6	AK18	
6	IO_L17N_6	AK25	
6	IO_L17P_6	AK24	
6	IO_L18N_6	AL19	
6	IO_L18P_6	AM19	
6	IO_L19N_6	AL24	
6	IO_L19P_6	AL25	
6	IO_L1N_6	AR14	
6	IO_L1P_6	AT14	
6	IO_L2N_6	AT30	
6	IO_L2P_6	AR30	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
6	IO_L3N_6	AR15	
6	IO_L3P_6	AT15	
6	IO_L4N_VREF_6	AU29	
6	IO_L4P_6	AT29	
6	IO_L5N_6	AT16	
6	IO_L5P_6	AT17	
6	IO_L6N_6	AT27	
6	IO_L6P_6	AU28	
6	IO_L7N_6	AR17	
6	IO_L7P_6	AP17	
6	IO_L8N_CC_6(1)	AR27	
6	IO_L8P_CC_6(1)	AT26	
6	IO_L9N_CC_6(1)	AN19	
6	IO_L9P_CC_6(1)	AN20	
6	VCCO_6	AT23	
6	VCCO_6	AW24	
6	VCCO_6	AY21	
7	IO_L0N_7	M22	
7	IO_L0P_7	M23	
7	IO_L10N_CC_7(1)	E23	
7	IO_L10P_CC_7(1)	E22	
7	IO_L11N_CC_7(1)	G23	
7	IO_L11P_CC_7(1)	F24	
7	IO_L12N_VRP_7	D18	
7	IO_L12P_VRN_7	E19	
7	IO_L13N_7	H23	
7	IO_L13P_7	J23	
7	IO_L14N_VREF_7	F20	
7	IO_L14P_7	E20	
7	IO_L15N_7	H24	
7	IO_L15P_7	G24	
7	IO_L16N_7	G19	
7	IO_L16P_7	F19	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
7	IO_L17N_7	F25	
7	IO_L17P_7	F26	
7	IO_L18N_7	H20	
7	IO_L18P_7	H19	
7	IO_L19N_7	G26	
7	IO_L19P_7	H25	
7	IO_L1N_7	L21	
7	IO_L1P_7	M21	
7	IO_L2N_7	N23	
7	IO_L2P_7	N24	
7	IO_L3N_7	N21	
7	IO_L3P_7	N22	
7	IO_L4N_VREF_7	J21	
7	IO_L4P_7	H21	
7	IO_L5N_7	K20	
7	IO_L5P_7	J20	
7	IO_L6N_7	K23	
7	IO_L6P_7	L22	
7	IO_L7N_7	J22	
7	IO_L7P_7	K22	
7	IO_L8N_CC_7(1)	G22	
7	IO_L8P_CC_7(1)	F22	
7	IO_L9N_CC_7(1)	F21	
7	IO_L9P_CC_7(1)	G21	
7	VCCO_7	D19	
7	VCCO_7	G20	
7	VCCO_7	H17	
8	IO_L0N_8	AL22	
8	IO_L0P_8	AL21	
8	IO_L10N_CC_8(1)	AV20	
8	IO_L10P_CC_8(1)	AV21	
8	IO_L11N_CC_8(1)	AV25	
8	IO_L11P_CC_8(1)	AU24	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
8	IO_L12N_VRP_8	AU22	
8	IO_L12P_VRN_8	AU23	
8	IO_L13N_8	AV24	
8	IO_L13P_8	AV23	
8	IO_L14N_VREF_8	AP22	
8	IO_L14P_8	AR23	
8	IO_L15N_8	AT22	
8	IO_L15P_8	AR22	
8	IO_L16N_8	AM23	
8	IO_L16P_8	AM22	
8	IO_L17N_8	AP23	
8	IO_L17P_8	AN23	
8	IO_L18N_8	AP21	
8	IO_L18P_8	AP20	
8	IO_L19N_8	AM21	
8	IO_L19P_8	AN21	
8	IO_L1N_8	AK22	
8	IO_L1P_8	AK23	
8	IO_L2N_8	AJ21	
8	IO_L2P_8	AJ22	
8	IO_L3N_8	AL20	
8	IO_L3P_8	AK20	
8	IO_L4N_VREF_8	AU27	
8	IO_L4P_8	AU26	
8	IO_L5N_8	AU18	
8	IO_L5P_8	AU19	
8	IO_L6N_8	AT25	
8	IO_L6P_8	AR25	
8	IO_L7N_8	AT20	
8	IO_L7P_8	AR20	
8	IO_L8N_CC_8(1)	AR24	
8	IO_L8P_CC_8(1)	AT24	
8	IO_L9N_CC_8(1)	AT21	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
8	IO_L9P_CC_8[1]	AU21	
8	VCCO_8	AP19	
8	VCCO_8	AU20	
8	VCCO_8	AV17	
11	IO_L0N_11	G42	
11	IO_L0P_11	F42	
11	IO_L10N_CC_SM15N_11[1]	Y38	
11	IO_L10P_CC_SM15P_11[1]	Y39	
11	IO_L11N_CC_SM14N_11[1]	AA37	
11	IO_L11P_CC_SM14P_11[1]	Y37	
11	IO_L12N_VRP_11	P42	
11	IO_L12P_VRN_11	R42	
11	IO_L13N_11	R40	
11	IO_L13P_11	P41	
11	IO_L14N_VREF_11	T41	
11	IO_L14P_11	T40	
11	IO_L15N_SM13N_11	U41	
11	IO_L15P_SM13P_11	T42	
11	IO_L16N_SM12N_11	V41	
11	IO_L16P_SM12P_11	U42	
11	IO_L17N_SM11N_11	W41	
11	IO_L17P_SM11P_11	V40	
11	IO_L18N_SM10N_11	Y42	
11	IO_L18P_SM10P_11	W42	
11	IO_L19N_SM9N_11	AA41	
11	IO_L19P_SM9P_11	AA42	
11	IO_L1N_11	G41	
11	IO_L1P_11	F41	
11	IO_L2N_11	J41	
11	IO_L2P_11	H41	
11	IO_L3N_11	K42	
11	IO_L3P_11	J42	
11	IO_L4N_VREF_11	L41	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
11	IO_L4P_11	L40	
11	IO_L5N_11	M41	
11	IO_L5P_11	L42	
11	IO_L6N_11	N41	
11	IO_L6P_11	M42	
11	IO_L7N_11	P40	
11	IO_L7P_11	N40	
11	IO_L8N_CC_11(1)	Y40	
11	IO_L8P_CC_11(1)	W40	
11	IO_L9N_CC_11(1)	AA39	
11	IO_L9P_CC_11(1)	AA40	
11	VCCO_11	V37	
11	VCCO_11	Y41	
11	VCCO_11	AA38	
12	IO_L0N_12	AA6	
12	IO_L0P_12	AA7	
12	IO_L10N_CC_12(1)	N6	
12	IO_L10P_CC_12(1)	N5	
12	IO_L11N_CC_12(1)	U6	
12	IO_L11P_CC_12(1)	U7	
12	IO_L12N_VRP_12	P6	
12	IO_L12P_VRN_12	P5	
12	IO_L13N_12	T6	
12	IO_L13P_12	T7	
12	IO_L14N_VREF_12	R5	
12	IO_L14P_12	R4	
12	IO_L15N_12	T4	
12	IO_L15P_12	T5	
12	IO_L16N_12	AA10	
12	IO_L16P_12	AA11	
12	IO_L17N_12	Y10	
12	IO_L17P_12	AA9	
12	IO_L18N_12	W10	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L18P_12	W11	
12	IO_L19N_12	Y8	
12	IO_L19P_12	Y9	
12	IO_L1N_12	H5	
12	IO_L1P_12	G6	
12	IO_L2N_12	W6	
12	IO_L2P_12	W5	
12	IO_L3N_12	J5	
12	IO_L3P_12	H6	
12	IO_L4N_VREF_12	W7	
12	IO_L4P_12	Y7	
12	IO_L5N_12	K5	
12	IO_L5P_12	J6	
12	IO_L6N_12	V8	
12	IO_L6P_12	W8	
12	IO_L7N_12	L5	
12	IO_L7P_12	K4	
12	IO_L8N_CC_12(1)	V6	
12	IO_L8P_CC_12(1)	V5	
12	IO_L9N_CC_12(1)	M6	
12	IO_L9P_CC_12(1)	L6	
12	VCCO_12	U10	
12	VCCO_12	V7	
12	VCCO_12	AA8	
13	IO_L0N_SM8N_13	AB42	
13	IO_L0P_SM8P_13	AB41	
13	IO_L10N_CC_13(1)	AD40	
13	IO_L10P_CC_13(1)	AE40	
13	IO_L11N_CC_13(1)	AC39	
13	IO_L11P_CC_13(1)	AC40	
13	IO_L12N_VRP_13	AL40	
13	IO_L12P_VRN_13	AK40	
13	IO_L13N_13	AK42	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L13P_13	AL41	
13	IO_L14N_VREF_13	AM42	
13	IO_L14P_13	AL42	
13	IO_L15N_13	AN41	
13	IO_L15P_13	AM41	
13	IO_L16N_13	AP41	
13	IO_L16P_13	AP42	
13	IO_L17N_13	AT42	
13	IO_L17P_13	AR42	
13	IO_L18N_13	AU41	
13	IO_L18P_13	AT41	
13	IO_L19N_13	AV41	
13	IO_L19P_13	AU42	
13	IO_L1N_SM7N_13	AD42	
13	IO_L1P_SM7P_13	AC41	
13	IO_L2N_SM6N_13	AD41	
13	IO_L2P_SM6P_13	AE42	
13	IO_L3N_SM5N_13	AF42	
13	IO_L3P_SM5P_13	AF41	
13	IO_L4N_VREF_13	AG41	
13	IO_L4P_13	AF40	
13	IO_L5N_SM4N_13	AH41	
13	IO_L5P_SM4P_13	AG42	
13	IO_L6N_SM3N_13	AJ41	
13	IO_L6P_SM3P_13	AJ42	
13	IO_L7N_SM2N_13	AJ40	
13	IO_L7P_SM2P_13	AH40	
13	IO_L8N_CC_SM1N_13(1)	AB38	
13	IO_L8P_CC_SM1P_13(1)	AB37	
13	IO_L9N_CC_SM0N_13(1)	AC38	
13	IO_L9P_CC_SM0P_13(1)	AB39	
13	VCCO_13	AB35	
13	VCCO_13	AD39	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
13	VCCO_13	AE36	
15	IO_L0N_15	H39	
15	IO_L0P_15	H38	
15	IO_L10N_CC_15(1)	J40	
15	IO_L10P_CC_15(1)	H40	
15	IO_L11N_CC_15(1)	K39	
15	IO_L11P_CC_15(1)	K40	
15	IO_L12N_VRP_15	U37	
15	IO_L12P_VRN_15	V38	
15	IO_L13N_15	U38	
15	IO_L13P_15	T37	
15	IO_L14N_VREF_15	U39	
15	IO_L14P_15	T39	
15	IO_L15N_15	W38	
15	IO_L15P_15	V39	
15	IO_L16N_15	AA36	
15	IO_L16P_15	AA35	
15	IO_L17N_15	Y34	
15	IO_L17P_15	AA34	
15	IO_L18N_15	W35	
15	IO_L18P_15	Y35	
15	IO_L19N_15	W37	
15	IO_L19P_15	W36	
15	IO_L1N_15	G39	
15	IO_L1P_15	G38	
15	IO_L2N_15	F40	
15	IO_L2P_15	F39	
15	IO_L3N_15	E40	
15	IO_L3P_15	E39	
15	IO_L4N_VREF_15	R38	
15	IO_L4P_15	R39	
15	IO_L5N_15	P37	
15	IO_L5P_15	R37	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L6N_15	N38	
15	IO_L6P_15	P38	
15	IO_L7N_15	M39	
15	IO_L7P_15	N39	
15	IO_L8N_CC_15(1)	L39	
15	IO_L8P_CC_15(1)	M38	
15	IO_L9N_CC_15(1)	J38	
15	IO_L9P_CC_15(1)	K38	
15	VCCO_15	P39	
15	VCCO_15	R36	
15	VCCO_15	U40	
17	IO_L0N_17	AC34	
17	IO_L0P_17	AB34	
17	IO_L10N_CC_17(1)	AU39	
17	IO_L10P_CC_17(1)	AV40	
17	IO_L11N_CC_17(1)	AR39	
17	IO_L11P_CC_17(1)	AT39	
17	IO_L12N_VRP_17	AH39	
17	IO_L12P_VRN_17	AG39	
17	IO_L13N_17	AK39	
17	IO_L13P_17	AJ38	
17	IO_L14N_VREF_17	AK37	
17	IO_L14P_17	AK38	
17	IO_L15N_17	AH38	
17	IO_L15P_17	AJ37	
17	IO_L16N_17	AM39	
17	IO_L16P_17	AL39	
17	IO_L17N_17	AP38	
17	IO_L17P_17	AN39	
17	IO_L18N_17	AM38	
17	IO_L18P_17	AN38	
17	IO_L19N_17	AL37	
17	IO_L19P_17	AM37	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L1N_17	AB36	
17	IO_L1P_17	AC35	
17	IO_L2N_17	AD35	
17	IO_L2P_17	AC36	
17	IO_L3N_17	AD37	
17	IO_L3P_17	AD36	
17	IO_L4N_VREF_17	AD38	
17	IO_L4P_17	AE37	
17	IO_L5N_17	AE38	
17	IO_L5P_17	AE39	
17	IO_L6N_17	AG38	
17	IO_L6P_17	AF39	
17	IO_L7N_17	AF37	
17	IO_L7P_17	AG37	
17	IO_L8N_CC_17(1)	AP40	
17	IO_L8P_CC_17(1)	AN40	
17	IO_L9N_CC_17(1)	AT40	
17	IO_L9P_CC_17(1)	AR40	
17	VCCO_17	AG40	
17	VCCO_17	AH37	
17	VCCO_17	AK41	
18	IO_L0N_18	AK7	
18	IO_L0P_18	AJ7	
18	IO_L10N_CC_18(1)	AC6	
18	IO_L10P_CC_18(1)	AC5	
18	IO_L11N_CC_18(1)	AF6	
18	IO_L11P_CC_18(1)	AF5	
18	IO_L12N_VRP_18	AD7	
18	IO_L12P_VRN_18	AD6	
18	IO_L13N_18	AG7	
18	IO_L13P_18	AG6	
18	IO_L14N_VREF_18	AD5	
18	IO_L14P_18	AE5	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
18	IO_L15N_18	AE7	
18	IO_L15P_18	AF7	
18	IO_L16N_18	AE8	
18	IO_L16P_18	AD8	
18	IO_L17N_18	AF10	
18	IO_L17P_18	AF9	
18	IO_L18N_18	AE10	
18	IO_L18P_18	AE9	
18	IO_L19N_18	AF12	
18	IO_L19P_18	AF11	
18	IO_L1N_18	AC10	
18	IO_L1P_18	AB11	
18	IO_L2N_18	AK5	
18	IO_L2P_18	AL5	
18	IO_L3N_18	AB8	
18	IO_L3P_18	AB9	
18	IO_L4N_VREF_18	AJ5	
18	IO_L4P_18	AJ6	
18	IO_L5N_18	AC9	
18	IO_L5P_18	AC8	
18	IO_L6N_18	AH5	
18	IO_L6P_18	AH6	
18	IO_L7N_18	AD11	
18	IO_L7P_18	AD10	
18	IO_L8N_CC_18(1)	AH4	
18	IO_L8P_CC_18(1)	AG4	
18	IO_L9N_CC_18(1)	AB6	
18	IO_L9P_CC_18(1)	AB7	
18	VCCO_18	AD9	
18	VCCO_18	AE6	
18	VCCO_18	AG10	
19	IO_L0N_19	P35	
19	IO_L0P_19	R34	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
19	IO_L10N_CC_19[1]	T36	
19	IO_L10P_CC_19[1]	R35	
19	IO_L11N_CC_19[1]	V36	
19	IO_L11P_CC_19[1]	U36	
19	IO_L12N_VRP_19	G37	
19	IO_L12P_VRN_19	H36	
19	IO_L13N_19	G36	
19	IO_L13P_19	F36	
19	IO_L14N_VREF_19	E37	
19	IO_L14P_19	F37	
19	IO_L15N_19	D37	
19	IO_L15P_19	E38	
19	IO_L16N_19	V34	
19	IO_L16P_19	V35	
19	IO_L17N_19	W33	
19	IO_L17P_19	V33	
19	IO_L18N_19	W32	
19	IO_L18P_19	Y33	
19	IO_L19N_19	AA32	
19	IO_L19P_19	Y32	
19	IO_L1N_19	M36	
19	IO_L1P_19	N35	
19	IO_L2N_19	M37	
19	IO_L2P_19	L37	
19	IO_L3N_19	P36	
19	IO_L3P_19	N36	
19	IO_L4N_VREF_19	L35	
19	IO_L4P_19	L36	
19	IO_L5N_19	J35	
19	IO_L5P_19	K35	
19	IO_L6N_19	J36	
19	IO_L6P_19	H35	
19	IO_L7N_19	J37	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
19	IO_L7P_19	K37	
19	IO_L8N_CC_19(1)	T35	
19	IO_L8P_CC_19(1)	U34	
19	IO_L9N_CC_19(1)	U33	
19	IO_L9P_CC_19(1)	T34	
19	VCCO_19	G40	
19	VCCO_19	K41	
19	VCCO_19	L38	
20	IO_L0N_20	N8	
20	IO_L0P_20	N9	
20	IO_L10N_CC_20(1)	G8	
20	IO_L10P_CC_20(1)	G7	
20	IO_L11N_CC_20(1)	U9	
20	IO_L11P_CC_20(1)	U8	
20	IO_L12N_VRP_20	H9	
20	IO_L12P_VRN_20	H8	
20	IO_L13N_20	T11	
20	IO_L13P_20	T10	
20	IO_L14N_VREF_20	J7	
20	IO_L14P_20	J8	
20	IO_L15N_20	V11	
20	IO_L15P_20	U11	
20	IO_L16N_20	K9	
20	IO_L16P_20	K8	
20	IO_L17N_20	L7	
20	IO_L17P_20	K7	
20	IO_L18N_20	M8	
20	IO_L18P_20	M7	
20	IO_L19N_20	L9	
20	IO_L19P_20	M9	
20	IO_L1N_20	E8	
20	IO_L1P_20	E9	
20	IO_L2N_20	P8	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
20	IO_L2P_20	P7	
20	IO_L3N_20	E7	
20	IO_L3P_20	D7	
20	IO_L4N_VREF_20	R8	
20	IO_L4P_20	R7	
20	IO_L5N_20	F6	
20	IO_L5P_20	F7	
20	IO_L6N_20	T9	
20	IO_L6P_20	R9	
20	IO_L7N_20	F5	
20	IO_L7P_20	E5	
20	IO_L8N_CC_20(1)	V10	
20	IO_L8P_CC_20(1)	V9	
20	IO_L9N_CC_20(1)	G9	
20	IO_L9P_CC_20(1)	F9	
20	VCCO_20	L8	
20	VCCO_20	P9	
20	VCCO_20	R6	
21	IO_L0N_21	AB32	
21	IO_L0P_21	AB33	
21	IO_L10N_CC_21(1)	AG34	
21	IO_L10P_CC_21(1)	AH34	
21	IO_L11N_CC_21(1)	AG36	
21	IO_L11P_CC_21(1)	AH35	
21	IO_L12N_VRP_21	AP36	
21	IO_L12P_VRN_21	AP37	
21	IO_L13N_21	AN36	
21	IO_L13P_21	AP35	
21	IO_L14N_VREF_21	AN35	
21	IO_L14P_21	AM36	
21	IO_L15N_21	AM34	
21	IO_L15P_21	AN34	
21	IO_L16N_21	AJ36	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L16P_21	AH36	
21	IO_L17N_21	AK35	
21	IO_L17P_21	AJ35	
21	IO_L18N_21	AL35	
21	IO_L18P_21	AL36	
21	IO_L19N_21	AK34	
21	IO_L19P_21	AL34	
21	IO_L1N_21	AD32	
21	IO_L1P_21	AC33	
21	IO_L2N_21	AE32	
21	IO_L2P_21	AD33	
21	IO_L3N_21	AE34	
21	IO_L3P_21	AE33	
21	IO_L4N_VREF_21	AV38	
21	IO_L4P_21	AV39	
21	IO_L5N_21	AU37	
21	IO_L5P_21	AU38	
21	IO_L6N_21	AR38	
21	IO_L6P_21	AT37	
21	IO_L7N_21	AT36	
21	IO_L7P_21	AR37	
21	IO_L8N_CC_21(1)	AF34	
21	IO_L8P_CC_21(1)	AE35	
21	IO_L9N_CC_21(1)	AF36	
21	IO_L9P_CC_21(1)	AF35	
21	VCCO_21	AJ34	
21	VCCO_21	AL38	
21	VCCO_21	AM35	
23	IO_L0N_23	N34	
23	IO_L0P_23	N33	
23	IO_L10N_CC_23(1)	F32	
23	IO_L10P_CC_23(1)	F31	
23	IO_L11N_CC_23(1)	E33	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L11P_CC_23[1]	E32	
23	IO_L12N_VRP_23	K34	
23	IO_L12P_VRN_23	L34	
23	IO_L13N_23	J33	
23	IO_L13P_23	K33	
23	IO_L14N_VREF_23	J32	
23	IO_L14P_23	K32	
23	IO_L15N_23	L31	
23	IO_L15P_23	L32	
23	IO_L16N_23	P32	
23	IO_L16P_23	P33	
23	IO_L17N_23	R32	
23	IO_L17P_23	R33	
23	IO_L18N_23	U32	
23	IO_L18P_23	T32	
23	IO_L19N_23	T31	
23	IO_L19P_23	U31	
23	IO_L1N_23	M33	
23	IO_L1P_23	M34	
23	IO_L2N_23	M31	
23	IO_L2P_23	M32	
23	IO_L3N_23	P31	
23	IO_L3P_23	N31	
23	IO_L4N_VREF_23	G34	
23	IO_L4P_23	H34	
23	IO_L5N_23	H33	
23	IO_L5P_23	G33	
23	IO_L6N_23	G31	
23	IO_L6P_23	G32	
23	IO_L7N_23	J31	
23	IO_L7P_23	H31	
23	IO_L8N_CC_23[1]	E35	
23	IO_L8P_CC_23[1]	F35	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L9N_CC_23(1)	F34	
23	IO_L9P_CC_23(1)	E34	
23	VCCO_23	D39	
23	VCCO_23	E36	
23	VCCO_23	H37	
24	IO_L0N_24	H11	
24	IO_L0P_24	J12	
24	IO_L10N_CC_24(1)	L11	
24	IO_L10P_CC_24(1)	L12	
24	IO_L11N_CC_24(1)	G14	
24	IO_L11P_CC_24(1)	G13	
24	IO_L12N_VRP_24	M12	
24	IO_L12P_VRN_24	M11	
24	IO_L13N_24	E13	
24	IO_L13P_24	F14	
24	IO_L14N_VREF_24	P12	
24	IO_L14P_24	N11	
24	IO_L15N_24	D12	
24	IO_L15P_24	E12	
24	IO_L16N_24	N10	
24	IO_L16P_24	P11	
24	IO_L17N_24	E14	
24	IO_L17P_24	D13	
24	IO_L18N_24	P10	
24	IO_L18P_24	R10	
24	IO_L19N_24	F15	
24	IO_L19P_24	E15	
24	IO_L1N_24	G11	
24	IO_L1P_24	G12	
24	IO_L2N_24	F11	
24	IO_L2P_24	F12	
24	IO_L3N_24	F10	
24	IO_L3P_24	E10	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L4N_VREF_24	K13	
24	IO_L4P_24	K14	
24	IO_L5N_24	J11	
24	IO_L5P_24	K12	
24	IO_L6N_24	H13	
24	IO_L6P_24	J13	
24	IO_L7N_24	J10	
24	IO_L7P_24	H10	
24	IO_L8N_CC_24(1)	H15	
24	IO_L8P_CC_24(1)	H14	
24	IO_L9N_CC_24(1)	L10	
24	IO_L9P_CC_24(1)	K10	
24	VCCO_24	E6	
24	VCCO_24	G10	
24	VCCO_24	H7	
25	IO_L0N_25	AF31	
25	IO_L0P_25	AG31	
25	IO_L10N_CC_25(1)	AU31	
25	IO_L10P_CC_25(1)	AV31	
25	IO_L11N_CC_25(1)	AT31	
25	IO_L11P_CC_25(1)	AT32	
25	IO_L12N_VRP_25	AN31	
25	IO_L12P_VRN_25	AP31	
25	IO_L13N_25	AP32	
25	IO_L13P_25	AR32	
25	IO_L14N_VREF_25	AP33	
25	IO_L14P_25	AR33	
25	IO_L15N_25	AM33	
25	IO_L15P_25	AN33	
25	IO_L16N_25	AJ33	
25	IO_L16P_25	AK33	
25	IO_L17N_25	AK32	
25	IO_L17P_25	AJ32	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L18N_25	AM32	
25	IO_L18P_25	AL32	
25	IO_L19N_25	AM31	
25	IO_L19P_25	AL31	
25	IO_L1N_25	AG33	
25	IO_L1P_25	AF32	
25	IO_L2N_25	AG32	
25	IO_L2P_25	AH33	
25	IO_L3N_25	AJ31	
25	IO_L3P_25	AH31	
25	IO_L4N_VREF_25	AV36	
25	IO_L4P_25	AV35	
25	IO_L5N_25	AT35	
25	IO_L5P_25	AU36	
25	IO_L6N_25	AT34	
25	IO_L6P_25	AU34	
25	IO_L7N_25	AR34	
25	IO_L7P_25	AR35	
25	IO_L8N_CC_25(1)	AU33	
25	IO_L8P_CC_25(1)	AU32	
25	IO_L9N_CC_25(1)	AV34	
25	IO_L9P_CC_25(1)	AV33	
25	VCCO_25	AP39	
25	VCCO_25	AR36	
25	VCCO_25	AU40	
26	IO_L0N_26	AR7	
26	IO_L0P_26	AT7	
26	IO_L10N_CC_26(1)	AJ8	
26	IO_L10P_CC_26(1)	AK8	
26	IO_L11N_CC_26(1)	AP8	
26	IO_L11P_CC_26(1)	AN8	
26	IO_L12N_VRP_26	AK10	
26	IO_L12P_VRN_26	AK9	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L13N_26	AR8	
26	IO_L13P_26	AP7	
26	IO_L14N_VREF_26	AL10	
26	IO_L14P_26	AL9	
26	IO_L15N_26	AP5	
26	IO_L15P_26	AP6	
26	IO_L16N_26	AL7	
26	IO_L16P_26	AL6	
26	IO_L17N_26	AN5	
26	IO_L17P_26	AN4	
26	IO_L18N_26	AM6	
26	IO_L18P_26	AN6	
26	IO_L19N_26	AM8	
26	IO_L19P_26	AM7	
26	IO_L1N_26	AG11	
26	IO_L1P_26	AG12	
26	IO_L2N_26	AR5	
26	IO_L2P_26	AT6	
26	IO_L3N_26	AH9	
26	IO_L3P_26	AG9	
26	IO_L4N_VREF_26	AU6	
26	IO_L4P_26	AT5	
26	IO_L5N_26	AH11	
26	IO_L5P_26	AH10	
26	IO_L6N_26	AV5	
26	IO_L6P_26	AV6	
26	IO_L7N_26	AJ10	
26	IO_L7P_26	AJ11	
26	IO_L8N_CC_26(1)	AN9	
26	IO_L8P_CC_26(1)	AM9	
26	IO_L9N_CC_26(1)	AH8	
26	IO_L9P_CC_26(1)	AG8	
26	VCCO_26	AH7	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
26	VCCO_26	AK11	
26	VCCO_26	AL8	
27	IO_L0N_27	C31	
27	IO_L0P_27	D31	
27	IO_L10N_CC_27(1)	A36	
27	IO_L10P_CC_27(1)	A37	
27	IO_L11N_CC_27(1)	B36	
27	IO_L11P_CC_27(1)	B37	
27	IO_L12N_VRP_27	D38	
27	IO_L12P_VRN_27	C38	
27	IO_L13N_27	C40	
27	IO_L13P_27	C39	
27	IO_L14N_VREF_27	B38	
27	IO_L14P_27	B39	
27	IO_L15N_27	A40	
27	IO_L15P_27	A39	
27	IO_L16N_27	B41	
27	IO_L17N_27	C41	
27	IO_L18N_27	D41	
27	IO_L18P_27	D40	
27	IO_L19N_27	D42	
27	IO_L19P_27	E42	
27	IO_L1N_27	B31	
27	IO_L1P_27	C30	
27	IO_L2N_27	A31	
27	IO_L2P_27	A30	
27	IO_L3N_27	B32	
27	IO_L3P_27	A32	
27	IO_L4N_VREF_27	C33	
27	IO_L4P_27	B33	
27	IO_L5N_27	D33	
27	IO_L5P_27	D32	
27	IO_L6N_27	B34	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L6P_27	C34	
27	IO_L7N_27	A35	
27	IO_L7P_27	A34	
27	IO_L8N_CC_27(1)	D36	
27	IO_L8P_CC_27(1)	D35	
27	IO_L9N_CC_27(1)	C35	
27	IO_L9P_CC_27(1)	C36	
27	VCCO_27	B35	
27	VCCO_27	F33	
27	VCCO_27	J34	
29	IO_L0N_29	AW42	
29	IO_L0P_29	AY42	
29	IO_L10N_CC_29(1)	BA36	
29	IO_L10P_CC_29(1)	BB36	
29	IO_L11N_CC_29(1)	AW35	
29	IO_L11P_CC_29(1)	AY35	
29	IO_L12N_VRP_29	BA35	
29	IO_L12P_VRN_29	BB34	
29	IO_L13N_29	BA34	
29	IO_L13P_29	BB33	
29	IO_L14N_VREF_29	AY34	
29	IO_L14P_29	AY33	
29	IO_L15N_29	AW32	
29	IO_L15P_29	AW33	
29	IO_L16N_29	BA32	
29	IO_L16P_29	AY32	
29	IO_L17N_29	BB31	
29	IO_L17P_29	BB32	
29	IO_L18N_29	BA31	
29	IO_L18P_29	BA30	
29	IO_L19N_29	AW31	
29	IO_L19P_29	AY30	
29	IO_L1N_29	AW40	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
29	IO_L1P_29	AW41	
29	IO_L2N_29	BA41	
29	IO_L2P_29	AY40	
29	IO_L4N_VREF_29	BB39	
29	IO_L4P_29	BA40	
29	IO_L5N_29	BA39	
29	IO_L5P_29	BB38	
29	IO_L6N_29	AW37	
29	IO_L6P_29	AY38	
29	IO_L7N_29	AY39	
29	IO_L7P_29	AW38	
29	IO_L8N_CC_29(1)	BA37	
29	IO_L8P_CC_29(1)	BB37	
29	IO_L9N_CC_29(1)	AW36	
29	IO_L9P_CC_29(1)	AY37	
29	VCCO_29	AT33	
29	VCCO_29	AV37	
29	VCCO_29	AW34	
NA	MGTAVCC_112	W3	
NA	MGTAVCC_112	W4	
NA	MGTAVCC_114	AE3	
NA	MGTAVCC_114	AE4	
NA	MGTAVCC_116	N3	
NA	MGTAVCC_116	N4	
NA	MGTAVCC_118	AL3	
NA	MGTAVCC_118	AL4	
NA	MGTAVCC_120	G3	
NA	MGTAVCC_120	G4	
NA	MGTAVCC_122	AU3	
NA	MGTAVCC_122	AU4	
NA	MGTAVCC_124	D4	
NA	MGTAVCC_124	D5	
NA	MGTAVCC_126	AW5	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCC_126	AY3	
NA	MGTAVCC_128	C9	
NA	MGTAVCC_128	D9	
NA	MGTAVCC_130	AW10	
NA	MGTAVCC_130	AY10	
NA	MGTAVCC_132	C15	NC
NA	MGTAVCC_132	D15	NC
NA	MGTAVCC_134	AW16	NC
NA	MGTAVCC_134	AY16	NC
NA	MGTAVCCPLL_112	Y3	
NA	MGTAVCCPLL_114	AF3	
NA	MGTAVCCPLL_116	P3	
NA	MGTAVCCPLL_118	AM3	
NA	MGTAVCCPLL_120	H3	
NA	MGTAVCCPLL_122	AV3	
NA	MGTAVCCPLL_124	C2	
NA	MGTAVCCPLL_126	AY5	
NA	MGTAVCCPLL_128	C8	
NA	MGTAVCCPLL_130	AY11	
NA	MGTAVTTRX_112	U3	
NA	MGTAVTTRX_114	AC3	
NA	MGTAVTTRX_116	L3	
NA	MGTAVTTRX_118	AJ3	
NA	MGTAVTTRX_120	E3	
NA	MGTAVTTRX_122	AR3	
NA	MGTAVTTRX_124	C5	
NA	MGTAVTTRX_126	AY2	
NA	MGTAVTTRX_128	C11	
NA	MGTAVTTRX_130	AY8	
NA	MGTAVTTRXC	AA5	
NA	MGTAVTTTX_112	T3	
NA	MGTAVTTTX_112	AA3	
NA	MGTAVTTTX_114	AB3	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTTTX_114	AG3	
NA	MGTAVTTTX_116	K3	
NA	MGTAVTTTX_116	R3	
NA	MGTAVTTTX_118	AH3	
NA	MGTAVTTTX_118	AN3	
NA	MGTAVTTTX_120	D3	
NA	MGTAVTTTX_120	J3	
NA	MGTAVTTTX_122	AP3	
NA	MGTAVTTTX_122	AW3	
NA	MGTAVTTTX_124	C1	
NA	MGTAVTTTX_124	C6	
NA	MGTAVTTTX_126	AY1	
NA	MGTAVTTTX_126	AY6	
NA	MGTAVTTTX_128	C7	
NA	MGTAVTTTX_128	C12	
NA	MGTAVTTTX_130	AY7	
NA	MGTAVTTTX_130	AY12	
NA	MGTREFCLKN_112	V3	
NA	MGTREFCLKN_114	AD3	
NA	MGTREFCLKN_116	M3	
NA	MGTREFCLKN_118	AK3	
NA	MGTREFCLKN_120	F3	
NA	MGTREFCLKN_122	AT3	
NA	MGTREFCLKN_124	C3	
NA	MGTREFCLKN_126	AY4	
NA	MGTREFCLKN_128	C10	
NA	MGTREFCLKN_130	AY9	
NA	MGTREFCLKP_112	V4	
NA	MGTREFCLKP_114	AD4	
NA	MGTREFCLKP_116	M4	
NA	MGTREFCLKP_118	AK4	
NA	MGTREFCLKP_120	F4	
NA	MGTREFCLKP_122	AT4	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTREFCLKP_124	C4	
NA	MGTREFCLKP_126	AW4	
NA	MGTREFCLKP_128	D10	
NA	MGTREFCLKP_130	AW9	
NA	MGTRREF_112	AB4	
NA	MGTRXN0_112	V1	
NA	MGTRXN0_114	AD1	
NA	MGTRXN0_116	M1	
NA	MGTRXN0_118	AK1	
NA	MGTRXN0_120	F1	
NA	MGTRXN0_122	AT1	
NA	MGTRXN0_124	A4	
NA	MGTRXN0_126	BB3	NC
NA	MGTRXN0_128	A10	
NA	MGTRXN0_130	BB9	
NA	MGTRXN1_112	W1	
NA	MGTRXN1_114	AE1	
NA	MGTRXN1_116	N1	
NA	MGTRXN1_118	AL1	
NA	MGTRXN1_120	G1	
NA	MGTRXN1_122	AU1	
NA	MGTRXN1_124	A3	NC
NA	MGTRXN1_126	BB4	
NA	MGTRXN1_128	A9	
NA	MGTRXN1_130	BB10	
NA	MGTRXP0_112	U1	
NA	MGTRXP0_114	AC1	
NA	MGTRXP0_116	L1	
NA	MGTRXP0_118	AJ1	
NA	MGTRXP0_120	E1	
NA	MGTRXP0_122	AR1	
NA	MGTRXP0_124	A5	
NA	MGTRXP0_128	A11	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTRXP0_130	BB8	
NA	MGTRXP1_112	Y1	
NA	MGTRXP1_114	AF1	
NA	MGTRXP1_116	P1	
NA	MGTRXP1_118	AM1	
NA	MGTRXP1_120	H1	
NA	MGTRXP1_122	AV1	
NA	MGTRXP1_126	BB5	
NA	MGTRXP1_128	A8	
NA	MGTRXP1_130	BB11	
NA	MGTTXN0_112	U2	
NA	MGTTXN0_114	AC2	
NA	MGTTXN0_116	L2	
NA	MGTTXN0_118	AJ2	
NA	MGTTXN0_120	E2	
NA	MGTTXN0_122	AR2	
NA	MGTTXN0_124	B5	
NA	MGTTXN0_126	BA2	NC
NA	MGTTXN0_128	B11	
NA	MGTTXN0_130	BA8	
NA	MGTTXN1_112	Y2	
NA	MGTTXN1_114	AF2	
NA	MGTTXN1_116	P2	
NA	MGTTXN1_118	AM2	
NA	MGTTXN1_120	H2	
NA	MGTTXN1_122	AV2	
NA	MGTTXN1_124	B2	NC
NA	MGTTXN1_126	BA5	
NA	MGTTXN1_128	B8	
NA	MGTTXN1_130	BA11	
NA	MGTTXP0_112	T2	
NA	MGTTXP0_114	AB2	
NA	MGTTXP0_116	K2	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTTXP0_118	AH2	
NA	MGTTXP0_120	D2	
NA	MGTTXP0_122	AP2	
NA	MGTTXP0_124	B6	
NA	MGTTXP0_128	B12	
NA	MGTTXP0_130	BA7	
NA	MGTTXP1_112	AA2	
NA	MGTTXP1_114	AG2	
NA	MGTTXP1_116	R2	
NA	MGTTXP1_118	AN2	
NA	MGTTXP1_120	J2	
NA	MGTTXP1_122	AW2	
NA	MGTTXP1_126	BA6	
NA	MGTTXP1_128	B7	
NA	MGTTXP1_130	BA12	
NA	GND	A6	
NA	GND	A7	
NA	GND	A12	
NA	GND	A13	
NA	GND	A18	
NA	GND	A19	
NA	GND	A23	
NA	GND	A28	
NA	GND	A33	
NA	GND	A38	
NA	GND	B3	
NA	GND	B4	
NA	GND	B9	
NA	GND	B10	
NA	GND	B15	
NA	GND	B16	
NA	GND	B19	
NA	GND	B20	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B30	
NA	GND	B40	
NA	GND	C19	
NA	GND	C27	
NA	GND	C37	
NA	GND	C42	
NA	GND	D1	
NA	GND	D6	
NA	GND	D8	
NA	GND	D11	
NA	GND	D14	
NA	GND	D17	
NA	GND	D24	
NA	GND	D34	
NA	GND	E4	
NA	GND	E11	
NA	GND	E16	
NA	GND	E21	
NA	GND	E31	
NA	GND	E41	
NA	GND	F2	
NA	GND	F8	
NA	GND	F18	
NA	GND	F28	
NA	GND	F38	
NA	GND	G2	
NA	GND	G5	
NA	GND	G15	
NA	GND	G25	
NA	GND	G35	
NA	GND	H4	
NA	GND	H12	
NA	GND	H22	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	H32	
NA	GND	H42	
NA	GND	J1	
NA	GND	J4	
NA	GND	J9	
NA	GND	J19	
NA	GND	J24	
NA	GND	J29	
NA	GND	J39	
NA	GND	K1	
NA	GND	K6	
NA	GND	K11	
NA	GND	K16	
NA	GND	K21	
NA	GND	K26	
NA	GND	K31	
NA	GND	K36	
NA	GND	L4	
NA	GND	L13	
NA	GND	L18	
NA	GND	L23	
NA	GND	L28	
NA	GND	L33	
NA	GND	M2	
NA	GND	M5	
NA	GND	M10	
NA	GND	M15	
NA	GND	M20	
NA	GND	M25	
NA	GND	M30	
NA	GND	M35	
NA	GND	M40	
NA	GND	N2	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	N7	
NA	GND	N12	
NA	GND	N17	
NA	GND	N27	
NA	GND	N32	
NA	GND	N37	
NA	GND	N42	
NA	GND	P4	
NA	GND	P14	
NA	GND	P16	
NA	GND	P19	
NA	GND	P22	
NA	GND	P24	
NA	GND	P29	
NA	GND	P34	
NA	GND	R1	
NA	GND	R11	
NA	GND	R13	
NA	GND	R17	
NA	GND	R19	
NA	GND	R21	
NA	GND	R23	
NA	GND	R25	
NA	GND	R27	
NA	GND	R31	
NA	GND	R41	
NA	GND	T1	
NA	GND	T8	
NA	GND	T12	
NA	GND	T16	
NA	GND	T18	
NA	GND	T20	
NA	GND	T22	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	T24	
NA	GND	T26	
NA	GND	T28	
NA	GND	T33	
NA	GND	T38	
NA	GND	U4	
NA	GND	U5	
NA	GND	U13	
NA	GND	U15	
NA	GND	U17	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	
NA	GND	U25	
NA	GND	U27	
NA	GND	U29	
NA	GND	U35	
NA	GND	V2	
NA	GND	V12	
NA	GND	V14	
NA	GND	V16	
NA	GND	V18	
NA	GND	V20	
NA	GND	V22	
NA	GND	V24	
NA	GND	V26	
NA	GND	V28	
NA	GND	V30	
NA	GND	V32	
NA	GND	V42	
NA	GND	W2	
NA	GND	W9	
NA	GND	W13	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	W15	
NA	GND	W17	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W25	
NA	GND	W27	
NA	GND	W29	
NA	GND	W31	
NA	GND	W34	
NA	GND	W39	
NA	GND	Y4	
NA	GND	Y6	
NA	GND	Y11	
NA	GND	Y12	
NA	GND	Y14	
NA	GND	Y16	
NA	GND	Y18	
NA	GND	Y20	
NA	GND	Y24	
NA	GND	Y26	
NA	GND	Y28	
NA	GND	Y30	
NA	GND	Y36	
NA	GND	AA1	
NA	GND	AA13	
NA	GND	AA15	
NA	GND	AA17	
NA	GND	AA19	
NA	GND	AA23	
NA	GND	AA25	
NA	GND	AA27	
NA	GND	AA29	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AA31	
NA	GND	AA33	
NA	GND	AB1	
NA	GND	AB5	
NA	GND	AB10	
NA	GND	AB12	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB24	
NA	GND	AB26	
NA	GND	AB28	
NA	GND	AB30	
NA	GND	AB40	
NA	GND	AC4	
NA	GND	AC7	
NA	GND	AC11	
NA	GND	AC13	
NA	GND	AC15	
NA	GND	AC17	
NA	GND	AC19	
NA	GND	AC23	
NA	GND	AC25	
NA	GND	AC27	
NA	GND	AC29	
NA	GND	AC31	
NA	GND	AC32	
NA	GND	AC37	
NA	GND	AC42	
NA	GND	AD2	
NA	GND	AD12	
NA	GND	AD14	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AD16	
NA	GND	AD18	
NA	GND	AD20	
NA	GND	AD22	
NA	GND	AD24	
NA	GND	AD26	
NA	GND	AD28	
NA	GND	AD30	
NA	GND	AD34	
NA	GND	AE2	
NA	GND	AE11	
NA	GND	AE13	
NA	GND	AE15	
NA	GND	AE17	
NA	GND	AE19	
NA	GND	AE21	
NA	GND	AE23	
NA	GND	AE25	
NA	GND	AE27	
NA	GND	AE29	
NA	GND	AE31	
NA	GND	AE41	
NA	GND	AF4	
NA	GND	AF8	
NA	GND	AF14	
NA	GND	AF16	
NA	GND	AF18	
NA	GND	AF20	
NA	GND	AF22	
NA	GND	AF24	
NA	GND	AF26	
NA	GND	AF28	
NA	GND	AF33	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AF38	
NA	GND	AG1	
NA	GND	AG5	
NA	GND	AG13	
NA	GND	AG15	
NA	GND	AG17	
NA	GND	AG19	
NA	GND	AG21	
NA	GND	AG23	
NA	GND	AG25	
NA	GND	AG27	
NA	GND	AG35	
NA	GND	AH1	
NA	GND	AH12	
NA	GND	AH18	
NA	GND	AH20	
NA	GND	AH22	
NA	GND	AH24	
NA	GND	AH26	
NA	GND	AH28	
NA	GND	AH32	
NA	GND	AH42	
NA	GND	AJ4	
NA	GND	AJ9	
NA	GND	AJ13	
NA	GND	AJ14	
NA	GND	AJ17	
NA	GND	AJ19	
NA	GND	AJ23	
NA	GND	AJ25	
NA	GND	AJ27	
NA	GND	AJ29	
NA	GND	AJ39	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AK2	
NA	GND	AK6	
NA	GND	AK16	
NA	GND	AK21	
NA	GND	AK26	
NA	GND	AK31	
NA	GND	AK36	
NA	GND	AL2	
NA	GND	AL13	
NA	GND	AL18	
NA	GND	AL23	
NA	GND	AL33	
NA	GND	AM4	
NA	GND	AM5	
NA	GND	AM10	
NA	GND	AM15	
NA	GND	AM20	
NA	GND	AM25	
NA	GND	AM30	
NA	GND	AM40	
NA	GND	AN1	
NA	GND	AN7	
NA	GND	AN12	
NA	GND	AN17	
NA	GND	AN22	
NA	GND	AN27	
NA	GND	AN32	
NA	GND	AN37	
NA	GND	AN42	
NA	GND	AP1	
NA	GND	AP4	
NA	GND	AP14	
NA	GND	AP24	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AP29	
NA	GND	AP34	
NA	GND	AR4	
NA	GND	AR6	
NA	GND	AR11	
NA	GND	AR21	
NA	GND	AR31	
NA	GND	AR41	
NA	GND	AT2	
NA	GND	AT8	
NA	GND	AT18	
NA	GND	AT28	
NA	GND	AT38	
NA	GND	AU2	
NA	GND	AU5	
NA	GND	AU15	
NA	GND	AU25	
NA	GND	AU35	
NA	GND	AV4	
NA	GND	AV12	
NA	GND	AV22	
NA	GND	AV32	
NA	GND	AV42	
NA	GND	AW1	
NA	GND	AW6	
NA	GND	AW8	
NA	GND	AW11	
NA	GND	AW14	
NA	GND	AW17	
NA	GND	AW19	
NA	GND	AW29	
NA	GND	AW39	
NA	GND	AY26	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AY36	
NA	GND	AY41	
NA	GND	BA3	
NA	GND	BA4	
NA	GND	BA9	
NA	GND	BA10	
NA	GND	BA15	
NA	GND	BA16	
NA	GND	BA23	
NA	GND	BA33	
NA	GND	BA38	
NA	GND	BB6	
NA	GND	BB7	
NA	GND	BB12	
NA	GND	BB13	
NA	GND	BB18	
NA	GND	BB19	
NA	GND	BB25	
NA	GND	BB30	
NA	GND	BB35	
NA	GND	BB40	
NA	VCCAUX	R12	
NA	VCCAUX	T13	
NA	VCCAUX	T29	
NA	VCCAUX	U12	
NA	VCCAUX	U30	
NA	VCCAUX	W12	
NA	VCCAUX	W30	
NA	VCCAUX	Y31	
NA	VCCAUX	AA12	
NA	VCCAUX	AA30	
NA	VCCAUX	AB31	
NA	VCCAUX	AC12	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	AC30	
NA	VCCAUX	AD31	
NA	VCCAUX	AE12	
NA	VCCAUX	AE30	
NA	VCCAUX	AF13	
NA	VCCAUX	AF29	
NA	VCCAUX	AH13	
NA	VCCAUX	AJ12	
NA	VCCINT	P21	
NA	VCCINT	P23	
NA	VCCINT	R16	
NA	VCCINT	R18	
NA	VCCINT	R20	
NA	VCCINT	R22	
NA	VCCINT	R24	
NA	VCCINT	R26	
NA	VCCINT	R28	
NA	VCCINT	T15	
NA	VCCINT	T17	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	T23	
NA	VCCINT	T25	
NA	VCCINT	T27	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U18	
NA	VCCINT	U20	
NA	VCCINT	U22	
NA	VCCINT	U24	
NA	VCCINT	U26	
NA	VCCINT	U28	
NA	VCCINT	V13	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	V15	
NA	VCCINT	V17	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	V23	
NA	VCCINT	V25	
NA	VCCINT	V27	
NA	VCCINT	V29	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W18	
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	W24	
NA	VCCINT	W26	
NA	VCCINT	W28	
NA	VCCINT	Y13	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y23	
NA	VCCINT	Y25	
NA	VCCINT	Y27	
NA	VCCINT	Y29	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AA24	
NA	VCCINT	AA26	
NA	VCCINT	AA28	
NA	VCCINT	AB13	
NA	VCCINT	AB15	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB23	
NA	VCCINT	AB25	
NA	VCCINT	AB27	
NA	VCCINT	AB29	
NA	VCCINT	AC14	
NA	VCCINT	AC16	
NA	VCCINT	AC18	
NA	VCCINT	AC20	
NA	VCCINT	AC24	
NA	VCCINT	AC26	
NA	VCCINT	AC28	
NA	VCCINT	AD13	
NA	VCCINT	AD15	
NA	VCCINT	AD17	
NA	VCCINT	AD19	
NA	VCCINT	AD21	
NA	VCCINT	AD23	
NA	VCCINT	AD25	
NA	VCCINT	AD27	
NA	VCCINT	AD29	
NA	VCCINT	AE14	
NA	VCCINT	AE16	
NA	VCCINT	AE18	
NA	VCCINT	AE20	
NA	VCCINT	AE22	
NA	VCCINT	AE24	
NA	VCCINT	AE26	
NA	VCCINT	AE28	
NA	VCCINT	AF15	
NA	VCCINT	AF17	
NA	VCCINT	AF19	

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AF21	
NA	VCCINT	AF23	
NA	VCCINT	AF25	
NA	VCCINT	AF27	
NA	VCCINT	AG14	
NA	VCCINT	AG16	
NA	VCCINT	AG18	
NA	VCCINT	AG20	
NA	VCCINT	AG22	
NA	VCCINT	AG24	
NA	VCCINT	AG26	
NA	VCCINT	AG28	
NA	VCCINT	AH17	
NA	VCCINT	AH19	
NA	VCCINT	AH21	
NA	VCCINT	AH23	
NA	VCCINT	AH25	
NA	VCCINT	AH27	
NA	VCCINT	AJ18	
NA	VCCINT	AJ20	
NA	VCCINT	AJ24	
NA	UNUSED	A14	NC
NA	UNUSED	A15	NC
NA	UNUSED	A16	NC
NA	UNUSED	A17	NC
NA	UNUSED	A20	NC
NA	UNUSED	A21	NC
NA	UNUSED	A22	NC
NA	UNUSED	A24	NC
NA	UNUSED	A25	NC
NA	UNUSED	A26	NC
NA	UNUSED	A27	NC
NA	UNUSED	A29	NC

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	UNUSED	B13	NC
NA	UNUSED	B14	NC
NA	UNUSED	B17	NC
NA	UNUSED	B18	NC
NA	UNUSED	B21	NC
NA	UNUSED	B22	NC
NA	UNUSED	B23	NC
NA	UNUSED	B24	NC
NA	UNUSED	B26	NC
NA	UNUSED	B27	NC
NA	UNUSED	B28	NC
NA	UNUSED	B29	NC
NA	UNUSED	C13	NC
NA	UNUSED	C14	NC
NA	UNUSED	C16	NC
NA	UNUSED	C17	NC
NA	UNUSED	C18	NC
NA	UNUSED	C20	NC
NA	UNUSED	C21	NC
NA	UNUSED	C23	NC
NA	UNUSED	C24	NC
NA	UNUSED	C25	NC
NA	UNUSED	C26	NC
NA	UNUSED	C28	NC
NA	UNUSED	C29	NC
NA	UNUSED	C32	NC
NA	UNUSED	D16	NC
NA	UNUSED	D20	NC
NA	UNUSED	D21	NC
NA	UNUSED	D22	NC
NA	UNUSED	D23	NC
NA	UNUSED	D25	NC
NA	UNUSED	D26	NC

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	UNUSED	D27	NC
NA	UNUSED	D28	NC
NA	UNUSED	D29	NC
NA	UNUSED	D30	NC
NA	UNUSED	E24	NC
NA	UNUSED	E25	NC
NA	UNUSED	E27	NC
NA	UNUSED	E28	NC
NA	UNUSED	E29	NC
NA	UNUSED	E30	NC
NA	UNUSED	F30	NC
NA	UNUSED	G30	NC
NA	UNUSED	Y5	NC
NA	UNUSED	AA4	NC
NA	UNUSED	AL11	NC
NA	UNUSED	AL12	NC
NA	UNUSED	AM11	NC
NA	UNUSED	AM12	NC
NA	UNUSED	AN10	NC
NA	UNUSED	AN11	NC
NA	UNUSED	AP9	NC
NA	UNUSED	AP10	NC
NA	UNUSED	AP11	NC
NA	UNUSED	AP12	NC
NA	UNUSED	AR9	NC
NA	UNUSED	AR10	NC
NA	UNUSED	AR12	NC
NA	UNUSED	AR13	NC
NA	UNUSED	AT9	NC
NA	UNUSED	AT10	NC
NA	UNUSED	AT11	NC
NA	UNUSED	AT12	NC
NA	UNUSED	AU7	NC

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	UNUSED	AU8	NC
NA	UNUSED	AU9	NC
NA	UNUSED	AU10	NC
NA	UNUSED	AU11	NC
NA	UNUSED	AU12	NC
NA	UNUSED	AU13	NC
NA	UNUSED	AU14	NC
NA	UNUSED	AU16	NC
NA	UNUSED	AU17	NC
NA	UNUSED	AU30	NC
NA	UNUSED	AV7	NC
NA	UNUSED	AV8	NC
NA	UNUSED	AV9	NC
NA	UNUSED	AV10	NC
NA	UNUSED	AV11	NC
NA	UNUSED	AV13	NC
NA	UNUSED	AV14	NC
NA	UNUSED	AV15	NC
NA	UNUSED	AV16	NC
NA	UNUSED	AV18	NC
NA	UNUSED	AV19	NC
NA	UNUSED	AV26	NC
NA	UNUSED	AV28	NC
NA	UNUSED	AV29	NC
NA	UNUSED	AV30	NC
NA	UNUSED	AW7	NC
NA	UNUSED	AW12	NC
NA	UNUSED	AW13	NC
NA	UNUSED	AW15	NC
NA	UNUSED	AW18	NC
NA	UNUSED	AW20	NC
NA	UNUSED	AW21	NC
NA	UNUSED	AW22	NC

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	UNUSED	AW23	NC
NA	UNUSED	AW25	NC
NA	UNUSED	AW26	NC
NA	UNUSED	AW27	NC
NA	UNUSED	AW28	NC
NA	UNUSED	AW30	NC
NA	UNUSED	AY13	NC
NA	UNUSED	AY14	NC
NA	UNUSED	AY15	NC
NA	UNUSED	AY17	NC
NA	UNUSED	AY18	NC
NA	UNUSED	AY19	NC
NA	UNUSED	AY20	NC
NA	UNUSED	AY22	NC
NA	UNUSED	AY23	NC
NA	UNUSED	AY24	NC
NA	UNUSED	AY25	NC
NA	UNUSED	AY27	NC
NA	UNUSED	AY28	NC
NA	UNUSED	AY29	NC
NA	UNUSED	AY31	NC
NA	UNUSED	BA13	NC
NA	UNUSED	BA14	NC
NA	UNUSED	BA17	NC
NA	UNUSED	BA18	NC
NA	UNUSED	BA19	NC
NA	UNUSED	BA20	NC
NA	UNUSED	BA21	NC
NA	UNUSED	BA22	NC
NA	UNUSED	BA24	NC
NA	UNUSED	BA25	NC
NA	UNUSED	BA26	NC
NA	UNUSED	BA27	NC

Table 2-1: **CF1752 Package Pinout (XQR5VFX130) *(Continued)***

Bank	Pin Description	Pin Number	No Connect (NC)
NA	UNUSED	BA28	NC
NA	UNUSED	BA29	NC
NA	UNUSED	BB14	NC
NA	UNUSED	BB15	NC
NA	UNUSED	BB16	NC
NA	UNUSED	BB17	NC
NA	UNUSED	BB20	NC
NA	UNUSED	BB21	NC
NA	UNUSED	BB22	NC
NA	UNUSED	BB23	NC
NA	UNUSED	BB24	NC
NA	UNUSED	BB26	NC
NA	UNUSED	BB27	NC
NA	UNUSED	BB28	NC
NA	UNUSED	BB29	NC

Notes:

1. Do not connect a single-ended clock to the N-side of clock capable or global clock pins.

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Chapter 3

Pinout Diagrams

This chapter provides the pinout diagram for the Virtex-5QV FPGA in the CF1752 Package.

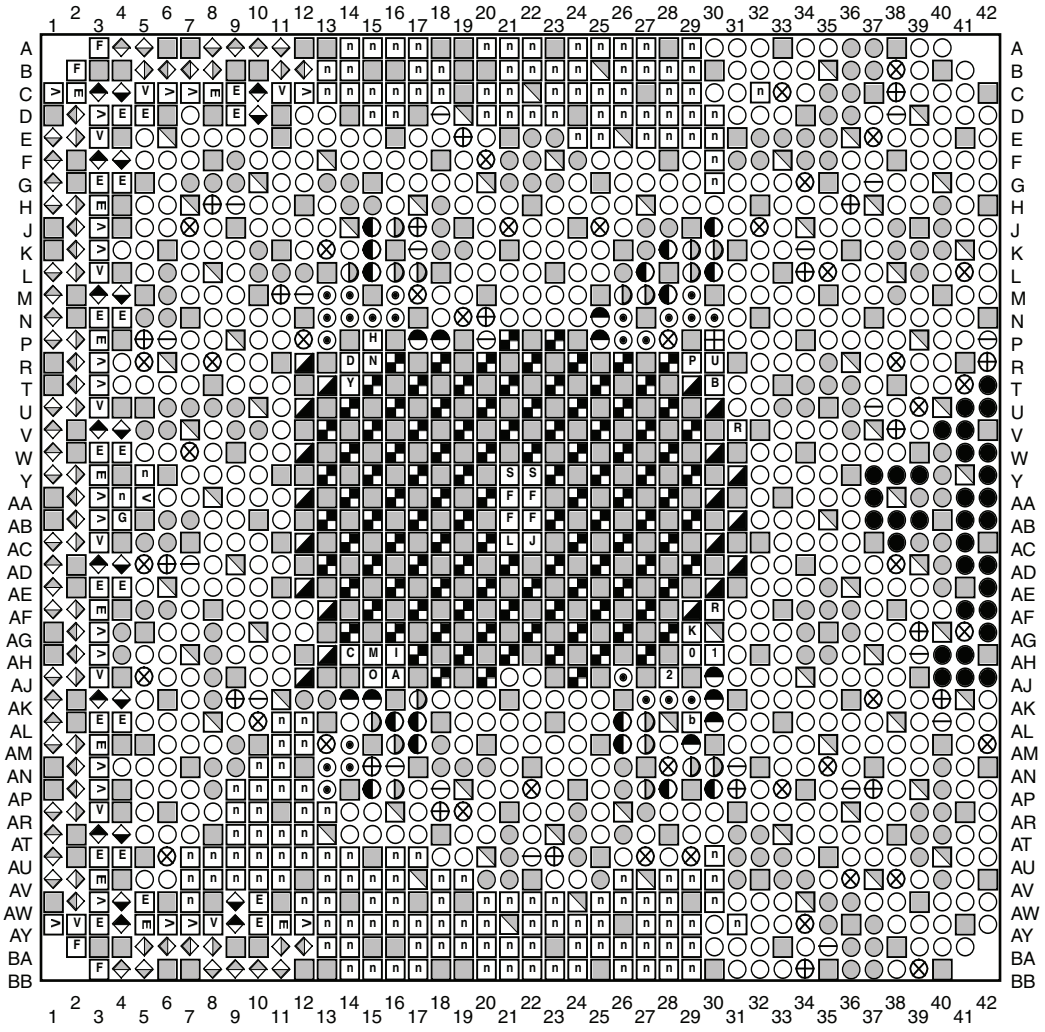
Note: Multi-function I/O pins are represented in these diagrams by symbols for only one of the pin's available functions, with precedence given to functionality in the following order:

- VREF, VRP, or VRN
- SM1 – SM7
- ADC1 – ADC7
- D0 – D31
- GC
- CC
- LC

For example, a pin description such as IO_L25N_CC_SM1_LC_7 is represented with an SM1-SM7 symbol, a pin description such as IO_L4N_GC_VREF_LC_4 is represented with a VREF symbol, and a pin description such as IO_L8P_D17_CC_LC_1 is represented with a D0-D31 symbol.

- CF1752 Package:
  - "CF1752 Package Pinout Diagram (XQR5VFX130)," page 70
  - "CF1752 Pinout Bank Diagram (XQR5VFX130)," page 71

CF1752 Package Pinout Diagram (XQR5VFX130)



User I/O Pins	Multi-Function Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	VREF	CCLK	PROGRAM_B	GND	MGTAVCC	MGTRXP
	VRN	CS_B	RDWR_B	RSVD	MGTAVCCPLL	MGTRXN
	VRP	D_IN	TCK	VBATT	MGTAVTTRX	MGTTXN
	P_GC	DONE	TDI	VCCAUX	MGTAVTTRXC	MGTTXP
	N_GC	D_OUT_BUSY	TDO	VCCINT	MGTAVTTTX	
	CC	HSWAPEN	TMS	VCCO	MGTREFCLKP	
	D0 - D31	INIT	DXP	NC	MGTREFCLKN	
	A0 - A25	M2, M1, M0	DXN	FLOAT	MGTRREF	
	SM	AVDD_0, AVSS_0, VP_0, VN_0, VREFP_0, VREFN_0				

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Figure 3-1: **CF1752 Package Pinout Diagram (XQR5VFX130)**

CF1752 Pinout Bank Diagram (XQR5VFX130)

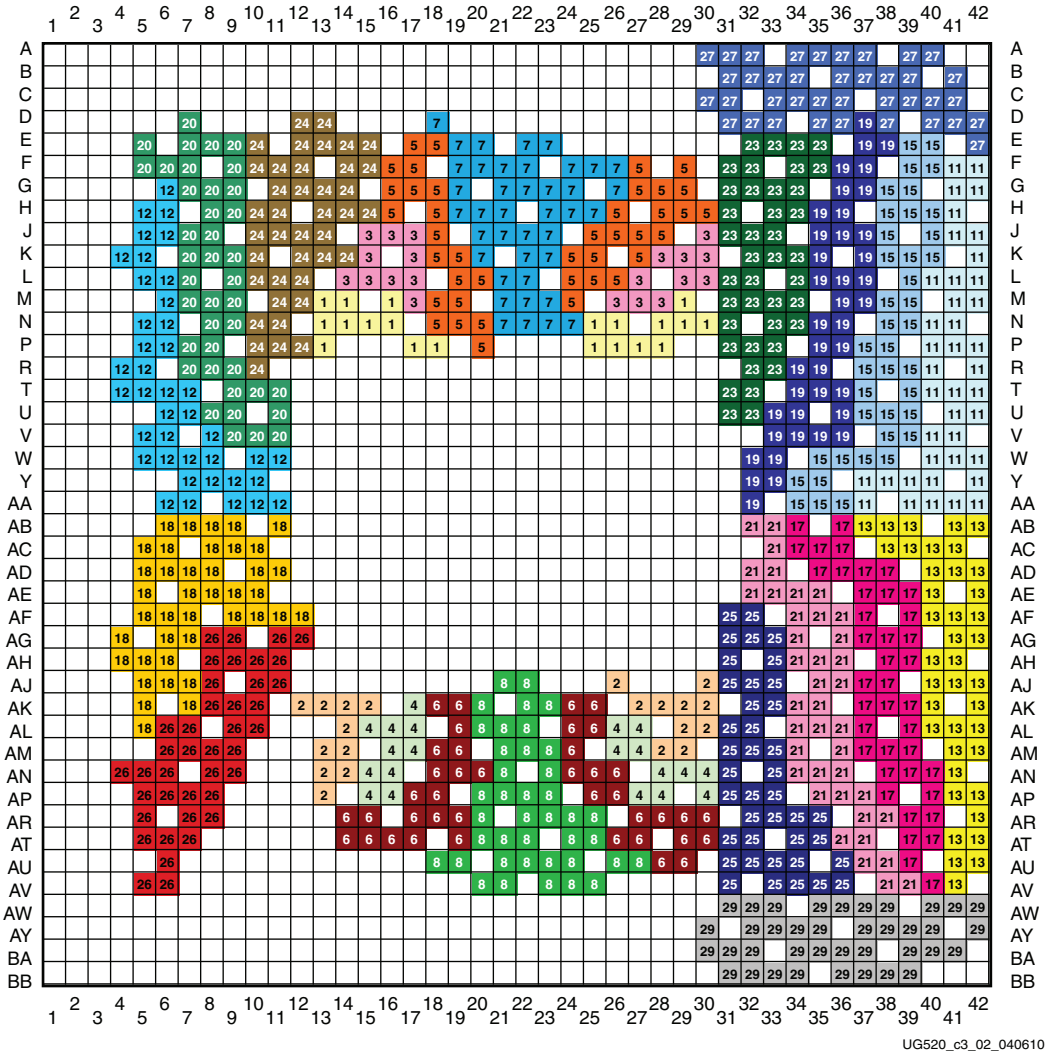

Figure 3-2: **CF1752 Bank Diagram**

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Chapter 4

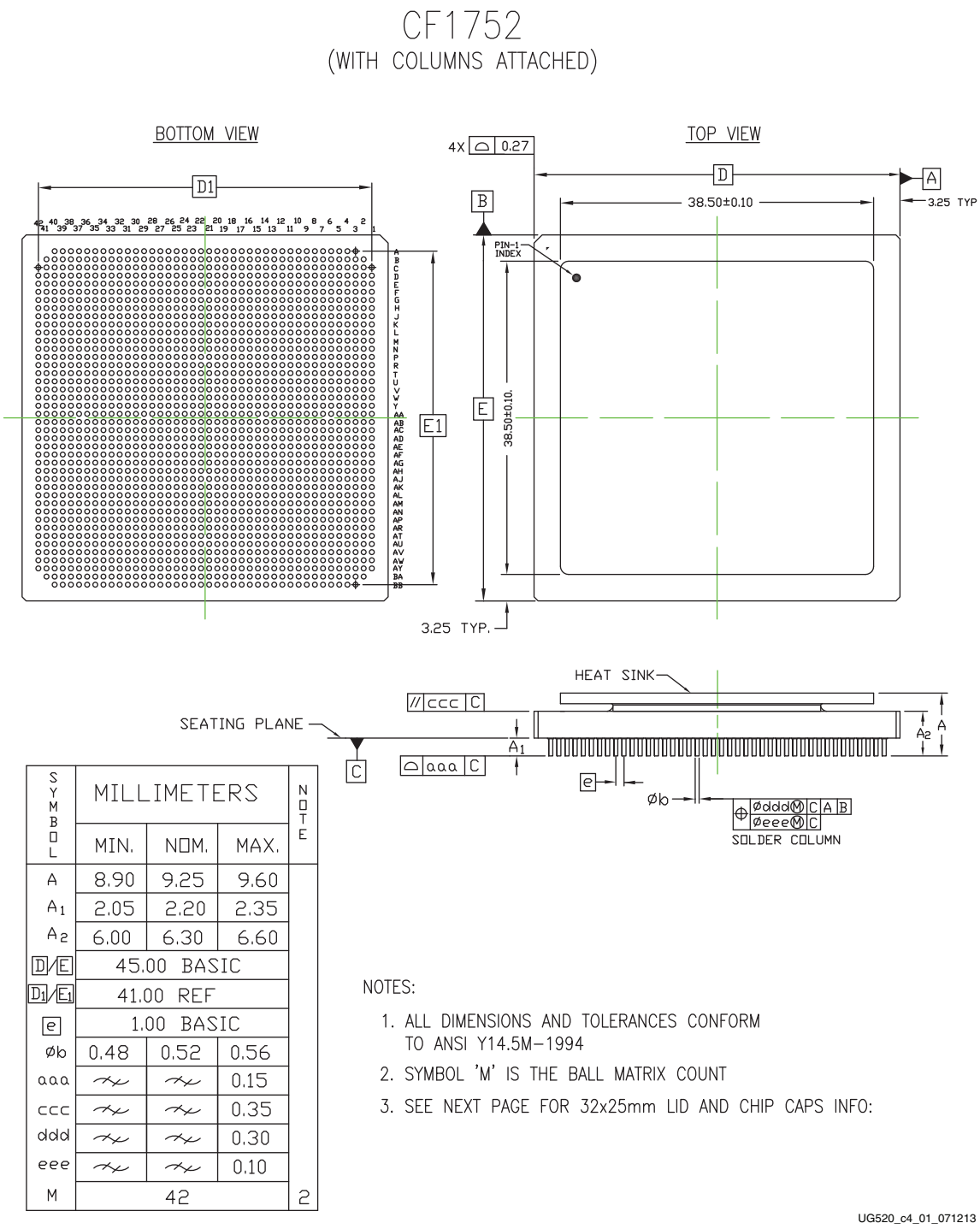
Mechanical Drawings

This chapter provides the mechanical drawing for the CF1752 package used by the radiation-hardened Virtex®-5QV FPGA.

Refer to XCN12020, *Virtex-4 and Virtex-5 QV FPGA CF Package Product Lid Size Change* for information about the change in lid size for the CF1752 package and part numbers affected by the change.

Refer to XCN13005, *Virtex-4 and Virtex-5 QV FPGA CF Package Assembly Location Change* for information on the discontinuation of the Virtex-5QV FPGA Ceramic Flip Chip Column Grid Array (CF package code), the Ceramic Flip Chip Land Grid Array that will be offered in its place (CN package code), and the replacement part numbers.

CF1752 Ceramic Flip-Chip Column Grid Array Package Specifications



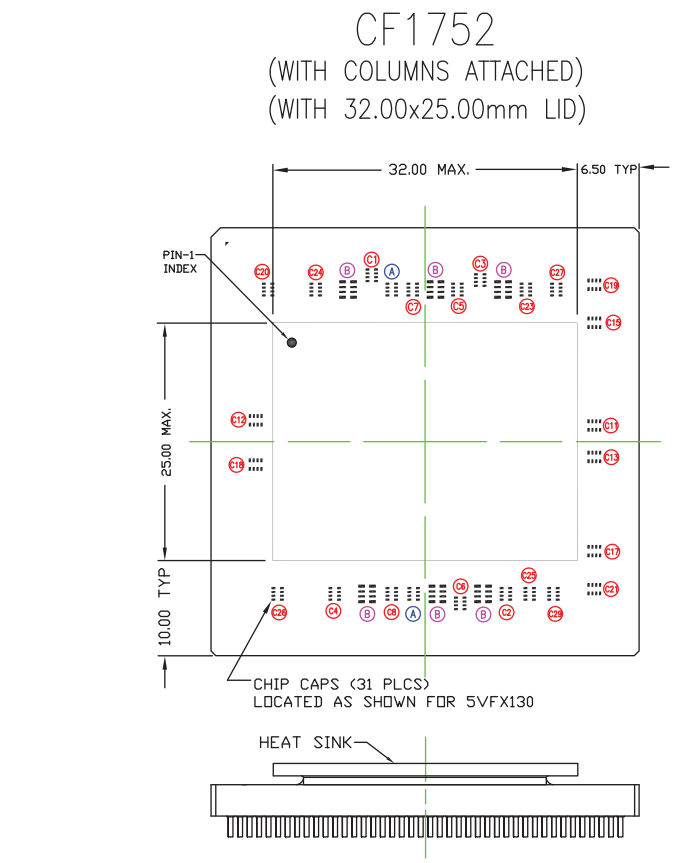
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	8.90	9.25	9.60	
A_1	2.05	2.20	2.35	
A_2	6.00	6.30	6.60	
D/E	45.00 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.48	0.52	0.56	
aaa	~	~	0.15	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	42			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX COUNT
3. SEE NEXT PAGE FOR 32x25mm LID AND CHIP CAPS INFO:

UG520_c4_01_071213

Figure 4-1: **CF1752 Ceramic Flip-Chip Column Grid Array Package Mechanical Drawing (38.5 mm × 38.5 mm Lid)**



NOTES:

1. THIS PAGE IS TO SHOW THE OPTIONAL LID AND CHIP CAP LOCATIONS.
2. ALL DIMENSIONS ARE THE SAME EXCEPT FOR THE LID.
3. CHIP CAPS: ACCEPTS 0603 (25 PLCS) AND 0805 (6 PLCS)
4. CHIP CAP REFERENCE: (A) – VCCAUX
   (B) – VCCINT
   (CN) – VCCO_[1~29] ("N" CORRESPONDS TO BANK NUMBER)

UG520_c4_02_071213

Figure 4-2: **CF1752 Ceramic Flip-Chip Column Grid Array Package Mechanical Drawing (32 mm × 25 mm Lid)**

Chapter 5

Recommended PCB Design Rules

This chapter defines recommended PCB design rules for the Virtex®-5QV FPGA in the CF1752 package including "Pad Land Dimensions", "Keep-Out Area", and "Grounding Pins Having No Connection".

Pad Land Dimensions

Xilinx provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the package side land geometry. The package land pad diameter is provided in Table 5-1. Typical PCB dimensions are described in Figure 5-1 and summarized in Table 5-1. These are guidelines only and can vary depending on PCB vendor and assembly capability. Non-Solder Mask Defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 5-1. The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB manufacturing process.

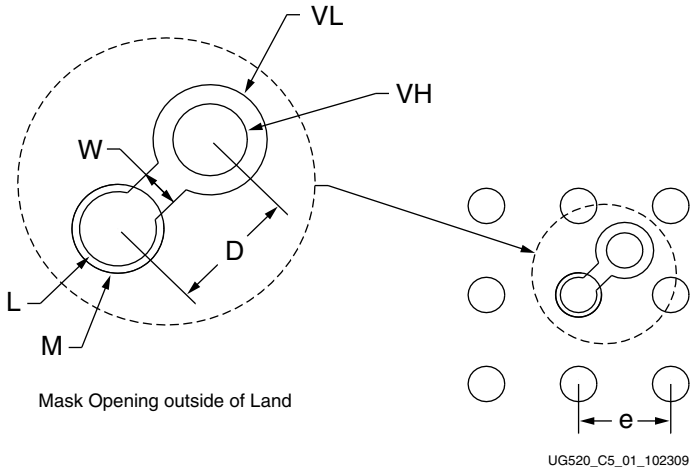


Figure 5-1: **Suggested Board Layout of Soldered Pads**

Table 5-1: **Recommended Dimensions (Figure 5-1)**

Description	Reference	Dimension (mm)
Package Land Pad Diameter		0.80
Solder Land Diameter	L	0.70
Opening in Solder Mask Diameter	M	0.80

Table 5-1: **Recommended Dimensions (Figure 5-1) *(Continued)***

Description	Reference	Dimension (mm)
Solder (Ball) Land Pitch	e	1.00
Line Width Between Via and Land	W	0.20
Distance Between Via and Land	D	0.70
Via Land Diameter	VL	0.46
Through Hole Diameter	VH	0.200

Keep-Out Area

To avoid physical conflicts between the CF1752 package and other components mounted on the PCB, the other components must not encroach in the space defined in Figure 5-2.

The space defined in Figure 5-2 must also be observed when using the super-set footprint defined in Table 8-1, page 83 to accommodate either the commercial XC5VFX130T Virtex-5 FPGA or the XQR5VFX130 Virtex-5QV FPGA

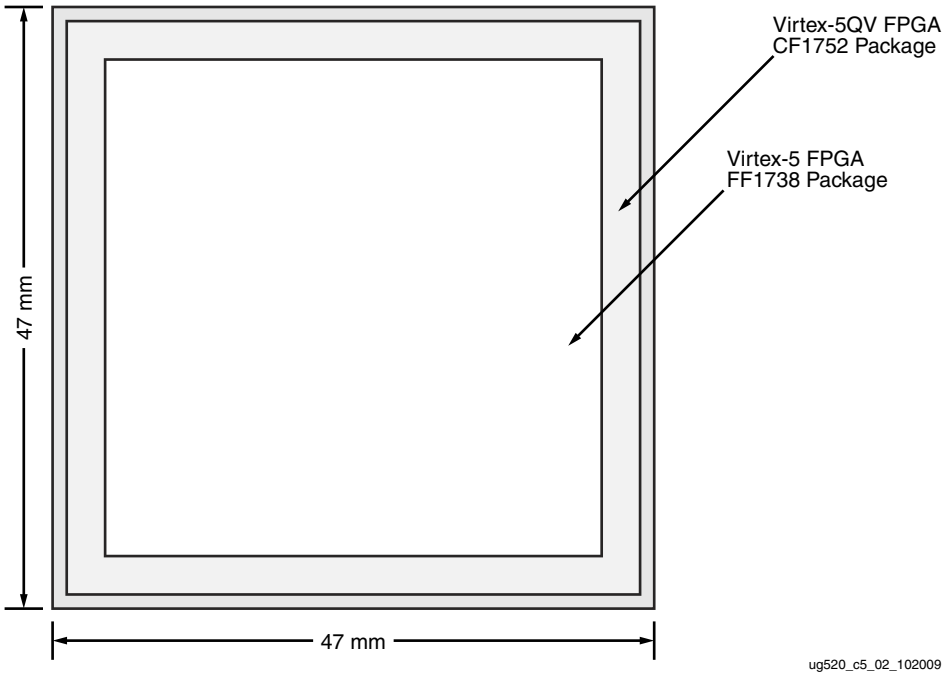


Figure 5-2: **Keep-Out Area for the CF1752 and FF1738 Package**

Grounding Pins Having No Connection

If the Virtex-5QV FPGA is used in a space or high-altitude environment, connect all pins defined as being unbonded or having no connections (NC) to system ground. `R_FUSE_0` and `VFS_0` must also be connected to GND.

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Chapter 6

Thermal Specifications

This chapter provides thermal data associated with Virtex-5QV FPGA packaging.

Introduction

Ceramic flip-chip column grid array (CF) packages are surface-mount-compatible packages using high-temperature solder columns as interconnections to the board. Compared to the solder spheres, the columns have lower stiffness and provide a higher stand-off. These features significantly increase the reliability of the solder joints. When combined with a high-density, multi-layer ceramic substrate, this packaging technology offers a high-density, reliable packaging solution.

CF Package Construction and Key Features

- IBM technology
- Qualified per MIL-STD-883
- Non-hermetic multi-layer ceramic substrate
- High planarity and excellent thermal stability at high temperature
- CTE matches well with the silicon die
- Low corrosion sensitivity
- Meets JEDEC MSL-1
- Meets NASA outgas requirements
- 90% Pb/10% Sn core columns
- 95% Pb/5% Sn die solder bumps
- Silicon carbide heat-spreader

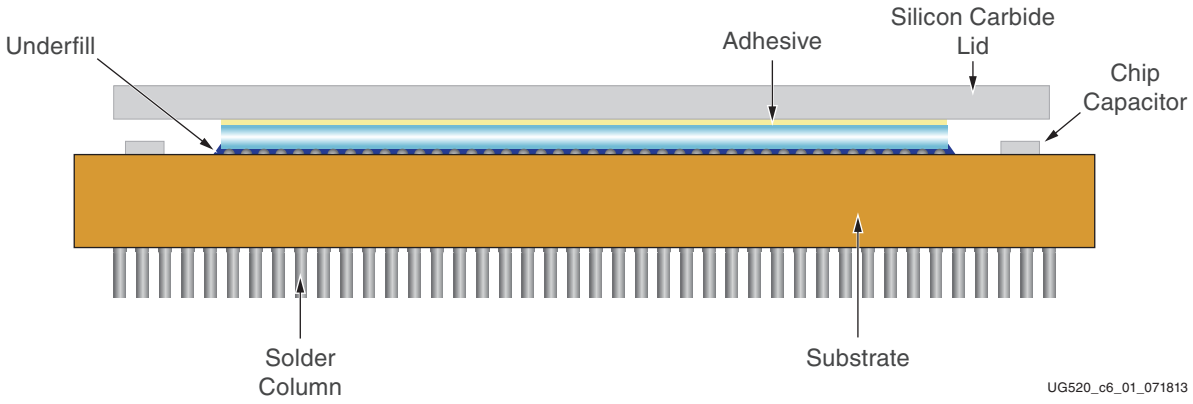

Figure 6-1: **CF1752 Package Construction with 38.5 mm × 38.5 mm Lid**

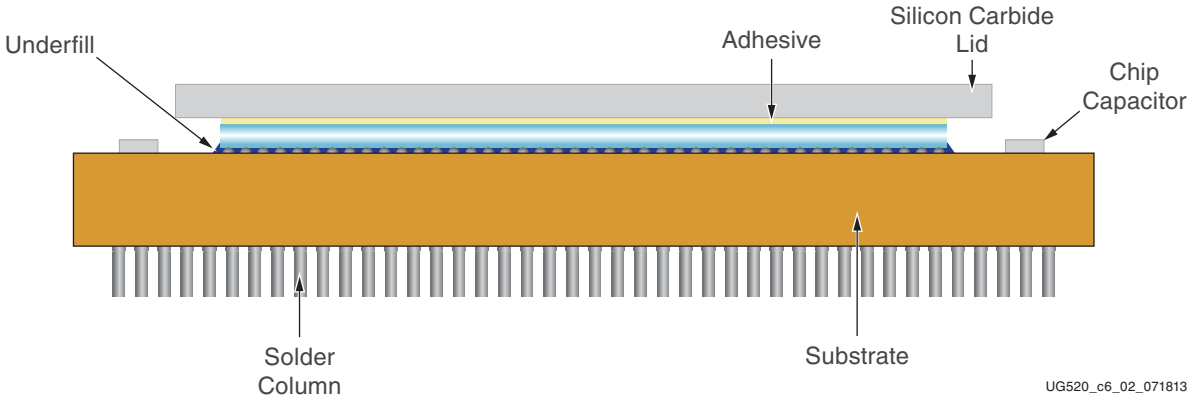

Figure 6-2: **CF1752 Package Construction with 32 mm × 25 mm Lid**

For more information on CGA technology and PCB recommendations refer to the *Ceramic Column Grid Assembly and Rework User Guide* by IBM (http://www.ibm.com).

Thermal Resistance and Package Mass

Virtex-5QV FPGAs are offered exclusively in CF packages for high thermal cycle reliability. The Virtex-5QV FPGA ceramic packages thermal resistance and package mass data is listed in Table 6-1. Additionally the junction-to-case and junction-to-board data (based on standard JEDEC four-layer measurements) is provided.

Table 6-1: **Thermal Characteristics**

Package	Device	Package Body Size	θJC (°C/Watt)	θJB (°C/Watt)	θJA (°C/Watt)	Mass (grams)
CF1752 (38.5 mm × 38.5 mm lid)	XQR5VFX130	45 mm × 45 mm	0.06	2.0	7.2	54.57
CF1752 (32 mm × 25 mm lid)	XQR5VFX130	45 mm × 45 mm	0.10	2.21	8.1	50.0

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Chapter 7

Reflow Soldering Process Guidelines

The Virtex®-5QV FPGAs are packaged in CF1752 packages using IBM's high-lead (Pb) solid-cast solder columns consisting of 90% lead and 10% tin. The columns are attached to the packages at IBM using a fully automated column-attach line. The last production step is a 100% laser-scan inspection. After inspection, the columns are not touched by IBM or Xilinx to ensure no bent columns. The devices are then pick and placed into shipping trays, with 1 unit per tray to avoid unnecessary handling.

Xilinx and IBM recommend that extreme care be taken when removing the parts from the trays. Remove the parts from the tray at a 90° angle to prevent columns from being bent. It is best to use an automatic pick and place machine to remove the parts.

Like BGA packages, the CF1752 package board level assembly process involves screen printing, solder reflow, and post reflow washing. General board mounting recommendations are available in the *Ceramic Column Grid Array Assembly and Rework User's Guide*, IBM, www.ibm.com.

It is highly recommended to use either a no-clean or a water-soluble solder paste. If cleaning is required, it is recommended to use a water-soluble paste and then wash with deionized water in a washer. Cleaning surfactants or solvents are not recommended because some cleaning solutions might contain chemicals that can attack the chip capacitors.

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Chapter 8

Pin Cross-Reference for PCB Prototyping with a Commercial Part

To minimize costs during development, the commercial XC5VFX130T Virtex®-5 FPGA can be substituted in place of the XQR5VFX130 Virtex-5QV FPGA, provided the differences in pin assignments are considered in the layout. Table 8-1 shows the pin assignments for both devices, and provides a super-set footprint that permits either device to be placed on to this footprint.

The keep-out space defined in Figure 5-2 must be observed when using the super-set footprint defined in Table 8-1 to accommodate either the commercial XC5VFX130T Virtex-5 FPGA or the XQR5VFX130 Virtex-5QV FPGA. All FPGA pins having no connection (listed as UNPOPULATED or UNUSED in Table 8-1 must be connected to GND for space flight compatibility. R_FUSE_0 and VFS_0 must also be connected to GND.

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA**

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
A2	NA	GND	A2	MGTRXP1_124	A2	UNPOPULATED	
A3	NA	GND	A3	MGTRXN1_124	A3	MGTRXN1_124	NC
A4	NA	MGTRXN0_124	A4	MGTRXN0_124	A4	MGTRXN0_124	
A5	NA	MGTRXP0_124	A5	MGTRXP0_124	A5	MGTRXP0_124	
A6	NA	GND	A6	UNPOPULATED	A6	GND	
A7	NA	GND	A7	UNPOPULATED	A7	GND	
A8	NA	MGTRXP1_128	A8	MGTRXP1_128	A8	MGTRXP1_128	
A9	NA	MGTRXN1_128	A9	MGTRXN1_128	A9	MGTRXN1_128	
A10	NA	MGTRXN0_128	A10	MGTRXN0_128	A10	MGTRXN0_128	
A11	NA	MGTRXP0_128	A11	MGTRXP0_128	A11	MGTRXP0_128	
A12	NA	GND	A12	UNPOPULATED	A12	GND	
A13	NA	GND	A13	UNPOPULATED	A13	GND	
A14	NA	GND	A14	UNUSED	A14	UNUSED	NC
A15	NA	GND	A15	UNUSED	A15	UNUSED	NC
A16	NA	GND	A16	UNUSED	A16	UNUSED	NC
A17	NA	GND	A17	UNUSED	A17	UNUSED	NC
A18	NA	GND	A18	UNPOPULATED	A18	GND	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
A19	NA	GND	A19	GND	A19	GND	
A20	NA	GND	A20	UNUSED	A20	UNUSED	NC
A21	NA	GND	A21	UNUSED	A21	UNUSED	NC
A22	NA	GND	A22	UNUSED	A22	UNUSED	NC
A23	NA	GND	A23	GND	A23	GND	
A24	NA	GND	A24	UNUSED	A24	UNUSED	NC
A25	NA	GND	A25	UNUSED	A25	UNUSED	NC
A26	NA	GND	A26	UNUSED	A26	UNUSED	NC
A27	NA	GND	A27	UNUSED	A27	UNUSED	NC
A28	NA	GND	A28	GND	A28	GND	
A29	NA	GND	A29	UNUSED	A29	UNUSED	NC
A30	27	IO_L2P_27	A30	IO_L2P_27	A30	IO_L2P_27	
A31	27	IO_L2N_27	A31	IO_L2N_27	A31	IO_L2N_27	
A32	27	IO_L3P_27	A32	IO_L3P_27	A32	IO_L3P_27	
A33	NA	GND	A33	GND	A33	GND	
A34	27	IO_L7P_27	A34	IO_L7P_27	A34	IO_L7P_27	
A35	27	IO_L7N_27	A35	IO_L7N_27	A35	IO_L7N_27	
A36	27	IO_L10N_CC_27	A36	IO_L10N_CC_27	A36	IO_L10N_CC_27	
A37	27	IO_L10P_CC_27	A37	IO_L10P_CC_27	A37	IO_L10P_CC_27	
A38	NA	GND	A38	GND	A38	GND	
A39	27	IO_L15P_27	A39	IO_L15P_27	A39	IO_L15P_27	
A40	27	IO_L15N_27	A40	IO_L15N_27	A40	IO_L15N_27	
A41	27	GND	A41	IO_L16P_27	A41	UNPOPULATED	
B1	NA	GND	B1	MGTTXP1_124	B1	UNPOPULATED	
B2	NA	GND	B2	MGTTXN1_124	B2	MGTTXN1_124	NC
B3	NA	GND	B3	GND	B3	GND	
B4	NA	GND	B4	GND	B4	GND	
B5	NA	MGTTXN0_124	B5	MGTTXN0_124	B5	MGTTXN0_124	
B6	NA	MGTTXP0_124	B6	MGTTXP0_124	B6	MGTTXP0_124	
B7	NA	MGTTXP1_128	B7	MGTTXP1_128	B7	MGTTXP1_128	
B8	NA	MGTTXN1_128	B8	MGTTXN1_128	B8	MGTTXN1_128	
B9	NA	GND	B9	GND	B9	GND	
B10	NA	GND	B10	GND	B10	GND	
B11	NA	MGTTXN0_128	B11	MGTTXN0_128	B11	MGTTXN0_128	
B12	NA	MGTTXP0_128	B12	MGTTXP0_128	B12	MGTTXP0_128	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
B13	NA	GND	B13	UNUSED	B13	UNUSED	NC
B14	NA	GND	B14	UNUSED	B14	UNUSED	NC
B15	NA	GND	B15	GND	B15	GND	
B16	NA	GND	B16	GND	B16	GND	
B17	NA	GND	B17	UNUSED	B17	UNUSED	NC
B18	NA	GND	B18	UNUSED	B18	UNUSED	NC
B19	NA	GND	B19	GND	B19	GND	
B20	NA	GND	B20	GND	B20	GND	
B21	NA	GND	B21	UNUSED	B21	UNUSED	NC
B22	NA	GND	B22	UNUSED	B22	UNUSED	NC
B23	NA	GND	B23	UNUSED	B23	UNUSED	NC
B24	NA	GND	B24	UNUSED	B24	UNUSED	NC
B25	5	VCCO_5	B25	VCCO_5	B25	VCCO_5	
B26	NA	GND	B26	UNUSED	B26	UNUSED	NC
B27	NA	GND	B27	UNUSED	B27	UNUSED	NC
B28	NA	GND	B28	UNUSED	B28	UNUSED	NC
B29	NA	GND	B29	UNUSED	B29	UNUSED	NC
B30	NA	GND	B30	GND	B30	GND	
B31	27	IO_L1N_27	B31	IO_L1N_27	B31	IO_L1N_27	
B32	27	IO_L3N_27	B32	IO_L3N_27	B32	IO_L3N_27	
B33	27	IO_L4P_27	B33	IO_L4P_27	B33	IO_L4P_27	
B34	27	IO_L6N_27	B34	IO_L6N_27	B34	IO_L6N_27	
B35	27	VCCO_27	B35	VCCO_27	B35	VCCO_27	
B36	27	IO_L11N_CC_27	B36	IO_L11N_CC_27	B36	IO_L11N_CC_27	
B37	27	IO_L11P_CC_27	B37	IO_L11P_CC_27	B37	IO_L11P_CC_27	
B38	27	IO_L14N_VREF_27	B38	IO_L14N_VREF_27	B38	IO_L14N_VREF_27	
B39	27	IO_L14P_27	B39	IO_L14P_27	B39	IO_L14P_27	
B40	NA	GND	B40	GND	B40	GND	
B41	27	IO_L16N_27	B41	IO_L16N_27	B41	IO_L16N_27	
B42	27	GND	B42	IO_L17P_27	B42	UNPOPULATED	
C1	NA	MGTAVTTTX_124	C1	MGTAVTTTX_124	C1	MGTAVTTTX_124	
C2	NA	MGTAVCCPLL_124	C2	MGTAVCCPLL_124	C2	MGTAVCCPLL_124	
C3	NA	MGTREFCLKN_124	C3	MGTREFCLKN_124	C3	MGTREFCLKN_124	
C4	NA	MGTREFCLKP_124	C4	MGTREFCLKP_124	C4	MGTREFCLKP_124	
C5	NA	MGTAVTTRX_124	C5	MGTAVTTRX_124	C5	MGTAVTTRX_124	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
C6	NA	MGTAVTTTX_124	C6	MGTAVTTTX_124	C6	MGTAVTTTX_124	
C7	NA	MGTAVTTTX_128	C7	MGTAVTTTX_128	C7	MGTAVTTTX_128	
C8	NA	MGTAVCCPLL_128	C8	MGTAVCCPLL_128	C8	MGTAVCCPLL_128	
C9	NA	MGTAVCC_128	C9	MGTAVCC_128	C9	MGTAVCC_128	
C10	NA	MGTREFCLKN_128	C10	MGTREFCLKN_128	C10	MGTREFCLKN_128	
C11	NA	MGTAVTTRX_128	C11	MGTAVTTRX_128	C11	MGTAVTTRX_128	
C12	NA	MGTAVTTTX_128	C12	MGTAVTTTX_128	C12	MGTAVTTTX_128	
C13	NA	GND	C13	UNUSED	C13	UNUSED	NC
C14	NA	GND	C14	UNUSED	C14	UNUSED	NC
C15	NA	GND	C15	MGTAVCC_132	C15	MGTAVCC_132	NC
C16	NA	GND	C16	UNUSED	C16	UNUSED	NC
C17	NA	GND	C17	UNUSED	C17	UNUSED	NC
C18	NA	GND	C18	UNUSED	C18	UNUSED	NC
C19	NA	GND	C19	GND	C19	GND	
C20	NA	GND	C20	UNUSED	C20	UNUSED	NC
C21	NA	GND	C21	UNUSED	C21	UNUSED	NC
C22	5	VCCO_5	C22	VCCO_5	C22	VCCO_5	
C23	NA	GND	C23	UNUSED	C23	UNUSED	NC
C24	NA	GND	C24	UNUSED	C24	UNUSED	NC
C25	NA	GND	C25	UNUSED	C25	UNUSED	NC
C26	NA	GND	C26	UNUSED	C26	UNUSED	NC
C27	NA	GND	C27	GND	C27	GND	
C28	NA	GND	C28	UNUSED	C28	UNUSED	NC
C29	NA	GND	C29	UNUSED	C29	UNUSED	NC
C30	27	IO_L1P_27	C30	IO_L1P_27	C30	IO_L1P_27	
C31	27	IO_L0N_27	C31	IO_L0N_27	C31	IO_L0N_27	
C32	NA	GND	C32	UNUSED	C32	UNUSED	NC
C33	27	IO_L4N_VREF_27	C33	IO_L4N_VREF_27	C33	IO_L4N_VREF_27	
C34	27	IO_L6P_27	C34	IO_L6P_27	C34	IO_L6P_27	
C35	27	IO_L9N_CC_27	C35	IO_L9N_CC_27	C35	IO_L9N_CC_27	
C36	27	IO_L9P_CC_27	C36	IO_L9P_CC_27	C36	IO_L9P_CC_27	
C37	NA	GND	C37	GND	C37	GND	
C38	27	IO_L12P_VRN_27	C38	IO_L12P_VRN_27	C38	IO_L12P_VRN_27	
C39	27	IO_L13P_27	C39	IO_L13P_27	C39	IO_L13P_27	
C40	27	IO_L13N_27	C40	IO_L13N_27	C40	IO_L13N_27	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
C41	27	IO_L17N_27	C41	IO_L17N_27	C41	IO_L17N_27	
C42	NA	GND	C42	GND	C42	GND	
D1	NA	GND	D1	UNPOPULATED	D1	GND	
D2	NA	MGTTXP0_120	D2	MGTTXP0_120	D2	MGTTXP0_120	
D3	NA	MGTAVTTTX_120	D3	MGTAVTTTX_120	D3	MGTAVTTTX_120	
D4	NA	MGTAVCC_124	D4	MGTAVCC_124	D4	MGTAVCC_124	
D5	NA	MGTAVCC_124	D5	MGTAVCC_124	D5	MGTAVCC_124	
D6	NA	GND	D6	GND	D6	GND	
D7	20	IO_L3P_20	D7	IO_L3P_20	D7	IO_L3P_20	
D8	NA	GND	D8	GND	D8	GND	
D9	NA	MGTAVCC_128	D9	MGTAVCC_128	D9	MGTAVCC_128	
D10	NA	MGTREFCLKP_128	D10	MGTREFCLKP_128	D10	MGTREFCLKP_128	
D11	NA	GND	D11	GND	D11	GND	
D12	24	IO_L15N_24	D12	IO_L15N_24	D12	IO_L15N_24	
D13	24	IO_L17P_24	D13	IO_L17P_24	D13	IO_L17P_24	
D14	NA	GND	D14	GND	D14	GND	
D15	NA	GND	D15	MGTAVCC_132	D15	MGTAVCC_132	NC
D16	NA	GND	D16	UNUSED	D16	UNUSED	NC
D17	NA	GND	D17	GND	D17	GND	
D18	7	IO_L12N_VRP_7	D18	IO_L12N_VRP_7	D18	IO_L12N_VRP_7	
D19	7	VCCO_7	D19	VCCO_7	D19	VCCO_7	
D20	NA	GND	D20	UNUSED	D20	UNUSED	NC
D21	NA	GND	D21	UNUSED	D21	UNUSED	NC
D22	NA	GND	D22	UNUSED	D22	UNUSED	NC
D23	NA	GND	D23	UNUSED	D23	UNUSED	NC
D24	NA	GND	D24	GND	D24	GND	
D25	NA	GND	D25	UNUSED	D25	UNUSED	NC
D26	NA	GND	D26	UNUSED	D26	UNUSED	NC
D27	NA	GND	D27	UNUSED	D27	UNUSED	NC
D28	NA	GND	D28	UNUSED	D28	UNUSED	NC
D29	NA	GND	D29	UNUSED	D29	UNUSED	NC
D30	NA	GND	D30	UNUSED	D30	UNUSED	NC
D31	27	IO_L0P_27	D31	IO_L0P_27	D31	IO_L0P_27	
D32	27	IO_L5P_27	D32	IO_L5P_27	D32	IO_L5P_27	
D33	27	IO_L5N_27	D33	IO_L5N_27	D33	IO_L5N_27	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
D34	NA	GND	D34	GND	D34	GND	
D35	27	IO_L8P_CC_27	D35	IO_L8P_CC_27	D35	IO_L8P_CC_27	
D36	27	IO_L8N_CC_27	D36	IO_L8N_CC_27	D36	IO_L8N_CC_27	
D37	19	IO_L15N_19	D37	IO_L15N_19	D37	IO_L15N_19	
D38	27	IO_L12N_VRP_27	D38	IO_L12N_VRP_27	D38	IO_L12N_VRP_27	
D39	23	VCCO_23	D39	VCCO_23	D39	VCCO_23	
D40	27	IO_L18P_27	D40	IO_L18P_27	D40	IO_L18P_27	
D41	27	IO_L18N_27	D41	IO_L18N_27	D41	IO_L18N_27	
D42	27	IO_L19N_27	D42	IO_L19N_27	D42	IO_L19N_27	
E1	NA	MGTRXP0_120	E1	MGTRXP0_120	E1	MGTRXP0_120	
E2	NA	MGTTXN0_120	E2	MGTTXN0_120	E2	MGTTXN0_120	
E3	NA	MGTAVTTRX_120	E3	MGTAVTTRX_120	E3	MGTAVTTRX_120	
E4	NA	GND	E4	GND	E4	GND	
E5	20	IO_L7P_20	E5	IO_L7P_20	E5	IO_L7P_20	
E6	24	VCCO_24	E6	VCCO_24	E6	VCCO_24	
E7	20	IO_L3N_20	E7	IO_L3N_20	E7	IO_L3N_20	
E8	20	IO_L1N_20	E8	IO_L1N_20	E8	IO_L1N_20	
E9	20	IO_L1P_20	E9	IO_L1P_20	E9	IO_L1P_20	
E10	24	IO_L3P_24	E10	IO_L3P_24	E10	IO_L3P_24	
E11	NA	GND	E11	GND	E11	GND	
E12	24	IO_L15P_24	E12	IO_L15P_24	E12	IO_L15P_24	
E13	24	IO_L13N_24	E13	IO_L13N_24	E13	IO_L13N_24	
E14	24	IO_L17N_24	E14	IO_L17N_24	E14	IO_L17N_24	
E15	24	IO_L19P_24	E15	IO_L19P_24	E15	IO_L19P_24	
E16	NA	GND	E16	GND	E16	GND	
E17	5	IO_L1N_5	E17	IO_L1N_5	E17	IO_L1N_5	
E18	5	IO_L1P_5	E18	IO_L1P_5	E18	IO_L1P_5	
E19	7	IO_L12P_VRN_7	E19	IO_L12P_VRN_7	E19	IO_L12P_VRN_7	
E20	7	IO_L14P_7	E20	IO_L14P_7	E20	IO_L14P_7	
E21	NA	GND	E21	GND	E21	GND	
E22	7	IO_L10P_CC_7	E22	IO_L10P_CC_7	E22	IO_L10P_CC_7	
E23	7	IO_L10N_CC_7	E23	IO_L10N_CC_7	E23	IO_L10N_CC_7	
E24	NA	GND	E24	UNUSED	E24	UNUSED	NC
E25	NA	GND	E25	UNUSED	E25	UNUSED	NC
E26	3	VCCO_3	E26	VCCO_3	E26	VCCO_3	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
E27	NA	GND	E27	UNUSED	E27	UNUSED	NC
E28	NA	GND	E28	UNUSED	E28	UNUSED	NC
E29	NA	GND	E29	UNUSED	E29	UNUSED	NC
E30	NA	GND	E30	UNUSED	E30	UNUSED	NC
E31	NA	GND	E31	GND	E31	GND	
E32	23	IO_L11P_CC_23	E32	IO_L11P_CC_23	E32	IO_L11P_CC_23	
E33	23	IO_L11N_CC_23	E33	IO_L11N_CC_23	E33	IO_L11N_CC_23	
E34	23	IO_L9P_CC_23	E34	IO_L9P_CC_23	E34	IO_L9P_CC_23	
E35	23	IO_L8N_CC_23	E35	IO_L8N_CC_23	E35	IO_L8N_CC_23	
E36	23	VCCO_23	E36	VCCO_23	E36	VCCO_23	
E37	19	IO_L14N_VREF_19	E37	IO_L14N_VREF_19	E37	IO_L14N_VREF_19	
E38	19	IO_L15P_19	E38	IO_L15P_19	E38	IO_L15P_19	
E39	15	IO_L3P_15	E39	IO_L3P_15	E39	IO_L3P_15	
E40	15	IO_L3N_15	E40	IO_L3N_15	E40	IO_L3N_15	
E41	NA	GND	E41	GND	E41	GND	
E42	27	IO_L19P_27	E42	IO_L19P_27	E42	IO_L19P_27	
F1	NA	MGTRXN0_120	F1	MGTRXN0_120	F1	MGTRXN0_120	
F2	NA	GND	F2	GND	F2	GND	
F3	NA	MGTREFCLKN_120	F3	MGTREFCLKN_120	F3	MGTREFCLKN_120	
F4	NA	MGTREFCLKP_120	F4	MGTREFCLKP_120	F4	MGTREFCLKP_120	
F5	20	IO_L7N_20	F5	IO_L7N_20	F5	IO_L7N_20	
F6	20	IO_L5N_20	F6	IO_L5N_20	F6	IO_L5N_20	
F7	20	IO_L5P_20	F7	IO_L5P_20	F7	IO_L5P_20	
F8	NA	GND	F8	GND	F8	GND	
F9	20	IO_L9P_CC_20	F9	IO_L9P_CC_20	F9	IO_L9P_CC_20	
F10	24	IO_L3N_24	F10	IO_L3N_24	F10	IO_L3N_24	
F11	24	IO_L2N_24	F11	IO_L2N_24	F11	IO_L2N_24	
F12	24	IO_L2P_24	F12	IO_L2P_24	F12	IO_L2P_24	
F13	1	VCCO_1	F13	VCCO_1	F13	VCCO_1	
F14	24	IO_L13P_24	F14	IO_L13P_24	F14	IO_L13P_24	
F15	24	IO_L19N_24	F15	IO_L19N_24	F15	IO_L19N_24	
F16	5	IO_L3P_5	F16	IO_L3P_5	F16	IO_L3P_5	
F17	5	IO_L3N_5	F17	IO_L3N_5	F17	IO_L3N_5	
F18	NA	GND	F18	GND	F18	GND	
F19	7	IO_L16P_7	F19	IO_L16P_7	F19	IO_L16P_7	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
F20	7	IO_L14N_VREF_7	F20	IO_L14N_VREF_7	F20	IO_L14N_VREF_7	
F21	7	IO_L9N_CC_7	F21	IO_L9N_CC_7	F21	IO_L9N_CC_7	
F22	7	IO_L8P_CC_7	F22	IO_L8P_CC_7	F22	IO_L8P_CC_7	
F23	5	VCCO_5	F23	VCCO_5	F23	VCCO_5	
F24	7	IO_L11P_CC_7	F24	IO_L11P_CC_7	F24	IO_L11P_CC_7	
F25	7	IO_L17N_7	F25	IO_L17N_7	F25	IO_L17N_7	
F26	7	IO_L17P_7	F26	IO_L17P_7	F26	IO_L17P_7	
F27	5	IO_L13N_5	F27	IO_L13N_5	F27	IO_L13N_5	
F28	NA	GND	F28	GND	F28	GND	
F29	5	IO_L17N_5	F29	IO_L17N_5	F29	IO_L17N_5	
F30	NA	GND	F30	UNUSED	F30	UNUSED	NC
F31	23	IO_L10P_CC_23	F31	IO_L10P_CC_23	F31	IO_L10P_CC_23	
F32	23	IO_L10N_CC_23	F32	IO_L10N_CC_23	F32	IO_L10N_CC_23	
F33	27	VCCO_27	F33	VCCO_27	F33	VCCO_27	
F34	23	IO_L9N_CC_23	F34	IO_L9N_CC_23	F34	IO_L9N_CC_23	
F35	23	IO_L8P_CC_23	F35	IO_L8P_CC_23	F35	IO_L8P_CC_23	
F36	19	IO_L13P_19	F36	IO_L13P_19	F36	IO_L13P_19	
F37	19	IO_L14P_19	F37	IO_L14P_19	F37	IO_L14P_19	
F38	NA	GND	F38	GND	F38	GND	
F39	15	IO_L2P_15	F39	IO_L2P_15	F39	IO_L2P_15	
F40	15	IO_L2N_15	F40	IO_L2N_15	F40	IO_L2N_15	
F41	11	IO_L1P_11	F41	IO_L1P_11	F41	IO_L1P_11	
F42	11	IO_L0P_11	F42	IO_L0P_11	F42	IO_L0P_11	
G1	NA	MGTRXN1_120	G1	MGTRXN1_120	G1	MGTRXN1_120	
G2	NA	GND	G2	GND	G2	GND	
G3	NA	MGTAVCC_120	G3	MGTAVCC_120	G3	MGTAVCC_120	
G4	NA	MGTAVCC_120	G4	MGTAVCC_120	G4	MGTAVCC_120	
G5	NA	GND	G5	GND	G5	GND	
G6	12	IO_L1P_12	G6	IO_L1P_12	G6	IO_L1P_12	
G7	20	IO_L10P_CC_20	G7	IO_L10P_CC_20	G7	IO_L10P_CC_20	
G8	20	IO_L10N_CC_20	G8	IO_L10N_CC_20	G8	IO_L10N_CC_20	
G9	20	IO_L9N_CC_20	G9	IO_L9N_CC_20	G9	IO_L9N_CC_20	
G10	24	VCCO_24	G10	VCCO_24	G10	VCCO_24	
G11	24	IO_L1N_24	G11	IO_L1N_24	G11	IO_L1N_24	
G12	24	IO_L1P_24	G12	IO_L1P_24	G12	IO_L1P_24	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
G13	24	IO_L11P_CC_24	G13	IO_L11P_CC_24	G13	IO_L11P_CC_24	
G14	24	IO_L11N_CC_24	G14	IO_L11N_CC_24	G14	IO_L11N_CC_24	
G15	NA	GND	G15	GND	G15	GND	
G16	5	IO_L5P_5	G16	IO_L5P_5	G16	IO_L5P_5	
G17	5	IO_L7N_5	G17	IO_L7N_5	G17	IO_L7N_5	
G18	5	IO_L7P_5	G18	IO_L7P_5	G18	IO_L7P_5	
G19	7	IO_L16N_7	G19	IO_L16N_7	G19	IO_L16N_7	
G20	7	VCCO_7	G20	VCCO_7	G20	VCCO_7	
G21	7	IO_L9P_CC_7	G21	IO_L9P_CC_7	G21	IO_L9P_CC_7	
G22	7	IO_L8N_CC_7	G22	IO_L8N_CC_7	G22	IO_L8N_CC_7	
G23	7	IO_L11N_CC_7	G23	IO_L11N_CC_7	G23	IO_L11N_CC_7	
G24	7	IO_L15P_7	G24	IO_L15P_7	G24	IO_L15P_7	
G25	NA	GND	G25	GND	G25	GND	
G26	7	IO_L19N_7	G26	IO_L19N_7	G26	IO_L19N_7	
G27	5	IO_L13P_5	G27	IO_L13P_5	G27	IO_L13P_5	
G28	5	IO_L15P_5	G28	IO_L15P_5	G28	IO_L15P_5	
G29	5	IO_L17P_5	G29	IO_L17P_5	G29	IO_L17P_5	
G30	NA	GND	G30	UNUSED	G30	UNUSED	NC
G31	23	IO_L6N_23	G31	IO_L6N_23	G31	IO_L6N_23	
G32	23	IO_L6P_23	G32	IO_L6P_23	G32	IO_L6P_23	
G33	23	IO_L5P_23	G33	IO_L5P_23	G33	IO_L5P_23	
G34	23	IO_L4N_VREF_23	G34	IO_L4N_VREF_23	G34	IO_L4N_VREF_23	
G35	NA	GND	G35	GND	G35	GND	
G36	19	IO_L13N_19	G36	IO_L13N_19	G36	IO_L13N_19	
G37	19	IO_L12N_VRP_19	G37	IO_L12N_VRP_19	G37	IO_L12N_VRP_19	
G38	15	IO_L1P_15	G38	IO_L1P_15	G38	IO_L1P_15	
G39	15	IO_L1N_15	G39	IO_L1N_15	G39	IO_L1N_15	
G40	19	VCCO_19	G40	VCCO_19	G40	VCCO_19	
G41	11	IO_L1N_11	G41	IO_L1N_11	G41	IO_L1N_11	
G42	11	IO_L0N_11	G42	IO_L0N_11	G42	IO_L0N_11	
H1	NA	MGTRXP1_120	H1	MGTRXP1_120	H1	MGTRXP1_120	
H2	NA	MGTTXN1_120	H2	MGTTXN1_120	H2	MGTTXN1_120	
H3	NA	MGTAVCCPLL_120	H3	MGTAVCCPLL_120	H3	MGTAVCCPLL_120	
H4	NA	GND	H4	GND	H4	GND	
H5	12	IO_L1N_12	H5	IO_L1N_12	H5	IO_L1N_12	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
H6	12	IO_L3P_12	H6	IO_L3P_12	H6	IO_L3P_12	
H7	24	VCCO_24	H7	VCCO_24	H7	VCCO_24	
H8	20	IO_L12P_VRN_20	H8	IO_L12P_VRN_20	H8	IO_L12P_VRN_20	
H9	20	IO_L12N_VRP_20	H9	IO_L12N_VRP_20	H9	IO_L12N_VRP_20	
H10	24	IO_L7P_24	H10	IO_L7P_24	H10	IO_L7P_24	
H11	24	IO_L0N_24	H11	IO_L0N_24	H11	IO_L0N_24	
H12	NA	GND	H12	GND	H12	GND	
H13	24	IO_L6N_24	H13	IO_L6N_24	H13	IO_L6N_24	
H14	24	IO_L8P_CC_24	H14	IO_L8P_CC_24	H14	IO_L8P_CC_24	
H15	24	IO_L8N_CC_24	H15	IO_L8N_CC_24	H15	IO_L8N_CC_24	
H16	5	IO_L5N_5	H16	IO_L5N_5	H16	IO_L5N_5	
H17	7	VCCO_7	H17	VCCO_7	H17	VCCO_7	
H18	5	IO_L9N_CC_5	H18	IO_L9N_CC_5	H18	IO_L9N_CC_5	
H19	7	IO_L18P_7	H19	IO_L18P_7	H19	IO_L18P_7	
H20	7	IO_L18N_7	H20	IO_L18N_7	H20	IO_L18N_7	
H21	7	IO_L4P_7	H21	IO_L4P_7	H21	IO_L4P_7	
H22	NA	GND	H22	GND	H22	GND	
H23	7	IO_L13N_7	H23	IO_L13N_7	H23	IO_L13N_7	
H24	7	IO_L15N_7	H24	IO_L15N_7	H24	IO_L15N_7	
H25	7	IO_L19P_7	H25	IO_L19P_7	H25	IO_L19P_7	
H26	5	IO_L6P_5	H26	IO_L6P_5	H26	IO_L6P_5	
H27	3	VCCO_3	H27	VCCO_3	H27	VCCO_3	
H28	5	IO_L15N_5	H28	IO_L15N_5	H28	IO_L15N_5	
H29	5	IO_L19P_5	H29	IO_L19P_5	H29	IO_L19P_5	
H30	5	IO_L19N_5	H30	IO_L19N_5	H30	IO_L19N_5	
H31	23	IO_L7P_23	H31	IO_L7P_23	H31	IO_L7P_23	
H32	NA	GND	H32	GND	H32	GND	
H33	23	IO_L5N_23	H33	IO_L5N_23	H33	IO_L5N_23	
H34	23	IO_L4P_23	H34	IO_L4P_23	H34	IO_L4P_23	
H35	19	IO_L6P_19	H35	IO_L6P_19	H35	IO_L6P_19	
H36	19	IO_L12P_VRN_19	H36	IO_L12P_VRN_19	H36	IO_L12P_VRN_19	
H37	23	VCCO_23	H37	VCCO_23	H37	VCCO_23	
H38	15	IO_L0P_15	H38	IO_L0P_15	H38	IO_L0P_15	
H39	15	IO_L0N_15	H39	IO_L0N_15	H39	IO_L0N_15	
H40	15	IO_L10P_CC_15	H40	IO_L10P_CC_15	H40	IO_L10P_CC_15	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
H41	11	IO_L2P_11	H41	IO_L2P_11	H41	IO_L2P_11	
H42	NA	GND	H42	GND	H42	GND	
J1	NA	GND	J1	UNPOPULATED	J1	GND	
J2	NA	MGTTXP1_120	J2	MGTTXP1_120	J2	MGTTXP1_120	
J3	NA	MGTAVTTTX_120	J3	MGTAVTTTX_120	J3	MGTAVTTTX_120	
J4	NA	GND	J4	GND	J4	GND	
J5	12	IO_L3N_12	J5	IO_L3N_12	J5	IO_L3N_12	
J6	12	IO_L5P_12	J6	IO_L5P_12	J6	IO_L5P_12	
J7	20	IO_L14N_VREF_20	J7	IO_L14N_VREF_20	J7	IO_L14N_VREF_20	
J8	20	IO_L14P_20	J8	IO_L14P_20	J8	IO_L14P_20	
J9	NA	GND	J9	GND	J9	GND	
J10	24	IO_L7N_24	J10	IO_L7N_24	J10	IO_L7N_24	
J11	24	IO_L5N_24	J11	IO_L5N_24	J11	IO_L5N_24	
J12	24	IO_L0P_24	J12	IO_L0P_24	J12	IO_L0P_24	
J13	24	IO_L6P_24	J13	IO_L6P_24	J13	IO_L6P_24	
J14	1	VCCO_1	J14	VCCO_1	J14	VCCO_1	
J15	3	IO_L0N_CC_GC_3	J15	IO_L0N_CC_GC_3	J15	IO_L0N_CC_GC_3	
J16	3	IO_L0P_CC_GC_3	J16	IO_L0P_CC_GC_3	J16	IO_L0P_CC_GC_3	
J17	3	IO_L2P_GC_VRN_3	J17	IO_L2P_GC_VRN_3	J17	IO_L2P_GC_VRN_3	
J18	5	IO_L9P_CC_5	J18	IO_L9P_CC_5	J18	IO_L9P_CC_5	
J19	NA	GND	J19	GND	J19	GND	
J20	7	IO_L5P_7	J20	IO_L5P_7	J20	IO_L5P_7	
J21	7	IO_L4N_VREF_7	J21	IO_L4N_VREF_7	J21	IO_L4N_VREF_7	
J22	7	IO_L7N_7	J22	IO_L7N_7	J22	IO_L7N_7	
J23	7	IO_L13P_7	J23	IO_L13P_7	J23	IO_L13P_7	
J24	NA	GND	J24	GND	J24	GND	
J25	5	IO_L4N_VREF_5	J25	IO_L4N_VREF_5	J25	IO_L4N_VREF_5	
J26	5	IO_L6N_5	J26	IO_L6N_5	J26	IO_L6N_5	
J27	5	IO_L8N_CC_5	J27	IO_L8N_CC_5	J27	IO_L8N_CC_5	
J28	5	IO_L8P_CC_5	J28	IO_L8P_CC_5	J28	IO_L8P_CC_5	
J29	NA	GND	J29	GND	J29	GND	
J30	3	IO_L7N_GC_3	J30	IO_L7N_GC_3	J30	IO_L7N_GC_3	
J31	23	IO_L7N_23	J31	IO_L7N_23	J31	IO_L7N_23	
J32	23	IO_L14N_VREF_23	J32	IO_L14N_VREF_23	J32	IO_L14N_VREF_23	
J33	23	IO_L13N_23	J33	IO_L13N_23	J33	IO_L13N_23	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
J34	27	VCCO_27	J34	VCCO_27	J34	VCCO_27	
J35	19	IO_L5N_19	J35	IO_L5N_19	J35	IO_L5N_19	
J36	19	IO_L6N_19	J36	IO_L6N_19	J36	IO_L6N_19	
J37	19	IO_L7N_19	J37	IO_L7N_19	J37	IO_L7N_19	
J38	15	IO_L9N_CC_15	J38	IO_L9N_CC_15	J38	IO_L9N_CC_15	
J39	NA	GND	J39	GND	J39	GND	
J40	15	IO_L10N_CC_15	J40	IO_L10N_CC_15	J40	IO_L10N_CC_15	
J41	11	IO_L2N_11	J41	IO_L2N_11	J41	IO_L2N_11	
J42	11	IO_L3P_11	J42	IO_L3P_11	J42	IO_L3P_11	
K1	NA	GND	K1	UNPOPULATED	K1	GND	
K2	NA	MGTTXP0_116	K2	MGTTXP0_116	K2	MGTTXP0_116	
K3	NA	MGTAVTTTX_116	K3	MGTAVTTTX_116	K3	MGTAVTTTX_116	
K4	12	IO_L7P_12	K4	IO_L7P_12	K4	IO_L7P_12	
K5	12	IO_L5N_12	K5	IO_L5N_12	K5	IO_L5N_12	
K6	NA	GND	K6	GND	K6	GND	
K7	20	IO_L17P_20	K7	IO_L17P_20	K7	IO_L17P_20	
K8	20	IO_L16P_20	K8	IO_L16P_20	K8	IO_L16P_20	
K9	20	IO_L16N_20	K9	IO_L16N_20	K9	IO_L16N_20	
K10	24	IO_L9P_CC_24	K10	IO_L9P_CC_24	K10	IO_L9P_CC_24	
K11	NA	GND	K11	GND	K11	GND	
K12	24	IO_L5P_24	K12	IO_L5P_24	K12	IO_L5P_24	
K13	24	IO_L4N_VREF_24	K13	IO_L4N_VREF_24	K13	IO_L4N_VREF_24	
K14	24	IO_L4P_24	K14	IO_L4P_24	K14	IO_L4P_24	
K15	3	IO_L8N_GC_3	K15	IO_L8N_GC_3	K15	IO_L8N_GC_3	
K16	NA	GND	K16	GND	K16	GND	
K17	3	IO_L2N_GC_VRP_3	K17	IO_L2N_GC_VRP_3	K17	IO_L2N_GC_VRP_3	
K18	5	IO_L10P_CC_5	K18	IO_L10P_CC_5	K18	IO_L10P_CC_5	
K19	5	IO_L10N_CC_5	K19	IO_L10N_CC_5	K19	IO_L10N_CC_5	
K20	7	IO_L5N_7	K20	IO_L5N_7	K20	IO_L5N_7	
K21	NA	GND	K21	GND	K21	GND	
K22	7	IO_L7P_7	K22	IO_L7P_7	K22	IO_L7P_7	
K23	7	IO_L6N_7	K23	IO_L6N_7	K23	IO_L6N_7	
K24	5	IO_L2P_5	K24	IO_L2P_5	K24	IO_L2P_5	
K25	5	IO_L4P_5	K25	IO_L4P_5	K25	IO_L4P_5	
K26	NA	GND	K26	GND	K26	GND	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
K27	5	IO_L11P_CC_5	K27	IO_L11P_CC_5	K27	IO_L11P_CC_5	
K28	3	IO_L5N_GC_3	K28	IO_L5N_GC_3	K28	IO_L5N_GC_3	
K29	3	IO_L7P_GC_3	K29	IO_L7P_GC_3	K29	IO_L7P_GC_3	
K30	3	IO_L9P_GC_3	K30	IO_L9P_GC_3	K30	IO_L9P_GC_3	
K31	NA	GND	K31	GND	K31	GND	
K32	23	IO_L14P_23	K32	IO_L14P_23	K32	IO_L14P_23	
K33	23	IO_L13P_23	K33	IO_L13P_23	K33	IO_L13P_23	
K34	23	IO_L12N_VRP_23	K34	IO_L12N_VRP_23	K34	IO_L12N_VRP_23	
K35	19	IO_L5P_19	K35	IO_L5P_19	K35	IO_L5P_19	
K36	NA	GND	K36	GND	K36	GND	
K37	19	IO_L7P_19	K37	IO_L7P_19	K37	IO_L7P_19	
K38	15	IO_L9P_CC_15	K38	IO_L9P_CC_15	K38	IO_L9P_CC_15	
K39	15	IO_L11N_CC_15	K39	IO_L11N_CC_15	K39	IO_L11N_CC_15	
K40	15	IO_L11P_CC_15	K40	IO_L11P_CC_15	K40	IO_L11P_CC_15	
K41	19	VCCO_19	K41	VCCO_19	K41	VCCO_19	
K42	11	IO_L3N_11	K42	IO_L3N_11	K42	IO_L3N_11	
L1	NA	MGTRXP0_116	L1	MGTRXP0_116	L1	MGTRXP0_116	
L2	NA	MGTTXN0_116	L2	MGTTXN0_116	L2	MGTTXN0_116	
L3	NA	MGTAVTTRX_116	L3	MGTAVTTRX_116	L3	MGTAVTTRX_116	
L4	NA	GND	L4	GND	L4	GND	
L5	12	IO_L7N_12	L5	IO_L7N_12	L5	IO_L7N_12	
L6	12	IO_L9P_CC_12	L6	IO_L9P_CC_12	L6	IO_L9P_CC_12	
L7	20	IO_L17N_20	L7	IO_L17N_20	L7	IO_L17N_20	
L8	20	VCCO_20	L8	VCCO_20	L8	VCCO_20	
L9	20	IO_L19N_20	L9	IO_L19N_20	L9	IO_L19N_20	
L10	24	IO_L9N_CC_24	L10	IO_L9N_CC_24	L10	IO_L9N_CC_24	
L11	24	IO_L10N_CC_24	L11	IO_L10N_CC_24	L11	IO_L10N_CC_24	
L12	24	IO_L10P_CC_24	L12	IO_L10P_CC_24	L12	IO_L10P_CC_24	
L13	NA	GND	L13	GND	L13	GND	
L14	3	IO_L8P_GC_3	L14	IO_L8P_GC_3	L14	IO_L8P_GC_3	
L15	3	IO_L6N_GC_3	L15	IO_L6N_GC_3	L15	IO_L6N_GC_3	
L16	3	IO_L6P_GC_3	L16	IO_L6P_GC_3	L16	IO_L6P_GC_3	
L17	3	IO_L4P_GC_3	L17	IO_L4P_GC_3	L17	IO_L4P_GC_3	
L18	NA	GND	L18	GND	L18	GND	
L19	5	IO_L18N_5	L19	IO_L18N_5	L19	IO_L18N_5	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
L20	5	IO_L18P_5	L20	IO_L18P_5	L20	IO_L18P_5	
L21	7	IO_L1N_7	L21	IO_L1N_7	L21	IO_L1N_7	
L22	7	IO_L6P_7	L22	IO_L6P_7	L22	IO_L6P_7	
L23	NA	GND	L23	GND	L23	GND	
L24	5	IO_L0P_5	L24	IO_L0P_5	L24	IO_L0P_5	
L25	5	IO_L2N_5	L25	IO_L2N_5	L25	IO_L2N_5	
L26	5	IO_L11N_CC_5	L26	IO_L11N_CC_5	L26	IO_L11N_CC_5	
L27	3	IO_L1N_CC_GC_3	L27	IO_L1N_CC_GC_3	L27	IO_L1N_CC_GC_3	
L28	NA	GND	L28	GND	L28	GND	
L29	3	IO_L5P_GC_3	L29	IO_L5P_GC_3	L29	IO_L5P_GC_3	
L30	3	IO_L9N_GC_3	L30	IO_L9N_GC_3	L30	IO_L9N_GC_3	
L31	23	IO_L15N_23	L31	IO_L15N_23	L31	IO_L15N_23	
L32	23	IO_L15P_23	L32	IO_L15P_23	L32	IO_L15P_23	
L33	NA	GND	L33	GND	L33	GND	
L34	23	IO_L12P_VRN_23	L34	IO_L12P_VRN_23	L34	IO_L12P_VRN_23	
L35	19	IO_L4N_VREF_19	L35	IO_L4N_VREF_19	L35	IO_L4N_VREF_19	
L36	19	IO_L4P_19	L36	IO_L4P_19	L36	IO_L4P_19	
L37	19	IO_L2P_19	L37	IO_L2P_19	L37	IO_L2P_19	
L38	19	VCCO_19	L38	VCCO_19	L38	VCCO_19	
L39	15	IO_L8N_CC_15	L39	IO_L8N_CC_15	L39	IO_L8N_CC_15	
L40	11	IO_L4P_11	L40	IO_L4P_11	L40	IO_L4P_11	
L41	11	IO_L4N_VREF_11	L41	IO_L4N_VREF_11	L41	IO_L4N_VREF_11	
L42	11	IO_L5P_11	L42	IO_L5P_11	L42	IO_L5P_11	
M1	NA	MGTRXN0_116	M1	MGTRXN0_116	M1	MGTRXN0_116	
M2	NA	GND	M2	GND	M2	GND	
M3	NA	MGTREFCLKN_116	M3	MGTREFCLKN_116	M3	MGTREFCLKN_116	
M4	NA	MGTREFCLKP_116	M4	MGTREFCLKP_116	M4	MGTREFCLKP_116	
M5	NA	GND	M5	GND	M5	GND	
M6	12	IO_L9N_CC_12	M6	IO_L9N_CC_12	M6	IO_L9N_CC_12	
M7	20	IO_L18P_20	M7	IO_L18P_20	M7	IO_L18P_20	
M8	20	IO_L18N_20	M8	IO_L18N_20	M8	IO_L18N_20	
M9	20	IO_L19P_20	M9	IO_L19P_20	M9	IO_L19P_20	
M10	NA	GND	M10	GND	M10	GND	
M11	24	IO_L12P_VRN_24	M11	IO_L12P_VRN_24	M11	IO_L12P_VRN_24	
M12	24	IO_L12N_VRP_24	M12	IO_L12N_VRP_24	M12	IO_L12N_VRP_24	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
M13	1	IO_L7N_A4_D20_1	M13	IO_L7N_A4_D20_1	M13	IO_L7N_A4_D20_1	
M14	1	IO_L7P_A5_D21_1	M14	IO_L7P_A5_D21_1	M14	IO_L7P_A5_D21_1	
M15	NA	GND	M15	GND	M15	GND	
M16	1	IO_L3P_A13_D29_1	M16	IO_L3P_A13_D29_1	M16	IO_L3P_A13_D29_1	
M17	3	IO_L4N_GC_VREF_3	M17	IO_L4N_GC_VREF_3	M17	IO_L4N_GC_VREF_3	
M18	5	IO_L16P_5	M18	IO_L16P_5	M18	IO_L16P_5	
M19	5	IO_L14P_5	M19	IO_L14P_5	M19	IO_L14P_5	
M20	NA	GND	M20	GND	M20	GND	
M21	7	IO_L1P_7	M21	IO_L1P_7	M21	IO_L1P_7	
M22	7	IO_L0N_7	M22	IO_L0N_7	M22	IO_L0N_7	
M23	7	IO_L0P_7	M23	IO_L0P_7	M23	IO_L0P_7	
M24	5	IO_L0N_5	M24	IO_L0N_5	M24	IO_L0N_5	
M25	NA	GND	M25	GND	M25	GND	
M26	3	IO_L1P_CC_GC_3	M26	IO_L1P_CC_GC_3	M26	IO_L1P_CC_GC_3	
M27	3	IO_L3P_GC_3	M27	IO_L3P_GC_3	M27	IO_L3P_GC_3	
M28	3	IO_L3N_GC_3	M28	IO_L3N_GC_3	M28	IO_L3N_GC_3	
M29	1	IO_L8N_CC_A2_D18_1	M29	IO_L8N_CC_A2_D18_1	M29	IO_L8N_CC_A2_D18_1	
M30	NA	GND	M30	GND	M30	GND	
M31	23	IO_L2N_23	M31	IO_L2N_23	M31	IO_L2N_23	
M32	23	IO_L2P_23	M32	IO_L2P_23	M32	IO_L2P_23	
M33	23	IO_L1N_23	M33	IO_L1N_23	M33	IO_L1N_23	
M34	23	IO_L1P_23	M34	IO_L1P_23	M34	IO_L1P_23	
M35	NA	GND	M35	GND	M35	GND	
M36	19	IO_L1N_19	M36	IO_L1N_19	M36	IO_L1N_19	
M37	19	IO_L2N_19	M37	IO_L2N_19	M37	IO_L2N_19	
M38	15	IO_L8P_CC_15	M38	IO_L8P_CC_15	M38	IO_L8P_CC_15	
M39	15	IO_L7N_15	M39	IO_L7N_15	M39	IO_L7N_15	
M40	NA	GND	M40	GND	M40	GND	
M41	11	IO_L5N_11	M41	IO_L5N_11	M41	IO_L5N_11	
M42	11	IO_L6P_11	M42	IO_L6P_11	M42	IO_L6P_11	
N1	NA	MGTRXN1_116	N1	MGTRXN1_116	N1	MGTRXN1_116	
N2	NA	GND	N2	GND	N2	GND	
N3	NA	MGTAVCC_116	N3	MGTAVCC_116	N3	MGTAVCC_116	
N4	NA	MGTAVCC_116	N4	MGTAVCC_116	N4	MGTAVCC_116	
N5	12	IO_L10P_CC_12	N5	IO_L10P_CC_12	N5	IO_L10P_CC_12	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
N6	12	IO_L10N_CC_12	N6	IO_L10N_CC_12	N6	IO_L10N_CC_12	
N7	NA	GND	N7	GND	N7	GND	
N8	20	IO_L0N_20	N8	IO_L0N_20	N8	IO_L0N_20	
N9	20	IO_L0P_20	N9	IO_L0P_20	N9	IO_L0P_20	
N10	24	IO_L16N_24	N10	IO_L16N_24	N10	IO_L16N_24	
N11	24	IO_L14P_24	N11	IO_L14P_24	N11	IO_L14P_24	
N12	NA	GND	N12	GND	N12	GND	
N13	1	IO_L9P_CC_A1_D17_1	N13	IO_L9P_CC_A1_D17_1	N13	IO_L9P_CC_A1_D17_1	
N14	1	IO_L5N_A8_D24_1	N14	IO_L5N_A8_D24_1	N14	IO_L5N_A8_D24_1	
N15	1	IO_L5P_A9_D25_1	N15	IO_L5P_A9_D25_1	N15	IO_L5P_A9_D25_1	
N16	1	IO_L3N_A12_D28_1	N16	IO_L3N_A12_D28_1	N16	IO_L3N_A12_D28_1	
N17	NA	GND	N17	GND	N17	GND	
N18	5	IO_L16N_5	N18	IO_L16N_5	N18	IO_L16N_5	
N19	5	IO_L14N_VREF_5	N19	IO_L14N_VREF_5	N19	IO_L14N_VREF_5	
N20	5	IO_L12P_VRN_5	N20	IO_L12P_VRN_5	N20	IO_L12P_VRN_5	
N21	7	IO_L3N_7	N21	IO_L3N_7	N21	IO_L3N_7	
N22	7	IO_L3P_7	N22	IO_L3P_7	N22	IO_L3P_7	
N23	7	IO_L2N_7	N23	IO_L2N_7	N23	IO_L2N_7	
N24	7	IO_L2P_7	N24	IO_L2P_7	N24	IO_L2P_7	
N25	1	IO_L0P_A19_1	N25	IO_L0P_A19_1	N25	IO_L0P_A19_1	
N26	1	IO_L2N_A14_D30_1	N26	IO_L2N_A14_D30_1	N26	IO_L2N_A14_D30_1	
N27	NA	GND	N27	GND	N27	GND	
N28	1	IO_L6P_A7_D23_1	N28	IO_L6P_A7_D23_1	N28	IO_L6P_A7_D23_1	
N29	1	IO_L6N_A6_D22_1	N29	IO_L6N_A6_D22_1	N29	IO_L6N_A6_D22_1	
N30	1	IO_L8P_CC_A3_D19_1	N30	IO_L8P_CC_A3_D19_1	N30	IO_L8P_CC_A3_D19_1	
N31	23	IO_L3P_23	N31	IO_L3P_23	N31	IO_L3P_23	
N32	NA	GND	N32	GND	N32	GND	
N33	23	IO_L0P_23	N33	IO_L0P_23	N33	IO_L0P_23	
N34	23	IO_L0N_23	N34	IO_L0N_23	N34	IO_L0N_23	
N35	19	IO_L1P_19	N35	IO_L1P_19	N35	IO_L1P_19	
N36	19	IO_L3P_19	N36	IO_L3P_19	N36	IO_L3P_19	
N37	NA	GND	N37	GND	N37	GND	
N38	15	IO_L6N_15	N38	IO_L6N_15	N38	IO_L6N_15	
N39	15	IO_L7P_15	N39	IO_L7P_15	N39	IO_L7P_15	
N40	11	IO_L7P_11	N40	IO_L7P_11	N40	IO_L7P_11	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
N41	11	IO_L6N_11	N41	IO_L6N_11	N41	IO_L6N_11	
N42	NA	GND	N42	GND	N42	GND	
P1	NA	MGTRXP1_116	P1	MGTRXP1_116	P1	MGTRXP1_116	
P2	NA	MGTTXN1_116	P2	MGTTXN1_116	P2	MGTTXN1_116	
P3	NA	MGTAVCCPLL_116	P3	MGTAVCCPLL_116	P3	MGTAVCCPLL_116	
P4	NA	GND	P4	GND	P4	GND	
P5	12	IO_L12P_VRN_12	P5	IO_L12P_VRN_12	P5	IO_L12P_VRN_12	
P6	12	IO_L12N_VRP_12	P6	IO_L12N_VRP_12	P6	IO_L12N_VRP_12	
P7	20	IO_L2P_20	P7	IO_L2P_20	P7	IO_L2P_20	
P8	20	IO_L2N_20	P8	IO_L2N_20	P8	IO_L2N_20	
P9	20	VCCO_20	P9	VCCO_20	P9	VCCO_20	
P10	24	IO_L18N_24	P10	IO_L18N_24	P10	IO_L18N_24	
P11	24	IO_L16P_24	P11	IO_L16P_24	P11	IO_L16P_24	
P12	24	IO_L14N_VREF_24	P12	IO_L14N_VREF_24	P12	IO_L14N_VREF_24	
P13	1	IO_L9N_CC_A0_D16_1	P13	IO_L9N_CC_A0_D16_1	P13	IO_L9N_CC_A0_D16_1	
P14	NA	GND	P14	GND	P14	GND	
P15	0	HSWAPEN_0	P15	HSWAPEN_0	P15	HSWAPEN_0	
P16	NA	GND	P16	GND	P16	GND	
P17	1	IO_L1N_A16_1	P17	IO_L1N_A16_1	P17	IO_L1N_A16_1	
P18	1	IO_L1P_A17_1	P18	IO_L1P_A17_1	P18	IO_L1P_A17_1	
P19	NA	GND	P19	GND	P19	GND	
P20	5	IO_L12N_VRP_5	P20	IO_L12N_VRP_5	P20	IO_L12N_VRP_5	
P21	NA	VCCINT	P21	VCCINT	P21	VCCINT	
P22	NA	GND	P22	GND	P22	GND	
P23	NA	VCCINT	P23	VCCINT	P23	VCCINT	
P24	NA	GND	P24	GND	P24	GND	
P25	1	IO_L0N_A18_1	P25	IO_L0N_A18_1	P25	IO_L0N_A18_1	
P26	1	IO_L2P_A15_D31_1	P26	IO_L2P_A15_D31_1	P26	IO_L2P_A15_D31_1	
P27	1	IO_L4P_A11_D27_1	P27	IO_L4P_A11_D27_1	P27	IO_L4P_A11_D27_1	
P28	1	IO_L4N_VREF_A10_D26_1	P28	IO_L4N_VREF_A10_D26_1	P28	IO_L4N_VREF_A10_D26_1	
P29	NA	GND	P29	GND	P29	GND	
P30	0	VBATT_0	P30	VBATT_0	P30	VBATT_0	
P31	23	IO_L3N_23	P31	IO_L3N_23	P31	IO_L3N_23	
P32	23	IO_L16N_23	P32	IO_L16N_23	P32	IO_L16N_23	
P33	23	IO_L16P_23	P33	IO_L16P_23	P33	IO_L16P_23	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
P34	NA	GND	P34	GND	P34	GND	
P35	19	IO_L0N_19	P35	IO_L0N_19	P35	IO_L0N_19	
P36	19	IO_L3N_19	P36	IO_L3N_19	P36	IO_L3N_19	
P37	15	IO_L5N_15	P37	IO_L5N_15	P37	IO_L5N_15	
P38	15	IO_L6P_15	P38	IO_L6P_15	P38	IO_L6P_15	
P39	15	VCCO_15	P39	VCCO_15	P39	VCCO_15	
P40	11	IO_L7N_11	P40	IO_L7N_11	P40	IO_L7N_11	
P41	11	IO_L13P_11	P41	IO_L13P_11	P41	IO_L13P_11	
P42	11	IO_L12N_VRP_11	P42	IO_L12N_VRP_11	P42	IO_L12N_VRP_11	
R1	NA	GND	R1	UNPOPULATED	R1	GND	
R2	NA	MGTTXP1_116	R2	MGTTXP1_116	R2	MGTTXP1_116	
R3	NA	MGTAVTTTX_116	R3	MGTAVTTTX_116	R3	MGTAVTTTX_116	
R4	12	IO_L14P_12	R4	IO_L14P_12	R4	IO_L14P_12	
R5	12	IO_L14N_VREF_12	R5	IO_L14N_VREF_12	R5	IO_L14N_VREF_12	
R6	20	VCCO_20	R6	VCCO_20	R6	VCCO_20	
R7	20	IO_L4P_20	R7	IO_L4P_20	R7	IO_L4P_20	
R8	20	IO_L4N_VREF_20	R8	IO_L4N_VREF_20	R8	IO_L4N_VREF_20	
R9	20	IO_L6P_20	R9	IO_L6P_20	R9	IO_L6P_20	
R10	24	IO_L18P_24	R10	IO_L18P_24	R10	IO_L18P_24	
R11	NA	GND	R11	GND	R11	GND	
R12	NA	VCCAUX	R12	VCCAUX	R12	VCCAUX	
R13	NA	GND	R13	GND	R13	GND	
R14	0	DONE_0	R14	DONE_0	R14	DONE_0	
R15	0	D_IN_0	R15	D_IN_0	R15	D_IN_0	
R16	NA	VCCINT	R16	VCCINT	R16	VCCINT	
R17	NA	GND	R17	GND	R17	GND	
R18	NA	VCCINT	R18	VCCINT	R18	VCCINT	
R19	NA	GND	R19	GND	R19	GND	
R20	NA	VCCINT	R20	VCCINT	R20	VCCINT	
R21	NA	GND	R21	GND	R21	GND	
R22	NA	VCCINT	R22	VCCINT	R22	VCCINT	
R23	NA	GND	R23	GND	R23	GND	
R24	NA	VCCINT	R24	VCCINT	R24	VCCINT	
R25	NA	GND	R25	GND	R25	GND	
R26	NA	VCCINT	R26	VCCINT	R26	VCCINT	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
R27	NA	GND	R27	GND	R27	GND	
R28	NA	VCCINT	R28	VCCINT	R28	VCCINT	
R29	0	PROGRAM_B_0	R29	PROGRAM_B_0	R29	PROGRAM_B_0	
R30	0	RDWR_B_0	R30	RDWR_B_0	R30	RDWR_B_0	
R31	NA	GND	R31	GND	R31	GND	
R32	23	IO_L17N_23	R32	IO_L17N_23	R32	IO_L17N_23	
R33	23	IO_L17P_23	R33	IO_L17P_23	R33	IO_L17P_23	
R34	19	IO_L0P_19	R34	IO_L0P_19	R34	IO_L0P_19	
R35	19	IO_L10P_CC_19	R35	IO_L10P_CC_19	R35	IO_L10P_CC_19	
R36	15	VCCO_15	R36	VCCO_15	R36	VCCO_15	
R37	15	IO_L5P_15	R37	IO_L5P_15	R37	IO_L5P_15	
R38	15	IO_L4N_VREF_15	R38	IO_L4N_VREF_15	R38	IO_L4N_VREF_15	
R39	15	IO_L4P_15	R39	IO_L4P_15	R39	IO_L4P_15	
R40	11	IO_L13N_11	R40	IO_L13N_11	R40	IO_L13N_11	
R41	NA	GND	R41	GND	R41	GND	
R42	11	IO_L12P_VRN_11	R42	IO_L12P_VRN_11	R42	IO_L12P_VRN_11	
T1	NA	GND	T1	UNPOPULATED	T1	GND	
T2	NA	MGTTXP0_112	T2	MGTTXP0_112	T2	MGTTXP0_112	
T3	NA	MGTAVTTTX_112	T3	MGTAVTTTX_112	T3	MGTAVTTTX_112	
T4	12	IO_L15N_12	T4	IO_L15N_12	T4	IO_L15N_12	
T5	12	IO_L15P_12	T5	IO_L15P_12	T5	IO_L15P_12	
T6	12	IO_L13N_12	T6	IO_L13N_12	T6	IO_L13N_12	
T7	12	IO_L13P_12	T7	IO_L13P_12	T7	IO_L13P_12	
T8	NA	GND	T8	GND	T8	GND	
T9	20	IO_L6N_20	T9	IO_L6N_20	T9	IO_L6N_20	
T10	20	IO_L13P_20	T10	IO_L13P_20	T10	IO_L13P_20	
T11	20	IO_L13N_20	T11	IO_L13N_20	T11	IO_L13N_20	
T12	NA	GND	T12	GND	T12	GND	
T13	NA	VCCAUX	T13	VCCAUX	T13	VCCAUX	
T14	0	INIT_B_0	T14	INIT_B_0	T14	INIT_B_0	
T15	NA	VCCINT	T15	VCCINT	T15	VCCINT	
T16	NA	GND	T16	GND	T16	GND	
T17	NA	VCCINT	T17	VCCINT	T17	VCCINT	
T18	NA	GND	T18	GND	T18	GND	
T19	NA	VCCINT	T19	VCCINT	T19	VCCINT	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
T20	NA	GND	T20	GND	T20	GND	
T21	NA	VCCINT	T21	VCCINT	T21	VCCINT	
T22	NA	GND	T22	GND	T22	GND	
T23	NA	VCCINT	T23	VCCINT	T23	VCCINT	
T24	NA	GND	T24	GND	T24	GND	
T25	NA	VCCINT	T25	VCCINT	T25	VCCINT	
T26	NA	GND	T26	GND	T26	GND	
T27	NA	VCCINT	T27	VCCINT	T27	VCCINT	
T28	NA	GND	T28	GND	T28	GND	
T29	NA	VCCAUX	T29	VCCAUX	T29	VCCAUX	
T30	0	CS_B_0	T30	CS_B_0	T30	CS_B_0	
T31	23	IO_L19N_23	T31	IO_L19N_23	T31	IO_L19N_23	
T32	23	IO_L18P_23	T32	IO_L18P_23	T32	IO_L18P_23	
T33	NA	GND	T33	GND	T33	GND	
T34	19	IO_L9P_CC_19	T34	IO_L9P_CC_19	T34	IO_L9P_CC_19	
T35	19	IO_L8N_CC_19	T35	IO_L8N_CC_19	T35	IO_L8N_CC_19	
T36	19	IO_L10N_CC_19	T36	IO_L10N_CC_19	T36	IO_L10N_CC_19	
T37	15	IO_L13P_15	T37	IO_L13P_15	T37	IO_L13P_15	
T38	NA	GND	T38	GND	T38	GND	
T39	15	IO_L14P_15	T39	IO_L14P_15	T39	IO_L14P_15	
T40	11	IO_L14P_11	T40	IO_L14P_11	T40	IO_L14P_11	
T41	11	IO_L14N_VREF_11	T41	IO_L14N_VREF_11	T41	IO_L14N_VREF_11	
T42	11	IO_L15P_SM13P_11	T42	IO_L15P_SM13P_11	T42	IO_L15P_SM13P_11	
U1	NA	MGTRXP0_112	U1	MGTRXP0_112	U1	MGTRXP0_112	
U2	NA	MGTTXN0_112	U2	MGTTXN0_112	U2	MGTTXN0_112	
U3	NA	MGTAVTTRX_112	U3	MGTAVTTRX_112	U3	MGTAVTTRX_112	
U4	NA	GND	U4	GND	U4	GND	
U5	NA	GND	U5	GND	U5	GND	
U6	12	IO_L11N_CC_12	U6	IO_L11N_CC_12	U6	IO_L11N_CC_12	
U7	12	IO_L11P_CC_12	U7	IO_L11P_CC_12	U7	IO_L11P_CC_12	
U8	20	IO_L11P_CC_20	U8	IO_L11P_CC_20	U8	IO_L11P_CC_20	
U9	20	IO_L11N_CC_20	U9	IO_L11N_CC_20	U9	IO_L11N_CC_20	
U10	12	VCCO_12	U10	VCCO_12	U10	VCCO_12	
U11	20	IO_L15P_20	U11	IO_L15P_20	U11	IO_L15P_20	
U12	NA	VCCAUX	U12	VCCAUX	U12	VCCAUX	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
U13	NA	GND	U13	GND	U13	GND	
U14	NA	VCCINT	U14	VCCINT	U14	VCCINT	
U15	NA	GND	U15	GND	U15	GND	
U16	NA	VCCINT	U16	VCCINT	U16	VCCINT	
U17	NA	GND	U17	GND	U17	GND	
U18	NA	VCCINT	U18	VCCINT	U18	VCCINT	
U19	NA	GND	U19	GND	U19	GND	
U20	NA	VCCINT	U20	VCCINT	U20	VCCINT	
U21	NA	GND	U21	GND	U21	GND	
U22	NA	VCCINT	U22	VCCINT	U22	VCCINT	
U23	NA	GND	U23	GND	U23	GND	
U24	NA	VCCINT	U24	VCCINT	U24	VCCINT	
U25	NA	GND	U25	GND	U25	GND	
U26	NA	VCCINT	U26	VCCINT	U26	VCCINT	
U27	NA	GND	U27	GND	U27	GND	
U28	NA	VCCINT	U28	VCCINT	U28	VCCINT	
U29	NA	GND	U29	GND	U29	GND	
U30	NA	VCCAUX	U30	VCCAUX	U30	VCCAUX	
U31	23	IO_L19P_23	U31	IO_L19P_23	U31	IO_L19P_23	
U32	23	IO_L18N_23	U32	IO_L18N_23	U32	IO_L18N_23	
U33	19	IO_L9N_CC_19	U33	IO_L9N_CC_19	U33	IO_L9N_CC_19	
U34	19	IO_L8P_CC_19	U34	IO_L8P_CC_19	U34	IO_L8P_CC_19	
U35	NA	GND	U35	GND	U35	GND	
U36	19	IO_L11P_CC_19	U36	IO_L11P_CC_19	U36	IO_L11P_CC_19	
U37	15	IO_L12N_VRP_15	U37	IO_L12N_VRP_15	U37	IO_L12N_VRP_15	
U38	15	IO_L13N_15	U38	IO_L13N_15	U38	IO_L13N_15	
U39	15	IO_L14N_VREF_15	U39	IO_L14N_VREF_15	U39	IO_L14N_VREF_15	
U40	15	VCCO_15	U40	VCCO_15	U40	VCCO_15	
U41	11	IO_L15N_SM13N_11	U41	IO_L15N_SM13N_11	U41	IO_L15N_SM13N_11	
U42	11	IO_L16P_SM12P_11	U42	IO_L16P_SM12P_11	U42	IO_L16P_SM12P_11	
V1	NA	MGTRXN0_112	V1	MGTRXN0_112	V1	MGTRXN0_112	
V2	NA	GND	V2	GND	V2	GND	
V3	NA	MGTREFCLKN_112	V3	MGTREFCLKN_112	V3	MGTREFCLKN_112	
V4	NA	MGTREFCLKP_112	V4	MGTREFCLKP_112	V4	MGTREFCLKP_112	
V5	12	IO_L8P_CC_12	V5	IO_L8P_CC_12	V5	IO_L8P_CC_12	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
V6	12	IO_L8N_CC_12	V6	IO_L8N_CC_12	V6	IO_L8N_CC_12	
V7	12	VCCO_12	V7	VCCO_12	V7	VCCO_12	
V8	12	IO_L6N_12	V8	IO_L6N_12	V8	IO_L6N_12	
V9	20	IO_L8P_CC_20	V9	IO_L8P_CC_20	V9	IO_L8P_CC_20	
V10	20	IO_L8N_CC_20	V10	IO_L8N_CC_20	V10	IO_L8N_CC_20	
V11	20	IO_L15N_20	V11	IO_L15N_20	V11	IO_L15N_20	
V12	NA	GND	V12	GND	V12	GND	
V13	NA	VCCINT	V13	VCCINT	V13	VCCINT	
V14	NA	GND	V14	GND	V14	GND	
V15	NA	VCCINT	V15	VCCINT	V15	VCCINT	
V16	NA	GND	V16	GND	V16	GND	
V17	NA	VCCINT	V17	VCCINT	V17	VCCINT	
V18	NA	GND	V18	GND	V18	GND	
V19	NA	VCCINT	V19	VCCINT	V19	VCCINT	
V20	NA	GND	V20	GND	V20	GND	
V21	NA	VCCINT	V21	VCCINT	V21	VCCINT	
V22	NA	GND	V22	GND	V22	GND	
V23	NA	VCCINT	V23	VCCINT	V23	VCCINT	
V24	NA	GND	V24	GND	V24	GND	
V25	NA	VCCINT	V25	VCCINT	V25	VCCINT	
V26	NA	GND	V26	GND	V26	GND	
V27	NA	VCCINT	V27	VCCINT	V27	VCCINT	
V28	NA	GND	V28	GND	V28	GND	
V29	NA	VCCINT	V29	VCCINT	V29	VCCINT	
V30	NA	GND	V30	GND	V30	GND	
V31	0	GND	V31	RSVD	V31	VFS_0	NC
V32	NA	GND	V32	GND	V32	GND	
V33	19	IO_L17P_19	V33	IO_L17P_19	V33	IO_L17P_19	
V34	19	IO_L16N_19	V34	IO_L16N_19	V34	IO_L16N_19	
V35	19	IO_L16P_19	V35	IO_L16P_19	V35	IO_L16P_19	
V36	19	IO_L11N_CC_19	V36	IO_L11N_CC_19	V36	IO_L11N_CC_19	
V37	11	VCCO_11	V37	VCCO_11	V37	VCCO_11	
V38	15	IO_L12P_VRN_15	V38	IO_L12P_VRN_15	V38	IO_L12P_VRN_15	
V39	15	IO_L15P_15	V39	IO_L15P_15	V39	IO_L15P_15	
V40	11	IO_L17P_SM11P_11	V40	IO_L17P_SM11P_11	V40	IO_L17P_SM11P_11	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
V41	11	IO_L16N_SM12N_11	V41	IO_L16N_SM12N_11	V41	IO_L16N_SM12N_11	
V42	NA	GND	V42	GND	V42	GND	
W1	NA	MGTRXN1_112	W1	MGTRXN1_112	W1	MGTRXN1_112	
W2	NA	GND	W2	GND	W2	GND	
W3	NA	MGTAVCC_112	W3	MGTAVCC_112	W3	MGTAVCC_112	
W4	NA	MGTAVCC_112	W4	MGTAVCC_112	W4	MGTAVCC_112	
W5	12	IO_L2P_12	W5	IO_L2P_12	W5	IO_L2P_12	
W6	12	IO_L2N_12	W6	IO_L2N_12	W6	IO_L2N_12	
W7	12	IO_L4N_VREF_12	W7	IO_L4N_VREF_12	W7	IO_L4N_VREF_12	
W8	12	IO_L6P_12	W8	IO_L6P_12	W8	IO_L6P_12	
W9	NA	GND	W9	GND	W9	GND	
W10	12	IO_L18N_12	W10	IO_L18N_12	W10	IO_L18N_12	
W11	12	IO_L18P_12	W11	IO_L18P_12	W11	IO_L18P_12	
W12	NA	VCCAUX	W12	VCCAUX	W12	VCCAUX	
W13	NA	GND	W13	GND	W13	GND	
W14	NA	VCCINT	W14	VCCINT	W14	VCCINT	
W15	NA	GND	W15	GND	W15	GND	
W16	NA	VCCINT	W16	VCCINT	W16	VCCINT	
W17	NA	GND	W17	GND	W17	GND	
W18	NA	VCCINT	W18	VCCINT	W18	VCCINT	
W19	NA	GND	W19	GND	W19	GND	
W20	NA	VCCINT	W20	VCCINT	W20	VCCINT	
W21	NA	GND	W21	GND	W21	GND	
W22	NA	VCCINT	W22	VCCINT	W22	VCCINT	
W23	NA	GND	W23	GND	W23	GND	
W24	NA	VCCINT	W24	VCCINT	W24	VCCINT	
W25	NA	GND	W25	GND	W25	GND	
W26	NA	VCCINT	W26	VCCINT	W26	VCCINT	
W27	NA	GND	W27	GND	W27	GND	
W28	NA	VCCINT	W28	VCCINT	W28	VCCINT	
W29	NA	GND	W29	GND	W29	GND	
W30	NA	VCCAUX	W30	VCCAUX	W30	VCCAUX	
W31	NA	GND	W31	GND	W31	GND	
W32	19	IO_L18N_19	W32	IO_L18N_19	W32	IO_L18N_19	
W33	19	IO_L17N_19	W33	IO_L17N_19	W33	IO_L17N_19	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
W34	NA	GND	W34	GND	W34	GND	
W35	15	IO_L18N_15	W35	IO_L18N_15	W35	IO_L18N_15	
W36	15	IO_L19P_15	W36	IO_L19P_15	W36	IO_L19P_15	
W37	15	IO_L19N_15	W37	IO_L19N_15	W37	IO_L19N_15	
W38	15	IO_L15N_15	W38	IO_L15N_15	W38	IO_L15N_15	
W39	NA	GND	W39	GND	W39	GND	
W40	11	IO_L8P_CC_11	W40	IO_L8P_CC_11	W40	IO_L8P_CC_11	
W41	11	IO_L17N_SM11N_11	W41	IO_L17N_SM11N_11	W41	IO_L17N_SM11N_11	
W42	11	IO_L18P_SM10P_11	W42	IO_L18P_SM10P_11	W42	IO_L18P_SM10P_11	
Y1	NA	MGTRXP1_112	Y1	MGTRXP1_112	Y1	MGTRXP1_112	
Y2	NA	MGTTXN1_112	Y2	MGTTXN1_112	Y2	MGTTXN1_112	
Y3	NA	MGTAVCCPLL_112	Y3	MGTAVCCPLL_112	Y3	MGTAVCCPLL_112	
Y4	NA	GND	Y4	GND	Y4	GND	
Y5	NA	GND	Y5	UNUSED	Y5	UNUSED	NC
Y6	NA	GND	Y6	GND	Y6	GND	
Y7	12	IO_L4P_12	Y7	IO_L4P_12	Y7	IO_L4P_12	
Y8	12	IO_L19N_12	Y8	IO_L19N_12	Y8	IO_L19N_12	
Y9	12	IO_L19P_12	Y9	IO_L19P_12	Y9	IO_L19P_12	
Y10	12	IO_L17N_12	Y10	IO_L17N_12	Y10	IO_L17N_12	
Y11	NA	GND	Y11	GND	Y11	GND	
Y12	NA	GND	Y12	GND	Y12	GND	
Y13	NA	VCCINT	Y13	VCCINT	Y13	VCCINT	
Y14	NA	GND	Y14	GND	Y14	GND	
Y15	NA	VCCINT	Y15	VCCINT	Y15	VCCINT	
Y16	NA	GND	Y16	GND	Y16	GND	
Y17	NA	VCCINT	Y17	VCCINT	Y17	VCCINT	
Y18	NA	GND	Y18	GND	Y18	GND	
Y19	NA	VCCINT	Y19	VCCINT	Y19	VCCINT	
Y20	NA	GND	Y20	GND	Y20	GND	
Y21	0	AVSS_0 (connect to GND)	Y21	AVSS_0	Y21	AVSS_0 (connect to GND)	
Y22	0	AVDD_0 (connect to VCCAUX)	Y22	AVDD_0	Y22	AVDD_0 (connect to VCCAUX)	
Y23	NA	VCCINT	Y23	VCCINT	Y23	VCCINT	
Y24	NA	GND	Y24	GND	Y24	GND	
Y25	NA	VCCINT	Y25	VCCINT	Y25	VCCINT	
Y26	NA	GND	Y26	GND	Y26	GND	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
Y27	NA	VCCINT	Y27	VCCINT	Y27	VCCINT	
Y28	NA	GND	Y28	GND	Y28	GND	
Y29	NA	VCCINT	Y29	VCCINT	Y29	VCCINT	
Y30	NA	GND	Y30	GND	Y30	GND	
Y31	NA	VCCAUX	Y31	VCCAUX	Y31	VCCAUX	
Y32	19	IO_L19P_19	Y32	IO_L19P_19	Y32	IO_L19P_19	
Y33	19	IO_L18P_19	Y33	IO_L18P_19	Y33	IO_L18P_19	
Y34	15	IO_L17N_15	Y34	IO_L17N_15	Y34	IO_L17N_15	
Y35	15	IO_L18P_15	Y35	IO_L18P_15	Y35	IO_L18P_15	
Y36	NA	GND	Y36	GND	Y36	GND	
Y37	11	IO_L11P_CC_SM14P_11	Y37	IO_L11P_CC_SM14P_11	Y37	IO_L11P_CC_SM14P_11	
Y38	11	IO_L10N_CC_SM15N_11	Y38	IO_L10N_CC_SM15N_11	Y38	IO_L10N_CC_SM15N_11	
Y39	11	IO_L10P_CC_SM15P_11	Y39	IO_L10P_CC_SM15P_11	Y39	IO_L10P_CC_SM15P_11	
Y40	11	IO_L8N_CC_11	Y40	IO_L8N_CC_11	Y40	IO_L8N_CC_11	
Y41	11	VCCO_11	Y41	VCCO_11	Y41	VCCO_11	
Y42	11	IO_L18N_SM10N_11	Y42	IO_L18N_SM10N_11	Y42	IO_L18N_SM10N_11	
AA1	NA	GND	AA1	UNPOPULATED	AA1	GND	
AA2	NA	MGTTXP1_112	AA2	MGTTXP1_112	AA2	MGTTXP1_112	
AA3	NA	MGTAVTTTX_112	AA3	MGTAVTTTX_112	AA3	MGTAVTTTX_112	
AA4	NA	GND	AA4	UNUSED	AA4	UNUSED	NC
AA5	NA	MGTAVTTRXC	AA5	MGTAVTTRXC	AA5	MGTAVTTRXC	
AA6	12	IO_L0N_12	AA6	IO_L0N_12	AA6	IO_L0N_12	
AA7	12	IO_L0P_12	AA7	IO_L0P_12	AA7	IO_L0P_12	
AA8	12	VCCO_12	AA8	VCCO_12	AA8	VCCO_12	
AA9	12	IO_L17P_12	AA9	IO_L17P_12	AA9	IO_L17P_12	
AA10	12	IO_L16N_12	AA10	IO_L16N_12	AA10	IO_L16N_12	
AA11	12	IO_L16P_12	AA11	IO_L16P_12	AA11	IO_L16P_12	
AA12	NA	VCCAUX	AA12	VCCAUX	AA12	VCCAUX	
AA13	NA	GND	AA13	GND	AA13	GND	
AA14	NA	VCCINT	AA14	VCCINT	AA14	VCCINT	
AA15	NA	GND	AA15	GND	AA15	GND	
AA16	NA	VCCINT	AA16	VCCINT	AA16	VCCINT	
AA17	NA	GND	AA17	GND	AA17	GND	
AA18	NA	VCCINT	AA18	VCCINT	AA18	VCCINT	
AA19	NA	GND	AA19	GND	AA19	GND	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AA20	NA	VCCINT	AA20	VCCINT	AA20	VCCINT	
AA21	0	GND	AA21	VREFN_0	AA21	VREFN_0	NC
AA22	0	GND	AA22	VP_0	AA22	VP_0	NC
AA23	NA	GND	AA23	GND	AA23	GND	
AA24	NA	VCCINT	AA24	VCCINT	AA24	VCCINT	
AA25	NA	GND	AA25	GND	AA25	GND	
AA26	NA	VCCINT	AA26	VCCINT	AA26	VCCINT	
AA27	NA	GND	AA27	GND	AA27	GND	
AA28	NA	VCCINT	AA28	VCCINT	AA28	VCCINT	
AA29	NA	GND	AA29	GND	AA29	GND	
AA30	NA	VCCAUX	AA30	VCCAUX	AA30	VCCAUX	
AA31	NA	GND	AA31	GND	AA31	GND	
AA32	19	IO_L19N_19	AA32	IO_L19N_19	AA32	IO_L19N_19	
AA33	NA	GND	AA33	GND	AA33	GND	
AA34	15	IO_L17P_15	AA34	IO_L17P_15	AA34	IO_L17P_15	
AA35	15	IO_L16P_15	AA35	IO_L16P_15	AA35	IO_L16P_15	
AA36	15	IO_L16N_15	AA36	IO_L16N_15	AA36	IO_L16N_15	
AA37	11	IO_L11N_CC_SM14N_11	AA37	IO_L11N_CC_SM14N_11	AA37	IO_L11N_CC_SM14N_11	
AA38	11	VCCO_11	AA38	VCCO_11	AA38	VCCO_11	
AA39	11	IO_L9N_CC_11	AA39	IO_L9N_CC_11	AA39	IO_L9N_CC_11	
AA40	11	IO_L9P_CC_11	AA40	IO_L9P_CC_11	AA40	IO_L9P_CC_11	
AA41	11	IO_L19N_SM9N_11	AA41	IO_L19N_SM9N_11	AA41	IO_L19N_SM9N_11	
AA42	11	IO_L19P_SM9P_11	AA42	IO_L19P_SM9P_11	AA42	IO_L19P_SM9P_11	
AB1	NA	GND	AB1	UNPOPULATED	AB1	GND	
AB2	NA	MGTTXP0_114	AB2	MGTTXP0_114	AB2	MGTTXP0_114	
AB3	NA	MGTAVTTTX_114	AB3	MGTAVTTTX_114	AB3	MGTAVTTTX_114	
AB4	NA	MGTRREF_112	AB4	MGTRREF_112	AB4	MGTRREF_112	
AB5	NA	GND	AB5	GND	AB5	GND	
AB6	18	IO_L9N_CC_18	AB6	IO_L9N_CC_18	AB6	IO_L9N_CC_18	
AB7	18	IO_L9P_CC_18	AB7	IO_L9P_CC_18	AB7	IO_L9P_CC_18	
AB8	18	IO_L3N_18	AB8	IO_L3N_18	AB8	IO_L3N_18	
AB9	18	IO_L3P_18	AB9	IO_L3P_18	AB9	IO_L3P_18	
AB10	NA	GND	AB10	GND	AB10	GND	
AB11	18	IO_L1P_18	AB11	IO_L1P_18	AB11	IO_L1P_18	
AB12	NA	GND	AB12	GND	AB12	GND	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AB13	NA	VCCINT	AB13	VCCINT	AB13	VCCINT	
AB14	NA	GND	AB14	GND	AB14	GND	
AB15	NA	VCCINT	AB15	VCCINT	AB15	VCCINT	
AB16	NA	GND	AB16	GND	AB16	GND	
AB17	NA	VCCINT	AB17	VCCINT	AB17	VCCINT	
AB18	NA	GND	AB18	GND	AB18	GND	
AB19	NA	VCCINT	AB19	VCCINT	AB19	VCCINT	
AB20	NA	GND	AB20	GND	AB20	GND	
AB21	0	GND	AB21	VN_0	AB21	VN_0	NC
AB22	0	GND	AB22	VREFP_0	AB22	VREFP_0	NC
AB23	NA	VCCINT	AB23	VCCINT	AB23	VCCINT	
AB24	NA	GND	AB24	GND	AB24	GND	
AB25	NA	VCCINT	AB25	VCCINT	AB25	VCCINT	
AB26	NA	GND	AB26	GND	AB26	GND	
AB27	NA	VCCINT	AB27	VCCINT	AB27	VCCINT	
AB28	NA	GND	AB28	GND	AB28	GND	
AB29	NA	VCCINT	AB29	VCCINT	AB29	VCCINT	
AB30	NA	GND	AB30	GND	AB30	GND	
AB31	NA	VCCAUX	AB31	VCCAUX	AB31	VCCAUX	
AB32	21	IO_L0N_21	AB32	IO_L0N_21	AB32	IO_L0N_21	
AB33	21	IO_L0P_21	AB33	IO_L0P_21	AB33	IO_L0P_21	
AB34	17	IO_L0P_17	AB34	IO_L0P_17	AB34	IO_L0P_17	
AB35	13	VCCO_13	AB35	VCCO_13	AB35	VCCO_13	
AB36	17	IO_L1N_17	AB36	IO_L1N_17	AB36	IO_L1N_17	
AB37	13	IO_L8P_CC_SM1P_13	AB37	IO_L8P_CC_SM1P_13	AB37	IO_L8P_CC_SM1P_13	
AB38	13	IO_L8N_CC_SM1N_13	AB38	IO_L8N_CC_SM1N_13	AB38	IO_L8N_CC_SM1N_13	
AB39	13	IO_L9P_CC_SM0P_13	AB39	IO_L9P_CC_SM0P_13	AB39	IO_L9P_CC_SM0P_13	
AB40	NA	GND	AB40	GND	AB40	GND	
AB41	13	IO_L0P_SM8P_13	AB41	IO_L0P_SM8P_13	AB41	IO_L0P_SM8P_13	
AB42	13	IO_L0N_SM8N_13	AB42	IO_L0N_SM8N_13	AB42	IO_L0N_SM8N_13	
AC1	NA	MGTRXP0_114	AC1	MGTRXP0_114	AC1	MGTRXP0_114	
AC2	NA	MGTTXN0_114	AC2	MGTTXN0_114	AC2	MGTTXN0_114	
AC3	NA	MGTAVTTRX_114	AC3	MGTAVTTRX_114	AC3	MGTAVTTRX_114	
AC4	NA	GND	AC4	GND	AC4	GND	
AC5	18	IO_L10P_CC_18	AC5	IO_L10P_CC_18	AC5	IO_L10P_CC_18	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AC6	18	IO_L10N_CC_18	AC6	IO_L10N_CC_18	AC6	IO_L10N_CC_18	
AC7	NA	GND	AC7	GND	AC7	GND	
AC8	18	IO_L5P_18	AC8	IO_L5P_18	AC8	IO_L5P_18	
AC9	18	IO_L5N_18	AC9	IO_L5N_18	AC9	IO_L5N_18	
AC10	18	IO_L1N_18	AC10	IO_L1N_18	AC10	IO_L1N_18	
AC11	NA	GND	AC11	GND	AC11	GND	
AC12	NA	VCCAUX	AC12	VCCAUX	AC12	VCCAUX	
AC13	NA	GND	AC13	GND	AC13	GND	
AC14	NA	VCCINT	AC14	VCCINT	AC14	VCCINT	
AC15	NA	GND	AC15	GND	AC15	GND	
AC16	NA	VCCINT	AC16	VCCINT	AC16	VCCINT	
AC17	NA	GND	AC17	GND	AC17	GND	
AC18	NA	VCCINT	AC18	VCCINT	AC18	VCCINT	
AC19	NA	GND	AC19	GND	AC19	GND	
AC20	NA	VCCINT	AC20	VCCINT	AC20	VCCINT	
AC21	0	DXN_0	AC21	DXN_0	AC21	DXN_0	
AC22	0	DXP_0	AC22	DXP_0	AC22	DXP_0	
AC23	NA	GND	AC23	GND	AC23	GND	
AC24	NA	VCCINT	AC24	VCCINT	AC24	VCCINT	
AC25	NA	GND	AC25	GND	AC25	GND	
AC26	NA	VCCINT	AC26	VCCINT	AC26	VCCINT	
AC27	NA	GND	AC27	GND	AC27	GND	
AC28	NA	VCCINT	AC28	VCCINT	AC28	VCCINT	
AC29	NA	GND	AC29	GND	AC29	GND	
AC30	NA	VCCAUX	AC30	VCCAUX	AC30	VCCAUX	
AC31	NA	GND	AC31	GND	AC31	GND	
AC32	NA	GND	AC32	GND	AC32	GND	
AC33	21	IO_L1P_21	AC33	IO_L1P_21	AC33	IO_L1P_21	
AC34	17	IO_L0N_17	AC34	IO_L0N_17	AC34	IO_L0N_17	
AC35	17	IO_L1P_17	AC35	IO_L1P_17	AC35	IO_L1P_17	
AC36	17	IO_L2P_17	AC36	IO_L2P_17	AC36	IO_L2P_17	
AC37	NA	GND	AC37	GND	AC37	GND	
AC38	13	IO_L9N_CC_SM0N_13	AC38	IO_L9N_CC_SM0N_13	AC38	IO_L9N_CC_SM0N_13	
AC39	13	IO_L11N_CC_13	AC39	IO_L11N_CC_13	AC39	IO_L11N_CC_13	
AC40	13	IO_L11P_CC_13	AC40	IO_L11P_CC_13	AC40	IO_L11P_CC_13	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AC41	13	IO_L1P_SM7P_13	AC41	IO_L1P_SM7P_13	AC41	IO_L1P_SM7P_13	
AC42	NA	GND	AC42	GND	AC42	GND	
AD1	NA	MGTRXN0_114	AD1	MGTRXN0_114	AD1	MGTRXN0_114	
AD2	NA	GND	AD2	GND	AD2	GND	
AD3	NA	MGTREFCLKN_114	AD3	MGTREFCLKN_114	AD3	MGTREFCLKN_114	
AD4	NA	MGTREFCLKP_114	AD4	MGTREFCLKP_114	AD4	MGTREFCLKP_114	
AD5	18	IO_L14N_VREF_18	AD5	IO_L14N_VREF_18	AD5	IO_L14N_VREF_18	
AD6	18	IO_L12P_VRN_18	AD6	IO_L12P_VRN_18	AD6	IO_L12P_VRN_18	
AD7	18	IO_L12N_VRP_18	AD7	IO_L12N_VRP_18	AD7	IO_L12N_VRP_18	
AD8	18	IO_L16P_18	AD8	IO_L16P_18	AD8	IO_L16P_18	
AD9	18	VCCO_18	AD9	VCCO_18	AD9	VCCO_18	
AD10	18	IO_L7P_18	AD10	IO_L7P_18	AD10	IO_L7P_18	
AD11	18	IO_L7N_18	AD11	IO_L7N_18	AD11	IO_L7N_18	
AD12	NA	GND	AD12	GND	AD12	GND	
AD13	NA	VCCINT	AD13	VCCINT	AD13	VCCINT	
AD14	NA	GND	AD14	GND	AD14	GND	
AD15	NA	VCCINT	AD15	VCCINT	AD15	VCCINT	
AD16	NA	GND	AD16	GND	AD16	GND	
AD17	NA	VCCINT	AD17	VCCINT	AD17	VCCINT	
AD18	NA	GND	AD18	GND	AD18	GND	
AD19	NA	VCCINT	AD19	VCCINT	AD19	VCCINT	
AD20	NA	GND	AD20	GND	AD20	GND	
AD21	NA	VCCINT	AD21	VCCINT	AD21	VCCINT	
AD22	NA	GND	AD22	GND	AD22	GND	
AD23	NA	VCCINT	AD23	VCCINT	AD23	VCCINT	
AD24	NA	GND	AD24	GND	AD24	GND	
AD25	NA	VCCINT	AD25	VCCINT	AD25	VCCINT	
AD26	NA	GND	AD26	GND	AD26	GND	
AD27	NA	VCCINT	AD27	VCCINT	AD27	VCCINT	
AD28	NA	GND	AD28	GND	AD28	GND	
AD29	NA	VCCINT	AD29	VCCINT	AD29	VCCINT	
AD30	NA	GND	AD30	GND	AD30	GND	
AD31	NA	VCCAUX	AD31	VCCAUX	AD31	VCCAUX	
AD32	21	IO_L1N_21	AD32	IO_L1N_21	AD32	IO_L1N_21	
AD33	21	IO_L2P_21	AD33	IO_L2P_21	AD33	IO_L2P_21	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AD34	NA	GND	AD34	GND	AD34	GND	
AD35	17	IO_L2N_17	AD35	IO_L2N_17	AD35	IO_L2N_17	
AD36	17	IO_L3P_17	AD36	IO_L3P_17	AD36	IO_L3P_17	
AD37	17	IO_L3N_17	AD37	IO_L3N_17	AD37	IO_L3N_17	
AD38	17	IO_L4N_VREF_17	AD38	IO_L4N_VREF_17	AD38	IO_L4N_VREF_17	
AD39	13	VCCO_13	AD39	VCCO_13	AD39	VCCO_13	
AD40	13	IO_L10N_CC_13	AD40	IO_L10N_CC_13	AD40	IO_L10N_CC_13	
AD41	13	IO_L2N_SM6N_13	AD41	IO_L2N_SM6N_13	AD41	IO_L2N_SM6N_13	
AD42	13	IO_L1N_SM7N_13	AD42	IO_L1N_SM7N_13	AD42	IO_L1N_SM7N_13	
AE1	NA	MGTRXN1_114	AE1	MGTRXN1_114	AE1	MGTRXN1_114	
AE2	NA	GND	AE2	GND	AE2	GND	
AE3	NA	MGTAVCC_114	AE3	MGTAVCC_114	AE3	MGTAVCC_114	
AE4	NA	MGTAVCC_114	AE4	MGTAVCC_114	AE4	MGTAVCC_114	
AE5	18	IO_L14P_18	AE5	IO_L14P_18	AE5	IO_L14P_18	
AE6	18	VCCO_18	AE6	VCCO_18	AE6	VCCO_18	
AE7	18	IO_L15N_18	AE7	IO_L15N_18	AE7	IO_L15N_18	
AE8	18	IO_L16N_18	AE8	IO_L16N_18	AE8	IO_L16N_18	
AE9	18	IO_L18P_18	AE9	IO_L18P_18	AE9	IO_L18P_18	
AE10	18	IO_L18N_18	AE10	IO_L18N_18	AE10	IO_L18N_18	
AE11	NA	GND	AE11	GND	AE11	GND	
AE12	NA	VCCAUX	AE12	VCCAUX	AE12	VCCAUX	
AE13	NA	GND	AE13	GND	AE13	GND	
AE14	NA	VCCINT	AE14	VCCINT	AE14	VCCINT	
AE15	NA	GND	AE15	GND	AE15	GND	
AE16	NA	VCCINT	AE16	VCCINT	AE16	VCCINT	
AE17	NA	GND	AE17	GND	AE17	GND	
AE18	NA	VCCINT	AE18	VCCINT	AE18	VCCINT	
AE19	NA	GND	AE19	GND	AE19	GND	
AE20	NA	VCCINT	AE20	VCCINT	AE20	VCCINT	
AE21	NA	GND	AE21	GND	AE21	GND	
AE22	NA	VCCINT	AE22	VCCINT	AE22	VCCINT	
AE23	NA	GND	AE23	GND	AE23	GND	
AE24	NA	VCCINT	AE24	VCCINT	AE24	VCCINT	
AE25	NA	GND	AE25	GND	AE25	GND	
AE26	NA	VCCINT	AE26	VCCINT	AE26	VCCINT	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AE27	NA	GND	AE27	GND	AE27	GND	
AE28	NA	VCCINT	AE28	VCCINT	AE28	VCCINT	
AE29	NA	GND	AE29	GND	AE29	GND	
AE30	NA	VCCAUX	AE30	VCCAUX	AE30	VCCAUX	
AE31	NA	GND	AE31	GND	AE31	GND	
AE32	21	IO_L2N_21	AE32	IO_L2N_21	AE32	IO_L2N_21	
AE33	21	IO_L3P_21	AE33	IO_L3P_21	AE33	IO_L3P_21	
AE34	21	IO_L3N_21	AE34	IO_L3N_21	AE34	IO_L3N_21	
AE35	21	IO_L8P_CC_21	AE35	IO_L8P_CC_21	AE35	IO_L8P_CC_21	
AE36	13	VCCO_13	AE36	VCCO_13	AE36	VCCO_13	
AE37	17	IO_L4P_17	AE37	IO_L4P_17	AE37	IO_L4P_17	
AE38	17	IO_L5N_17	AE38	IO_L5N_17	AE38	IO_L5N_17	
AE39	17	IO_L5P_17	AE39	IO_L5P_17	AE39	IO_L5P_17	
AE40	13	IO_L10P_CC_13	AE40	IO_L10P_CC_13	AE40	IO_L10P_CC_13	
AE41	NA	GND	AE41	GND	AE41	GND	
AE42	13	IO_L2P_SM6P_13	AE42	IO_L2P_SM6P_13	AE42	IO_L2P_SM6P_13	
AF1	NA	MGTRXP1_114	AF1	MGTRXP1_114	AF1	MGTRXP1_114	
AF2	NA	MGTTXN1_114	AF2	MGTTXN1_114	AF2	MGTTXN1_114	
AF3	NA	MGTAVCCPLL_114	AF3	MGTAVCCPLL_114	AF3	MGTAVCCPLL_114	
AF4	NA	GND	AF4	GND	AF4	GND	
AF5	18	IO_L11P_CC_18	AF5	IO_L11P_CC_18	AF5	IO_L11P_CC_18	
AF6	18	IO_L11N_CC_18	AF6	IO_L11N_CC_18	AF6	IO_L11N_CC_18	
AF7	18	IO_L15P_18	AF7	IO_L15P_18	AF7	IO_L15P_18	
AF8	NA	GND	AF8	GND	AF8	GND	
AF9	18	IO_L17P_18	AF9	IO_L17P_18	AF9	IO_L17P_18	
AF10	18	IO_L17N_18	AF10	IO_L17N_18	AF10	IO_L17N_18	
AF11	18	IO_L19P_18	AF11	IO_L19P_18	AF11	IO_L19P_18	
AF12	18	IO_L19N_18	AF12	IO_L19N_18	AF12	IO_L19N_18	
AF13	NA	VCCAUX	AF13	VCCAUX	AF13	VCCAUX	
AF14	NA	GND	AF14	GND	AF14	GND	
AF15	NA	VCCINT	AF15	VCCINT	AF15	VCCINT	
AF16	NA	GND	AF16	GND	AF16	GND	
AF17	NA	VCCINT	AF17	VCCINT	AF17	VCCINT	
AF18	NA	GND	AF18	GND	AF18	GND	
AF19	NA	VCCINT	AF19	VCCINT	AF19	VCCINT	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AF20	NA	GND	AF20	GND	AF20	GND	
AF21	NA	VCCINT	AF21	VCCINT	AF21	VCCINT	
AF22	NA	GND	AF22	GND	AF22	GND	
AF23	NA	VCCINT	AF23	VCCINT	AF23	VCCINT	
AF24	NA	GND	AF24	GND	AF24	GND	
AF25	NA	VCCINT	AF25	VCCINT	AF25	VCCINT	
AF26	NA	GND	AF26	GND	AF26	GND	
AF27	NA	VCCINT	AF27	VCCINT	AF27	VCCINT	
AF28	NA	GND	AF28	GND	AF28	GND	
AF29	NA	VCCAUX	AF29	VCCAUX	AF29	VCCAUX	
AF30	0	GND	AF30	RSVD	AF30	R_FUSE_0	NC
AF31	25	IO_L0N_25	AF31	IO_L0N_25	AF31	IO_L0N_25	
AF32	25	IO_L1P_25	AF32	IO_L1P_25	AF32	IO_L1P_25	
AF33	NA	GND	AF33	GND	AF33	GND	
AF34	21	IO_L8N_CC_21	AF34	IO_L8N_CC_21	AF34	IO_L8N_CC_21	
AF35	21	IO_L9P_CC_21	AF35	IO_L9P_CC_21	AF35	IO_L9P_CC_21	
AF36	21	IO_L9N_CC_21	AF36	IO_L9N_CC_21	AF36	IO_L9N_CC_21	
AF37	17	IO_L7N_17	AF37	IO_L7N_17	AF37	IO_L7N_17	
AF38	NA	GND	AF38	GND	AF38	GND	
AF39	17	IO_L6P_17	AF39	IO_L6P_17	AF39	IO_L6P_17	
AF40	13	IO_L4P_13	AF40	IO_L4P_13	AF40	IO_L4P_13	
AF41	13	IO_L3P_SM5P_13	AF41	IO_L3P_SM5P_13	AF41	IO_L3P_SM5P_13	
AF42	13	IO_L3N_SM5N_13	AF42	IO_L3N_SM5N_13	AF42	IO_L3N_SM5N_13	
AG1	NA	GND	AG1	UNPOPULATED	AG1	GND	
AG2	NA	MGTTXP1_114	AG2	MGTTXP1_114	AG2	MGTTXP1_114	
AG3	NA	MGTAVTTTX_114	AG3	MGTAVTTTX_114	AG3	MGTAVTTTX_114	
AG4	18	IO_L8P_CC_18	AG4	IO_L8P_CC_18	AG4	IO_L8P_CC_18	
AG5	NA	GND	AG5	GND	AG5	GND	
AG6	18	IO_L13P_18	AG6	IO_L13P_18	AG6	IO_L13P_18	
AG7	18	IO_L13N_18	AG7	IO_L13N_18	AG7	IO_L13N_18	
AG8	26	IO_L9P_CC_26	AG8	IO_L9P_CC_26	AG8	IO_L9P_CC_26	
AG9	26	IO_L3P_26	AG9	IO_L3P_26	AG9	IO_L3P_26	
AG10	18	VCCO_18	AG10	VCCO_18	AG10	VCCO_18	
AG11	26	IO_L1N_26	AG11	IO_L1N_26	AG11	IO_L1N_26	
AG12	26	IO_L1P_26	AG12	IO_L1P_26	AG12	IO_L1P_26	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AG13	NA	GND	AG13	GND	AG13	GND	
AG14	NA	VCCINT	AG14	VCCINT	AG14	VCCINT	
AG15	NA	GND	AG15	GND	AG15	GND	
AG16	NA	VCCINT	AG16	VCCINT	AG16	VCCINT	
AG17	NA	GND	AG17	GND	AG17	GND	
AG18	NA	VCCINT	AG18	VCCINT	AG18	VCCINT	
AG19	NA	GND	AG19	GND	AG19	GND	
AG20	NA	VCCINT	AG20	VCCINT	AG20	VCCINT	
AG21	NA	GND	AG21	GND	AG21	GND	
AG22	NA	VCCINT	AG22	VCCINT	AG22	VCCINT	
AG23	NA	GND	AG23	GND	AG23	GND	
AG24	NA	VCCINT	AG24	VCCINT	AG24	VCCINT	
AG25	NA	GND	AG25	GND	AG25	GND	
AG26	NA	VCCINT	AG26	VCCINT	AG26	VCCINT	
AG27	NA	GND	AG27	GND	AG27	GND	
AG28	NA	VCCINT	AG28	VCCINT	AG28	VCCINT	
AG29	0	TCK_0	AG29	TCK_0	AG29	TCK_0	
AG30	0	VCCO_0	AG30	VCCO_0	AG30	VCCO_0	
AG31	25	IO_L0P_25	AG31	IO_L0P_25	AG31	IO_L0P_25	
AG32	25	IO_L2N_25	AG32	IO_L2N_25	AG32	IO_L2N_25	
AG33	25	IO_L1N_25	AG33	IO_L1N_25	AG33	IO_L1N_25	
AG34	21	IO_L10N_CC_21	AG34	IO_L10N_CC_21	AG34	IO_L10N_CC_21	
AG35	NA	GND	AG35	GND	AG35	GND	
AG36	21	IO_L11N_CC_21	AG36	IO_L11N_CC_21	AG36	IO_L11N_CC_21	
AG37	17	IO_L7P_17	AG37	IO_L7P_17	AG37	IO_L7P_17	
AG38	17	IO_L6N_17	AG38	IO_L6N_17	AG38	IO_L6N_17	
AG39	17	IO_L12P_VRN_17	AG39	IO_L12P_VRN_17	AG39	IO_L12P_VRN_17	
AG40	17	VCCO_17	AG40	VCCO_17	AG40	VCCO_17	
AG41	13	IO_L4N_VREF_13	AG41	IO_L4N_VREF_13	AG41	IO_L4N_VREF_13	
AG42	13	IO_L5P_SM4P_13	AG42	IO_L5P_SM4P_13	AG42	IO_L5P_SM4P_13	
AH1	NA	GND	AH1	UNPOPULATED	AH1	GND	
AH2	NA	MGTTXP0_118	AH2	MGTTXP0_118	AH2	MGTTXP0_118	
AH3	NA	MGTAVTTTX_118	AH3	MGTAVTTTX_118	AH3	MGTAVTTTX_118	
AH4	18	IO_L8N_CC_18	AH4	IO_L8N_CC_18	AH4	IO_L8N_CC_18	
AH5	18	IO_L6N_18	AH5	IO_L6N_18	AH5	IO_L6N_18	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AH6	18	IO_L6P_18	AH6	IO_L6P_18	AH6	IO_L6P_18	
AH7	26	VCCO_26	AH7	VCCO_26	AH7	VCCO_26	
AH8	26	IO_L9N_CC_26	AH8	IO_L9N_CC_26	AH8	IO_L9N_CC_26	
AH9	26	IO_L3N_26	AH9	IO_L3N_26	AH9	IO_L3N_26	
AH10	26	IO_L5P_26	AH10	IO_L5P_26	AH10	IO_L5P_26	
AH11	26	IO_L5N_26	AH11	IO_L5N_26	AH11	IO_L5N_26	
AH12	NA	GND	AH12	GND	AH12	GND	
AH13	NA	VCCAUX	AH13	VCCAUX	AH13	VCCAUX	
AH14	0	CCLK_0	AH14	CCLK_0	AH14	CCLK_0	
AH15	0	TMS_0	AH15	TMS_0	AH15	TMS_0	
AH16	0	TDI_0	AH16	TDI_0	AH16	TDI_0	
AH17	NA	VCCINT	AH17	VCCINT	AH17	VCCINT	
AH18	NA	GND	AH18	GND	AH18	GND	
AH19	NA	VCCINT	AH19	VCCINT	AH19	VCCINT	
AH20	NA	GND	AH20	GND	AH20	GND	
AH21	NA	VCCINT	AH21	VCCINT	AH21	VCCINT	
AH22	NA	GND	AH22	GND	AH22	GND	
AH23	NA	VCCINT	AH23	VCCINT	AH23	VCCINT	
AH24	NA	GND	AH24	GND	AH24	GND	
AH25	NA	VCCINT	AH25	VCCINT	AH25	VCCINT	
AH26	NA	GND	AH26	GND	AH26	GND	
AH27	NA	VCCINT	AH27	VCCINT	AH27	VCCINT	
AH28	NA	GND	AH28	GND	AH28	GND	
AH29	0	M0_0	AH29	M0_0	AH29	M0_0	
AH30	0	M1_0	AH30	M1_0	AH30	M1_0	
AH31	25	IO_L3P_25	AH31	IO_L3P_25	AH31	IO_L3P_25	
AH32	NA	GND	AH32	GND	AH32	GND	
AH33	25	IO_L2P_25	AH33	IO_L2P_25	AH33	IO_L2P_25	
AH34	21	IO_L10P_CC_21	AH34	IO_L10P_CC_21	AH34	IO_L10P_CC_21	
AH35	21	IO_L11P_CC_21	AH35	IO_L11P_CC_21	AH35	IO_L11P_CC_21	
AH36	21	IO_L16P_21	AH36	IO_L16P_21	AH36	IO_L16P_21	
AH37	17	VCCO_17	AH37	VCCO_17	AH37	VCCO_17	
AH38	17	IO_L15N_17	AH38	IO_L15N_17	AH38	IO_L15N_17	
AH39	17	IO_L12N_VRP_17	AH39	IO_L12N_VRP_17	AH39	IO_L12N_VRP_17	
AH40	13	IO_L7P_SM2P_13	AH40	IO_L7P_SM2P_13	AH40	IO_L7P_SM2P_13	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AH41	13	IO_L5N_SM4N_13	AH41	IO_L5N_SM4N_13	AH41	IO_L5N_SM4N_13	
AH42	NA	GND	AH42	GND	AH42	GND	
AJ1	NA	MGTRXP0_118	AJ1	MGTRXP0_118	AJ1	MGTRXP0_118	
AJ2	NA	MGTTXN0_118	AJ2	MGTTXN0_118	AJ2	MGTTXN0_118	
AJ3	NA	MGTAVTTRX_118	AJ3	MGTAVTTRX_118	AJ3	MGTAVTTRX_118	
AJ4	NA	GND	AJ4	GND	AJ4	GND	
AJ5	18	IO_L4N_VREF_18	AJ5	IO_L4N_VREF_18	AJ5	IO_L4N_VREF_18	
AJ6	18	IO_L4P_18	AJ6	IO_L4P_18	AJ6	IO_L4P_18	
AJ7	18	IO_L0P_18	AJ7	IO_L0P_18	AJ7	IO_L0P_18	
AJ8	26	IO_L10N_CC_26	AJ8	IO_L10N_CC_26	AJ8	IO_L10N_CC_26	
AJ9	NA	GND	AJ9	GND	AJ9	GND	
AJ10	26	IO_L7N_26	AJ10	IO_L7N_26	AJ10	IO_L7N_26	
AJ11	26	IO_L7P_26	AJ11	IO_L7P_26	AJ11	IO_L7P_26	
AJ12	NA	VCCAUX	AJ12	VCCAUX	AJ12	VCCAUX	
AJ13	NA	GND	AJ13	GND	AJ13	GND	
AJ14	NA	GND	AJ14	GND	AJ14	GND	
AJ15	0	TDO_0	AJ15	TDO_0	AJ15	TDO_0	
AJ16	0	D_OUT_BUSY_0	AJ16	D_OUT_BUSY_0	AJ16	D_OUT_BUSY_0	
AJ17	NA	GND	AJ17	GND	AJ17	GND	
AJ18	NA	VCCINT	AJ18	VCCINT	AJ18	VCCINT	
AJ19	NA	GND	AJ19	GND	AJ19	GND	
AJ20	NA	VCCINT	AJ20	VCCINT	AJ20	VCCINT	
AJ21	8	IO_L2N_8	AJ21	IO_L2N_8	AJ21	IO_L2N_8	
AJ22	8	IO_L2P_8	AJ22	IO_L2P_8	AJ22	IO_L2P_8	
AJ23	NA	GND	AJ23	GND	AJ23	GND	
AJ24	NA	VCCINT	AJ24	VCCINT	AJ24	VCCINT	
AJ25	NA	GND	AJ25	GND	AJ25	GND	
AJ26	2	IO_L9N_D0_FS0_2	AJ26	IO_L9N_D0_FS0_2	AJ26	IO_L9N_D0_FS0_2	
AJ27	NA	GND	AJ27	GND	AJ27	GND	
AJ28	0	M2_0	AJ28	M2_0	AJ28	M2_0	
AJ29	NA	GND	AJ29	GND	AJ29	GND	
AJ30	2	IO_L1P_CC_A25_2	AJ30	IO_L1P_CC_A25_2	AJ30	IO_L1P_CC_A25_2	
AJ31	25	IO_L3N_25	AJ31	IO_L3N_25	AJ31	IO_L3N_25	
AJ32	25	IO_L17P_25	AJ32	IO_L17P_25	AJ32	IO_L17P_25	
AJ33	25	IO_L16N_25	AJ33	IO_L16N_25	AJ33	IO_L16N_25	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AJ34	21	VCCO_21	AJ34	VCCO_21	AJ34	VCCO_21	
AJ35	21	IO_L17P_21	AJ35	IO_L17P_21	AJ35	IO_L17P_21	
AJ36	21	IO_L16N_21	AJ36	IO_L16N_21	AJ36	IO_L16N_21	
AJ37	17	IO_L15P_17	AJ37	IO_L15P_17	AJ37	IO_L15P_17	
AJ38	17	IO_L13P_17	AJ38	IO_L13P_17	AJ38	IO_L13P_17	
AJ39	NA	GND	AJ39	GND	AJ39	GND	
AJ40	13	IO_L7N_SM2N_13	AJ40	IO_L7N_SM2N_13	AJ40	IO_L7N_SM2N_13	
AJ41	13	IO_L6N_SM3N_13	AJ41	IO_L6N_SM3N_13	AJ41	IO_L6N_SM3N_13	
AJ42	13	IO_L6P_SM3P_13	AJ42	IO_L6P_SM3P_13	AJ42	IO_L6P_SM3P_13	
AK1	NA	MGTRXN0_118	AK1	MGTRXN0_118	AK1	MGTRXN0_118	
AK2	NA	GND	AK2	GND	AK2	GND	
AK3	NA	MGTREFCLKN_118	AK3	MGTREFCLKN_118	AK3	MGTREFCLKN_118	
AK4	NA	MGTREFCLKP_118	AK4	MGTREFCLKP_118	AK4	MGTREFCLKP_118	
AK5	18	IO_L2N_18	AK5	IO_L2N_18	AK5	IO_L2N_18	
AK6	NA	GND	AK6	GND	AK6	GND	
AK7	18	IO_L0N_18	AK7	IO_L0N_18	AK7	IO_L0N_18	
AK8	26	IO_L10P_CC_26	AK8	IO_L10P_CC_26	AK8	IO_L10P_CC_26	
AK9	26	IO_L12P_VRN_26	AK9	IO_L12P_VRN_26	AK9	IO_L12P_VRN_26	
AK10	26	IO_L12N_VRP_26	AK10	IO_L12N_VRP_26	AK10	IO_L12N_VRP_26	
AK11	26	VCCO_26	AK11	VCCO_26	AK11	VCCO_26	
AK12	2	IO_L0P_CC_RS1_2	AK12	IO_L0P_CC_RS1_2	AK12	IO_L0P_CC_RS1_2	
AK13	2	IO_L0N_CC_RS0_2	AK13	IO_L0N_CC_RS0_2	AK13	IO_L0N_CC_RS0_2	
AK14	2	IO_L2N_A22_2	AK14	IO_L2N_A22_2	AK14	IO_L2N_A22_2	
AK15	2	IO_L2P_A23_2	AK15	IO_L2P_A23_2	AK15	IO_L2P_A23_2	
AK16	NA	GND	AK16	GND	AK16	GND	
AK17	4	IO_L1P_GC_D13_4	AK17	IO_L1P_GC_D13_4	AK17	IO_L1P_GC_D13_4	
AK18	6	IO_L16P_6	AK18	IO_L16P_6	AK18	IO_L16P_6	
AK19	6	IO_L16N_6	AK19	IO_L16N_6	AK19	IO_L16N_6	
AK20	8	IO_L3P_8	AK20	IO_L3P_8	AK20	IO_L3P_8	
AK21	NA	GND	AK21	GND	AK21	GND	
AK22	8	IO_L1N_8	AK22	IO_L1N_8	AK22	IO_L1N_8	
AK23	8	IO_L1P_8	AK23	IO_L1P_8	AK23	IO_L1P_8	
AK24	6	IO_L17P_6	AK24	IO_L17P_6	AK24	IO_L17P_6	
AK25	6	IO_L17N_6	AK25	IO_L17N_6	AK25	IO_L17N_6	
AK26	NA	GND	AK26	GND	AK26	GND	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AK27	2	IO_L9P_D1_FS1_2	AK27	IO_L9P_D1_FS1_2	AK27	IO_L9P_D1_FS1_2	
AK28	2	IO_L7P_D5_2	AK28	IO_L7P_D5_2	AK28	IO_L7P_D5_2	
AK29	2	IO_L7N_D4_2	AK29	IO_L7N_D4_2	AK29	IO_L7N_D4_2	
AK30	2	IO_L1N_CC_A24_2	AK30	IO_L1N_CC_A24_2	AK30	IO_L1N_CC_A24_2	
AK31	NA	GND	AK31	GND	AK31	GND	
AK32	25	IO_L17N_25	AK32	IO_L17N_25	AK32	IO_L17N_25	
AK33	25	IO_L16P_25	AK33	IO_L16P_25	AK33	IO_L16P_25	
AK34	21	IO_L19N_21	AK34	IO_L19N_21	AK34	IO_L19N_21	
AK35	21	IO_L17N_21	AK35	IO_L17N_21	AK35	IO_L17N_21	
AK36	NA	GND	AK36	GND	AK36	GND	
AK37	17	IO_L14N_VREF_17	AK37	IO_L14N_VREF_17	AK37	IO_L14N_VREF_17	
AK38	17	IO_L14P_17	AK38	IO_L14P_17	AK38	IO_L14P_17	
AK39	17	IO_L13N_17	AK39	IO_L13N_17	AK39	IO_L13N_17	
AK40	13	IO_L12P_VRN_13	AK40	IO_L12P_VRN_13	AK40	IO_L12P_VRN_13	
AK41	17	VCCO_17	AK41	VCCO_17	AK41	VCCO_17	
AK42	13	IO_L13N_13	AK42	IO_L13N_13	AK42	IO_L13N_13	
AL1	NA	MGTRXN1_118	AL1	MGTRXN1_118	AL1	MGTRXN1_118	
AL2	NA	GND	AL2	GND	AL2	GND	
AL3	NA	MGTAVCC_118	AL3	MGTAVCC_118	AL3	MGTAVCC_118	
AL4	NA	MGTAVCC_118	AL4	MGTAVCC_118	AL4	MGTAVCC_118	
AL5	18	IO_L2P_18	AL5	IO_L2P_18	AL5	IO_L2P_18	
AL6	26	IO_L16P_26	AL6	IO_L16P_26	AL6	IO_L16P_26	
AL7	26	IO_L16N_26	AL7	IO_L16N_26	AL7	IO_L16N_26	
AL8	26	VCCO_26	AL8	VCCO_26	AL8	VCCO_26	
AL9	26	IO_L14P_26	AL9	IO_L14P_26	AL9	IO_L14P_26	
AL10	26	IO_L14N_VREF_26	AL10	IO_L14N_VREF_26	AL10	IO_L14N_VREF_26	
AL11	NA	GND	AL11	UNUSED	AL11	UNUSED	NC
AL12	NA	GND	AL12	UNUSED	AL12	UNUSED	NC
AL13	NA	GND	AL13	GND	AL13	GND	
AL14	2	IO_L4P_FCS_B_2	AL14	IO_L4P_FCS_B_2	AL14	IO_L4P_FCS_B_2	
AL15	4	IO_L3P_GC_D9_4	AL15	IO_L3P_GC_D9_4	AL15	IO_L3P_GC_D9_4	
AL16	4	IO_L3N_GC_D8_4	AL16	IO_L3N_GC_D8_4	AL16	IO_L3N_GC_D8_4	
AL17	4	IO_L1N_GC_D12_4	AL17	IO_L1N_GC_D12_4	AL17	IO_L1N_GC_D12_4	
AL18	NA	GND	AL18	GND	AL18	GND	
AL19	6	IO_L18N_6	AL19	IO_L18N_6	AL19	IO_L18N_6	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AL20	8	IO_L3N_8	AL20	IO_L3N_8	AL20	IO_L3N_8	
AL21	8	IO_L0P_8	AL21	IO_L0P_8	AL21	IO_L0P_8	
AL22	8	IO_L0N_8	AL22	IO_L0N_8	AL22	IO_L0N_8	
AL23	NA	GND	AL23	GND	AL23	GND	
AL24	6	IO_L19N_6	AL24	IO_L19N_6	AL24	IO_L19N_6	
AL25	6	IO_L19P_6	AL25	IO_L19P_6	AL25	IO_L19P_6	
AL26	4	IO_L8N_CC_GC_4	AL26	IO_L8N_CC_GC_4	AL26	IO_L8N_CC_GC_4	
AL27	4	IO_L8P_CC_GC_4	AL27	IO_L8P_CC_GC_4	AL27	IO_L8P_CC_GC_4	
AL28	0	VCCO_0	AL28	VCCO_0	AL28	VCCO_0	
AL29	2	IO_L5N_CSO_B_2	AL29	IO_L5N_CSO_B_2	AL29	IO_L5N_CSO_B_2	
AL30	2	IO_L3P_A21_2	AL30	IO_L3P_A21_2	AL30	IO_L3P_A21_2	
AL31	25	IO_L19P_25	AL31	IO_L19P_25	AL31	IO_L19P_25	
AL32	25	IO_L18P_25	AL32	IO_L18P_25	AL32	IO_L18P_25	
AL33	NA	GND	AL33	GND	AL33	GND	
AL34	21	IO_L19P_21	AL34	IO_L19P_21	AL34	IO_L19P_21	
AL35	21	IO_L18N_21	AL35	IO_L18N_21	AL35	IO_L18N_21	
AL36	21	IO_L18P_21	AL36	IO_L18P_21	AL36	IO_L18P_21	
AL37	17	IO_L19N_17	AL37	IO_L19N_17	AL37	IO_L19N_17	
AL38	21	VCCO_21	AL38	VCCO_21	AL38	VCCO_21	
AL39	17	IO_L16P_17	AL39	IO_L16P_17	AL39	IO_L16P_17	
AL40	13	IO_L12N_VRP_13	AL40	IO_L12N_VRP_13	AL40	IO_L12N_VRP_13	
AL41	13	IO_L13P_13	AL41	IO_L13P_13	AL41	IO_L13P_13	
AL42	13	IO_L14P_13	AL42	IO_L14P_13	AL42	IO_L14P_13	
AM1	NA	MGTRXP1_118	AM1	MGTRXP1_118	AM1	MGTRXP1_118	
AM2	NA	MGTTXN1_118	AM2	MGTTXN1_118	AM2	MGTTXN1_118	
AM3	NA	MGTAVCCPLL_118	AM3	MGTAVCCPLL_118	AM3	MGTAVCCPLL_118	
AM4	NA	GND	AM4	GND	AM4	GND	
AM5	NA	GND	AM5	GND	AM5	GND	
AM6	26	IO_L18N_26	AM6	IO_L18N_26	AM6	IO_L18N_26	
AM7	26	IO_L19P_26	AM7	IO_L19P_26	AM7	IO_L19P_26	
AM8	26	IO_L19N_26	AM8	IO_L19N_26	AM8	IO_L19N_26	
AM9	26	IO_L8P_CC_26	AM9	IO_L8P_CC_26	AM9	IO_L8P_CC_26	
AM10	NA	GND	AM10	GND	AM10	GND	
AM11	NA	GND	AM11	UNUSED	AM11	UNUSED	NC
AM12	NA	GND	AM12	UNUSED	AM12	UNUSED	NC

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AM13	2	IO_L4N_VREF_FOE_B_MOSI_2	AM13	IO_L4N_VREF_FOE_B_MOSI_2	AM13	IO_L4N_VREF_FOE_B_MOSI_2	
AM14	2	IO_L8N_D2_FS2_2	AM14	IO_L8N_D2_FS2_2	AM14	IO_L8N_D2_FS2_2	
AM15	NA	GND	AM15	GND	AM15	GND	
AM16	4	IO_L5P_GC_4	AM16	IO_L5P_GC_4	AM16	IO_L5P_GC_4	
AM17	4	IO_L5N_GC_4	AM17	IO_L5N_GC_4	AM17	IO_L5N_GC_4	
AM18	6	IO_L10N_CC_6	AM18	IO_L10N_CC_6	AM18	IO_L10N_CC_6	
AM19	6	IO_L18P_6	AM19	IO_L18P_6	AM19	IO_L18P_6	
AM20	NA	GND	AM20	GND	AM20	GND	
AM21	8	IO_L19N_8	AM21	IO_L19N_8	AM21	IO_L19N_8	
AM22	8	IO_L16P_8	AM22	IO_L16P_8	AM22	IO_L16P_8	
AM23	8	IO_L16N_8	AM23	IO_L16N_8	AM23	IO_L16N_8	
AM24	6	IO_L15P_6	AM24	IO_L15P_6	AM24	IO_L15P_6	
AM25	NA	GND	AM25	GND	AM25	GND	
AM26	4	IO_L6N_GC_4	AM26	IO_L6N_GC_4	AM26	IO_L6N_GC_4	
AM27	4	IO_L6P_GC_4	AM27	IO_L6P_GC_4	AM27	IO_L6P_GC_4	
AM28	2	IO_L5P_FWE_B_2	AM28	IO_L5P_FWE_B_2	AM28	IO_L5P_FWE_B_2	
AM29	2	IO_L3N_A20_2	AM29	IO_L3N_A20_2	AM29	IO_L3N_A20_2	
AM30	NA	GND	AM30	GND	AM30	GND	
AM31	25	IO_L19N_25	AM31	IO_L19N_25	AM31	IO_L19N_25	
AM32	25	IO_L18N_25	AM32	IO_L18N_25	AM32	IO_L18N_25	
AM33	25	IO_L15N_25	AM33	IO_L15N_25	AM33	IO_L15N_25	
AM34	21	IO_L15N_21	AM34	IO_L15N_21	AM34	IO_L15N_21	
AM35	21	VCCO_21	AM35	VCCO_21	AM35	VCCO_21	
AM36	21	IO_L14P_21	AM36	IO_L14P_21	AM36	IO_L14P_21	
AM37	17	IO_L19P_17	AM37	IO_L19P_17	AM37	IO_L19P_17	
AM38	17	IO_L18N_17	AM38	IO_L18N_17	AM38	IO_L18N_17	
AM39	17	IO_L16N_17	AM39	IO_L16N_17	AM39	IO_L16N_17	
AM40	NA	GND	AM40	GND	AM40	GND	
AM41	13	IO_L15P_13	AM41	IO_L15P_13	AM41	IO_L15P_13	
AM42	13	IO_L14N_VREF_13	AM42	IO_L14N_VREF_13	AM42	IO_L14N_VREF_13	
AN1	NA	GND	AN1	UNPOPULATED	AN1	GND	
AN2	NA	MGTTXP1_118	AN2	MGTTXP1_118	AN2	MGTTXP1_118	
AN3	NA	MGTAVTTTX_118	AN3	MGTAVTTTX_118	AN3	MGTAVTTTX_118	
AN4	26	IO_L17P_26	AN4	IO_L17P_26	AN4	IO_L17P_26	
AN5	26	IO_L17N_26	AN5	IO_L17N_26	AN5	IO_L17N_26	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AN6	26	IO_L18P_26	AN6	IO_L18P_26	AN6	IO_L18P_26	
AN7	NA	GND	AN7	GND	AN7	GND	
AN8	26	IO_L11P_CC_26	AN8	IO_L11P_CC_26	AN8	IO_L11P_CC_26	
AN9	26	IO_L8N_CC_26	AN9	IO_L8N_CC_26	AN9	IO_L8N_CC_26	
AN10	NA	GND	AN10	UNUSED	AN10	UNUSED	NC
AN11	NA	GND	AN11	UNUSED	AN11	UNUSED	NC
AN12	NA	GND	AN12	GND	AN12	GND	
AN13	2	IO_L6P_D7_2	AN13	IO_L6P_D7_2	AN13	IO_L6P_D7_2	
AN14	2	IO_L8P_D3_2	AN14	IO_L8P_D3_2	AN14	IO_L8P_D3_2	
AN15	4	IO_L7P_GC_VRN_4	AN15	IO_L7P_GC_VRN_4	AN15	IO_L7P_GC_VRN_4	
AN16	4	IO_L7N_GC_VRP_4	AN16	IO_L7N_GC_VRP_4	AN16	IO_L7N_GC_VRP_4	
AN17	NA	GND	AN17	GND	AN17	GND	
AN18	6	IO_L10P_CC_6	AN18	IO_L10P_CC_6	AN18	IO_L10P_CC_6	
AN19	6	IO_L9N_CC_6	AN19	IO_L9N_CC_6	AN19	IO_L9N_CC_6	
AN20	6	IO_L9P_CC_6	AN20	IO_L9P_CC_6	AN20	IO_L9P_CC_6	
AN21	8	IO_L19P_8	AN21	IO_L19P_8	AN21	IO_L19P_8	
AN22	NA	GND	AN22	GND	AN22	GND	
AN23	8	IO_L17P_8	AN23	IO_L17P_8	AN23	IO_L17P_8	
AN24	6	IO_L15N_6	AN24	IO_L15N_6	AN24	IO_L15N_6	
AN25	6	IO_L13P_6	AN25	IO_L13P_6	AN25	IO_L13P_6	
AN26	6	IO_L11P_CC_6	AN26	IO_L11P_CC_6	AN26	IO_L11P_CC_6	
AN27	NA	GND	AN27	GND	AN27	GND	
AN28	4	IO_L4N_GC_VREF_4	AN28	IO_L4N_GC_VREF_4	AN28	IO_L4N_GC_VREF_4	
AN29	4	IO_L2P_GC_D11_4	AN29	IO_L2P_GC_D11_4	AN29	IO_L2P_GC_D11_4	
AN30	4	IO_L0P_GC_D15_4	AN30	IO_L0P_GC_D15_4	AN30	IO_L0P_GC_D15_4	
AN31	25	IO_L12N_VRP_25	AN31	IO_L12N_VRP_25	AN31	IO_L12N_VRP_25	
AN32	NA	GND	AN32	GND	AN32	GND	
AN33	25	IO_L15P_25	AN33	IO_L15P_25	AN33	IO_L15P_25	
AN34	21	IO_L15P_21	AN34	IO_L15P_21	AN34	IO_L15P_21	
AN35	21	IO_L14N_VREF_21	AN35	IO_L14N_VREF_21	AN35	IO_L14N_VREF_21	
AN36	21	IO_L13N_21	AN36	IO_L13N_21	AN36	IO_L13N_21	
AN37	NA	GND	AN37	GND	AN37	GND	
AN38	17	IO_L18P_17	AN38	IO_L18P_17	AN38	IO_L18P_17	
AN39	17	IO_L17P_17	AN39	IO_L17P_17	AN39	IO_L17P_17	
AN40	17	IO_L8P_CC_17	AN40	IO_L8P_CC_17	AN40	IO_L8P_CC_17	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AN41	13	IO_L15N_13	AN41	IO_L15N_13	AN41	IO_L15N_13	
AN42	NA	GND	AN42	GND	AN42	GND	
AP1	NA	GND	AP1	UNPOPULATED	AP1	GND	
AP2	NA	MGTTXP0_122	AP2	MGTTXP0_122	AP2	MGTTXP0_122	
AP3	NA	MGTAVTTTX_122	AP3	MGTAVTTTX_122	AP3	MGTAVTTTX_122	
AP4	NA	GND	AP4	GND	AP4	GND	
AP5	26	IO_L15N_26	AP5	IO_L15N_26	AP5	IO_L15N_26	
AP6	26	IO_L15P_26	AP6	IO_L15P_26	AP6	IO_L15P_26	
AP7	26	IO_L13P_26	AP7	IO_L13P_26	AP7	IO_L13P_26	
AP8	26	IO_L11N_CC_26	AP8	IO_L11N_CC_26	AP8	IO_L11N_CC_26	
AP9	NA	GND	AP9	UNUSED	AP9	UNUSED	NC
AP10	NA	GND	AP10	UNUSED	AP10	UNUSED	NC
AP11	NA	GND	AP11	UNUSED	AP11	UNUSED	NC
AP12	NA	GND	AP12	UNUSED	AP12	UNUSED	NC
AP13	2	IO_L6N_D6_2	AP13	IO_L6N_D6_2	AP13	IO_L6N_D6_2	
AP14	NA	GND	AP14	GND	AP14	GND	
AP15	4	IO_L9N_CC_GC_4	AP15	IO_L9N_CC_GC_4	AP15	IO_L9N_CC_GC_4	
AP16	4	IO_L9P_CC_GC_4	AP16	IO_L9P_CC_GC_4	AP16	IO_L9P_CC_GC_4	
AP17	6	IO_L7P_6	AP17	IO_L7P_6	AP17	IO_L7P_6	
AP18	6	IO_L12N_VRP_6	AP18	IO_L12N_VRP_6	AP18	IO_L12N_VRP_6	
AP19	8	VCCO_8	AP19	VCCO_8	AP19	VCCO_8	
AP20	8	IO_L18P_8	AP20	IO_L18P_8	AP20	IO_L18P_8	
AP21	8	IO_L18N_8	AP21	IO_L18N_8	AP21	IO_L18N_8	
AP22	8	IO_L14N_VREF_8	AP22	IO_L14N_VREF_8	AP22	IO_L14N_VREF_8	
AP23	8	IO_L17N_8	AP23	IO_L17N_8	AP23	IO_L17N_8	
AP24	NA	GND	AP24	GND	AP24	GND	
AP25	6	IO_L13N_6	AP25	IO_L13N_6	AP25	IO_L13N_6	
AP26	6	IO_L11N_CC_6	AP26	IO_L11N_CC_6	AP26	IO_L11N_CC_6	
AP27	4	IO_L4P_GC_4	AP27	IO_L4P_GC_4	AP27	IO_L4P_GC_4	
AP28	4	IO_L2N_GC_D10_4	AP28	IO_L2N_GC_D10_4	AP28	IO_L2N_GC_D10_4	
AP29	NA	GND	AP29	GND	AP29	GND	
AP30	4	IO_L0N_GC_D14_4	AP30	IO_L0N_GC_D14_4	AP30	IO_L0N_GC_D14_4	
AP31	25	IO_L12P_VRN_25	AP31	IO_L12P_VRN_25	AP31	IO_L12P_VRN_25	
AP32	25	IO_L13N_25	AP32	IO_L13N_25	AP32	IO_L13N_25	
AP33	25	IO_L14N_VREF_25	AP33	IO_L14N_VREF_25	AP33	IO_L14N_VREF_25	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AP34	NA	GND	AP34	GND	AP34	GND	
AP35	21	IO_L13P_21	AP35	IO_L13P_21	AP35	IO_L13P_21	
AP36	21	IO_L12N_VRP_21	AP36	IO_L12N_VRP_21	AP36	IO_L12N_VRP_21	
AP37	21	IO_L12P_VRN_21	AP37	IO_L12P_VRN_21	AP37	IO_L12P_VRN_21	
AP38	17	IO_L17N_17	AP38	IO_L17N_17	AP38	IO_L17N_17	
AP39	25	VCCO_25	AP39	VCCO_25	AP39	VCCO_25	
AP40	17	IO_L8N_CC_17	AP40	IO_L8N_CC_17	AP40	IO_L8N_CC_17	
AP41	13	IO_L16N_13	AP41	IO_L16N_13	AP41	IO_L16N_13	
AP42	13	IO_L16P_13	AP42	IO_L16P_13	AP42	IO_L16P_13	
AR1	NA	MGTRXP0_122	AR1	MGTRXP0_122	AR1	MGTRXP0_122	
AR2	NA	MGTTXN0_122	AR2	MGTTXN0_122	AR2	MGTTXN0_122	
AR3	NA	MGTAVTTRX_122	AR3	MGTAVTTRX_122	AR3	MGTAVTTRX_122	
AR4	NA	GND	AR4	GND	AR4	GND	
AR5	26	IO_L2N_26	AR5	IO_L2N_26	AR5	IO_L2N_26	
AR6	NA	GND	AR6	GND	AR6	GND	
AR7	26	IO_L0N_26	AR7	IO_L0N_26	AR7	IO_L0N_26	
AR8	26	IO_L13N_26	AR8	IO_L13N_26	AR8	IO_L13N_26	
AR9	NA	GND	AR9	UNUSED	AR9	UNUSED	NC
AR10	NA	GND	AR10	UNUSED	AR10	UNUSED	NC
AR11	NA	GND	AR11	GND	AR11	GND	
AR12	NA	GND	AR12	UNUSED	AR12	UNUSED	NC
AR13	NA	GND	AR13	UNUSED	AR13	UNUSED	NC
AR14	6	IO_L1N_6	AR14	IO_L1N_6	AR14	IO_L1N_6	
AR15	6	IO_L3N_6	AR15	IO_L3N_6	AR15	IO_L3N_6	
AR16	4	VCCO_4	AR16	VCCO_4	AR16	VCCO_4	
AR17	6	IO_L7N_6	AR17	IO_L7N_6	AR17	IO_L7N_6	
AR18	6	IO_L12P_VRN_6	AR18	IO_L12P_VRN_6	AR18	IO_L12P_VRN_6	
AR19	6	IO_L14N_VREF_6	AR19	IO_L14N_VREF_6	AR19	IO_L14N_VREF_6	
AR20	8	IO_L7P_8	AR20	IO_L7P_8	AR20	IO_L7P_8	
AR21	NA	GND	AR21	GND	AR21	GND	
AR22	8	IO_L15P_8	AR22	IO_L15P_8	AR22	IO_L15P_8	
AR23	8	IO_L14P_8	AR23	IO_L14P_8	AR23	IO_L14P_8	
AR24	8	IO_L8N_CC_8	AR24	IO_L8N_CC_8	AR24	IO_L8N_CC_8	
AR25	8	IO_L6P_8	AR25	IO_L6P_8	AR25	IO_L6P_8	
AR26	2	VCCO_2	AR26	VCCO_2	AR26	VCCO_2	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AR27	6	IO_L8N_CC_6	AR27	IO_L8N_CC_6	AR27	IO_L8N_CC_6	
AR28	6	IO_L0N_6	AR28	IO_L0N_6	AR28	IO_L0N_6	
AR29	6	IO_L0P_6	AR29	IO_L0P_6	AR29	IO_L0P_6	
AR30	6	IO_L2P_6	AR30	IO_L2P_6	AR30	IO_L2P_6	
AR31	NA	GND	AR31	GND	AR31	GND	
AR32	25	IO_L13P_25	AR32	IO_L13P_25	AR32	IO_L13P_25	
AR33	25	IO_L14P_25	AR33	IO_L14P_25	AR33	IO_L14P_25	
AR34	25	IO_L7N_25	AR34	IO_L7N_25	AR34	IO_L7N_25	
AR35	25	IO_L7P_25	AR35	IO_L7P_25	AR35	IO_L7P_25	
AR36	25	VCCO_25	AR36	VCCO_25	AR36	VCCO_25	
AR37	21	IO_L7P_21	AR37	IO_L7P_21	AR37	IO_L7P_21	
AR38	21	IO_L6N_21	AR38	IO_L6N_21	AR38	IO_L6N_21	
AR39	17	IO_L11N_CC_17	AR39	IO_L11N_CC_17	AR39	IO_L11N_CC_17	
AR40	17	IO_L9P_CC_17	AR40	IO_L9P_CC_17	AR40	IO_L9P_CC_17	
AR41	NA	GND	AR41	GND	AR41	GND	
AR42	13	IO_L17P_13	AR42	IO_L17P_13	AR42	IO_L17P_13	
AT1	NA	MGTRXN0_122	AT1	MGTRXN0_122	AT1	MGTRXN0_122	
AT2	NA	GND	AT2	GND	AT2	GND	
AT3	NA	MGTREFCLKN_122	AT3	MGTREFCLKN_122	AT3	MGTREFCLKN_122	
AT4	NA	MGTREFCLKP_122	AT4	MGTREFCLKP_122	AT4	MGTREFCLKP_122	
AT5	26	IO_L4P_26	AT5	IO_L4P_26	AT5	IO_L4P_26	
AT6	26	IO_L2P_26	AT6	IO_L2P_26	AT6	IO_L2P_26	
AT7	26	IO_L0P_26	AT7	IO_L0P_26	AT7	IO_L0P_26	
AT8	NA	GND	AT8	GND	AT8	GND	
AT9	NA	GND	AT9	UNUSED	AT9	UNUSED	NC
AT10	NA	GND	AT10	UNUSED	AT10	UNUSED	NC
AT11	NA	GND	AT11	UNUSED	AT11	UNUSED	NC
AT12	NA	GND	AT12	UNUSED	AT12	UNUSED	NC
AT13	4	VCCO_4	AT13	VCCO_4	AT13	VCCO_4	
AT14	6	IO_L1P_6	AT14	IO_L1P_6	AT14	IO_L1P_6	
AT15	6	IO_L3P_6	AT15	IO_L3P_6	AT15	IO_L3P_6	
AT16	6	IO_L5N_6	AT16	IO_L5N_6	AT16	IO_L5N_6	
AT17	6	IO_L5P_6	AT17	IO_L5P_6	AT17	IO_L5P_6	
AT18	NA	GND	AT18	GND	AT18	GND	
AT19	6	IO_L14P_6	AT19	IO_L14P_6	AT19	IO_L14P_6	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AT20	8	IO_L7N_8	AT20	IO_L7N_8	AT20	IO_L7N_8	
AT21	8	IO_L9N_CC_8	AT21	IO_L9N_CC_8	AT21	IO_L9N_CC_8	
AT22	8	IO_L15N_8	AT22	IO_L15N_8	AT22	IO_L15N_8	
AT23	6	VCCO_6	AT23	VCCO_6	AT23	VCCO_6	
AT24	8	IO_L8P_CC_8	AT24	IO_L8P_CC_8	AT24	IO_L8P_CC_8	
AT25	8	IO_L6N_8	AT25	IO_L6N_8	AT25	IO_L6N_8	
AT26	6	IO_L8P_CC_6	AT26	IO_L8P_CC_6	AT26	IO_L8P_CC_6	
AT27	6	IO_L6N_6	AT27	IO_L6N_6	AT27	IO_L6N_6	
AT28	NA	GND	AT28	GND	AT28	GND	
AT29	6	IO_L4P_6	AT29	IO_L4P_6	AT29	IO_L4P_6	
AT30	6	IO_L2N_6	AT30	IO_L2N_6	AT30	IO_L2N_6	
AT31	25	IO_L11N_CC_25	AT31	IO_L11N_CC_25	AT31	IO_L11N_CC_25	
AT32	25	IO_L11P_CC_25	AT32	IO_L11P_CC_25	AT32	IO_L11P_CC_25	
AT33	29	VCCO_29	AT33	VCCO_29	AT33	VCCO_29	
AT34	25	IO_L6N_25	AT34	IO_L6N_25	AT34	IO_L6N_25	
AT35	25	IO_L5N_25	AT35	IO_L5N_25	AT35	IO_L5N_25	
AT36	21	IO_L7N_21	AT36	IO_L7N_21	AT36	IO_L7N_21	
AT37	21	IO_L6P_21	AT37	IO_L6P_21	AT37	IO_L6P_21	
AT38	NA	GND	AT38	GND	AT38	GND	
AT39	17	IO_L11P_CC_17	AT39	IO_L11P_CC_17	AT39	IO_L11P_CC_17	
AT40	17	IO_L9N_CC_17	AT40	IO_L9N_CC_17	AT40	IO_L9N_CC_17	
AT41	13	IO_L18P_13	AT41	IO_L18P_13	AT41	IO_L18P_13	
AT42	13	IO_L17N_13	AT42	IO_L17N_13	AT42	IO_L17N_13	
AU1	NA	MGTRXN1_122	AU1	MGTRXN1_122	AU1	MGTRXN1_122	
AU2	NA	GND	AU2	GND	AU2	GND	
AU3	NA	MGTAVCC_122	AU3	MGTAVCC_122	AU3	MGTAVCC_122	
AU4	NA	MGTAVCC_122	AU4	MGTAVCC_122	AU4	MGTAVCC_122	
AU5	NA	GND	AU5	GND	AU5	GND	
AU6	26	IO_L4N_VREF_26	AU6	IO_L4N_VREF_26	AU6	IO_L4N_VREF_26	
AU7	NA	GND	AU7	UNUSED	AU7	UNUSED	NC
AU8	NA	GND	AU8	UNUSED	AU8	UNUSED	NC
AU9	NA	GND	AU9	UNUSED	AU9	UNUSED	NC
AU10	NA	GND	AU10	UNUSED	AU10	UNUSED	NC
AU11	NA	GND	AU11	UNUSED	AU11	UNUSED	NC
AU12	NA	GND	AU12	UNUSED	AU12	UNUSED	NC

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AU13	NA	GND	AU13	UNUSED	AU13	UNUSED	NC
AU14	NA	GND	AU14	UNUSED	AU14	UNUSED	NC
AU15	NA	GND	AU15	GND	AU15	GND	
AU16	NA	GND	AU16	UNUSED	AU16	UNUSED	NC
AU17	NA	GND	AU17	UNUSED	AU17	UNUSED	NC
AU18	8	IO_L5N_8	AU18	IO_L5N_8	AU18	IO_L5N_8	
AU19	8	IO_L5P_8	AU19	IO_L5P_8	AU19	IO_L5P_8	
AU20	8	VCCO_8	AU20	VCCO_8	AU20	VCCO_8	
AU21	8	IO_L9P_CC_8	AU21	IO_L9P_CC_8	AU21	IO_L9P_CC_8	
AU22	8	IO_L12N_VRP_8	AU22	IO_L12N_VRP_8	AU22	IO_L12N_VRP_8	
AU23	8	IO_L12P_VRN_8	AU23	IO_L12P_VRN_8	AU23	IO_L12P_VRN_8	
AU24	8	IO_L11P_CC_8	AU24	IO_L11P_CC_8	AU24	IO_L11P_CC_8	
AU25	NA	GND	AU25	GND	AU25	GND	
AU26	8	IO_L4P_8	AU26	IO_L4P_8	AU26	IO_L4P_8	
AU27	8	IO_L4N_VREF_8	AU27	IO_L4N_VREF_8	AU27	IO_L4N_VREF_8	
AU28	6	IO_L6P_6	AU28	IO_L6P_6	AU28	IO_L6P_6	
AU29	6	IO_L4N_VREF_6	AU29	IO_L4N_VREF_6	AU29	IO_L4N_VREF_6	
AU30	NA	GND	AU30	UNUSED	AU30	UNUSED	NC
AU31	25	IO_L10N_CC_25	AU31	IO_L10N_CC_25	AU31	IO_L10N_CC_25	
AU32	25	IO_L8P_CC_25	AU32	IO_L8P_CC_25	AU32	IO_L8P_CC_25	
AU33	25	IO_L8N_CC_25	AU33	IO_L8N_CC_25	AU33	IO_L8N_CC_25	
AU34	25	IO_L6P_25	AU34	IO_L6P_25	AU34	IO_L6P_25	
AU35	NA	GND	AU35	GND	AU35	GND	
AU36	25	IO_L5P_25	AU36	IO_L5P_25	AU36	IO_L5P_25	
AU37	21	IO_L5N_21	AU37	IO_L5N_21	AU37	IO_L5N_21	
AU38	21	IO_L5P_21	AU38	IO_L5P_21	AU38	IO_L5P_21	
AU39	17	IO_L10N_CC_17	AU39	IO_L10N_CC_17	AU39	IO_L10N_CC_17	
AU40	25	VCCO_25	AU40	VCCO_25	AU40	VCCO_25	
AU41	13	IO_L18N_13	AU41	IO_L18N_13	AU41	IO_L18N_13	
AU42	13	IO_L19P_13	AU42	IO_L19P_13	AU42	IO_L19P_13	
AV1	NA	MGTRXP1_122	AV1	MGTRXP1_122	AV1	MGTRXP1_122	
AV2	NA	MGTTXN1_122	AV2	MGTTXN1_122	AV2	MGTTXN1_122	
AV3	NA	MGTAVCCPLL_122	AV3	MGTAVCCPLL_122	AV3	MGTAVCCPLL_122	
AV4	NA	GND	AV4	GND	AV4	GND	
AV5	26	IO_L6N_26	AV5	IO_L6N_26	AV5	IO_L6N_26	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AV6	26	IO_L6P_26	AV6	IO_L6P_26	AV6	IO_L6P_26	
AV7	NA	GND	AV7	UNUSED	AV7	UNUSED	NC
AV8	NA	GND	AV8	UNUSED	AV8	UNUSED	NC
AV9	NA	GND	AV9	UNUSED	AV9	UNUSED	NC
AV10	NA	GND	AV10	UNUSED	AV10	UNUSED	NC
AV11	NA	GND	AV11	UNUSED	AV11	UNUSED	NC
AV12	NA	GND	AV12	GND	AV12	GND	
AV13	NA	GND	AV13	UNUSED	AV13	UNUSED	NC
AV14	NA	GND	AV14	UNUSED	AV14	UNUSED	NC
AV15	NA	GND	AV15	UNUSED	AV15	UNUSED	NC
AV16	NA	GND	AV16	UNUSED	AV16	UNUSED	NC
AV17	8	VCCO_8	AV17	VCCO_8	AV17	VCCO_8	
AV18	NA	GND	AV18	UNUSED	AV18	UNUSED	NC
AV19	NA	GND	AV19	UNUSED	AV19	UNUSED	NC
AV20	8	IO_L10N_CC_8	AV20	IO_L10N_CC_8	AV20	IO_L10N_CC_8	
AV21	8	IO_L10P_CC_8	AV21	IO_L10P_CC_8	AV21	IO_L10P_CC_8	
AV22	NA	GND	AV22	GND	AV22	GND	
AV23	8	IO_L13P_8	AV23	IO_L13P_8	AV23	IO_L13P_8	
AV24	8	IO_L13N_8	AV24	IO_L13N_8	AV24	IO_L13N_8	
AV25	8	IO_L11N_CC_8	AV25	IO_L11N_CC_8	AV25	IO_L11N_CC_8	
AV26	NA	GND	AV26	UNUSED	AV26	UNUSED	NC
AV27	2	VCCO_2	AV27	VCCO_2	AV27	VCCO_2	
AV28	NA	GND	AV28	UNUSED	AV28	UNUSED	NC
AV29	NA	GND	AV29	UNUSED	AV29	UNUSED	NC
AV30	NA	GND	AV30	UNUSED	AV30	UNUSED	NC
AV31	25	IO_L10P_CC_25	AV31	IO_L10P_CC_25	AV31	IO_L10P_CC_25	
AV32	NA	GND	AV32	GND	AV32	GND	
AV33	25	IO_L9P_CC_25	AV33	IO_L9P_CC_25	AV33	IO_L9P_CC_25	
AV34	25	IO_L9N_CC_25	AV34	IO_L9N_CC_25	AV34	IO_L9N_CC_25	
AV35	25	IO_L4P_25	AV35	IO_L4P_25	AV35	IO_L4P_25	
AV36	25	IO_L4N_VREF_25	AV36	IO_L4N_VREF_25	AV36	IO_L4N_VREF_25	
AV37	29	VCCO_29	AV37	VCCO_29	AV37	VCCO_29	
AV38	21	IO_L4N_VREF_21	AV38	IO_L4N_VREF_21	AV38	IO_L4N_VREF_21	
AV39	21	IO_L4P_21	AV39	IO_L4P_21	AV39	IO_L4P_21	
AV40	17	IO_L10P_CC_17	AV40	IO_L10P_CC_17	AV40	IO_L10P_CC_17	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AV41	13	IO_L19N_13	AV41	IO_L19N_13	AV41	IO_L19N_13	
AV42	NA	GND	AV42	GND	AV42	GND	
AW1	NA	GND	AW1	UNPOPULATED	AW1	GND	
AW2	NA	MGTTXP1_122	AW2	MGTTXP1_122	AW2	MGTTXP1_122	
AW3	NA	MGTAVTTTX_122	AW3	MGTAVTTTX_122	AW3	MGTAVTTTX_122	
AW4	NA	MGTREFCLKP_126	AW4	MGTREFCLKP_126	AW4	MGTREFCLKP_126	
AW5	NA	MGTAVCC_126	AW5	MGTAVCC_126	AW5	MGTAVCC_126	
AW6	NA	GND	AW6	GND	AW6	GND	
AW7	NA	GND	AW7	UNUSED	AW7	UNUSED	NC
AW8	NA	GND	AW8	GND	AW8	GND	
AW9	NA	MGTREFCLKP_130	AW9	MGTREFCLKP_130	AW9	MGTREFCLKP_130	
AW10	NA	MGTAVCC_130	AW10	MGTAVCC_130	AW10	MGTAVCC_130	
AW11	NA	GND	AW11	GND	AW11	GND	
AW12	NA	GND	AW12	UNUSED	AW12	UNUSED	NC
AW13	NA	GND	AW13	UNUSED	AW13	UNUSED	NC
AW14	NA	GND	AW14	GND	AW14	GND	
AW15	NA	GND	AW15	UNUSED	AW15	UNUSED	NC
AW16	NA	GND	AW16	MGTAVCC_134	AW16	MGTAVCC_134	NC
AW17	NA	GND	AW17	GND	AW17	GND	
AW18	NA	GND	AW18	UNUSED	AW18	UNUSED	NC
AW19	NA	GND	AW19	GND	AW19	GND	
AW20	NA	GND	AW20	UNUSED	AW20	UNUSED	NC
AW21	NA	GND	AW21	UNUSED	AW21	UNUSED	NC
AW22	NA	GND	AW22	UNUSED	AW22	UNUSED	NC
AW23	NA	GND	AW23	UNUSED	AW23	UNUSED	NC
AW24	6	VCCO_6	AW24	VCCO_6	AW24	VCCO_6	
AW25	NA	GND	AW25	UNUSED	AW25	UNUSED	NC
AW26	NA	GND	AW26	UNUSED	AW26	UNUSED	NC
AW27	NA	GND	AW27	UNUSED	AW27	UNUSED	NC
AW28	NA	GND	AW28	UNUSED	AW28	UNUSED	NC
AW29	NA	GND	AW29	GND	AW29	GND	
AW30	NA	GND	AW30	UNUSED	AW30	UNUSED	NC
AW31	29	IO_L19N_29	AW31	IO_L19N_29	AW31	IO_L19N_29	
AW32	29	IO_L15N_29	AW32	IO_L15N_29	AW32	IO_L15N_29	
AW33	29	IO_L15P_29	AW33	IO_L15P_29	AW33	IO_L15P_29	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AW34	29	VCCO_29	AW34	VCCO_29	AW34	VCCO_29	
AW35	29	IO_L11N_CC_29	AW35	IO_L11N_CC_29	AW35	IO_L11N_CC_29	
AW36	29	IO_L9N_CC_29	AW36	IO_L9N_CC_29	AW36	IO_L9N_CC_29	
AW37	29	IO_L6N_29	AW37	IO_L6N_29	AW37	IO_L6N_29	
AW38	29	IO_L7P_29	AW38	IO_L7P_29	AW38	IO_L7P_29	
AW39	NA	GND	AW39	GND	AW39	GND	
AW40	29	IO_L1N_29	AW40	IO_L1N_29	AW40	IO_L1N_29	
AW41	29	IO_L1P_29	AW41	IO_L1P_29	AW41	IO_L1P_29	
AW42	29	IO_L0N_29	AW42	IO_L0N_29	AW42	IO_L0N_29	
AY1	NA	MGTAVTTTX_126	AY1	MGTAVTTTX_126	AY1	MGTAVTTTX_126	
AY2	NA	MGTAVTTRX_126	AY2	MGTAVTTRX_126	AY2	MGTAVTTRX_126	
AY3	NA	MGTAVCC_126	AY3	MGTAVCC_126	AY3	MGTAVCC_126	
AY4	NA	MGTREFCLKN_126	AY4	MGTREFCLKN_126	AY4	MGTREFCLKN_126	
AY5	NA	MGTAVCCPLL_126	AY5	MGTAVCCPLL_126	AY5	MGTAVCCPLL_126	
AY6	NA	MGTAVTTTX_126	AY6	MGTAVTTTX_126	AY6	MGTAVTTTX_126	
AY7	NA	MGTAVTTTX_130	AY7	MGTAVTTTX_130	AY7	MGTAVTTTX_130	
AY8	NA	MGTAVTTRX_130	AY8	MGTAVTTRX_130	AY8	MGTAVTTRX_130	
AY9	NA	MGTREFCLKN_130	AY9	MGTREFCLKN_130	AY9	MGTREFCLKN_130	
AY10	NA	MGTAVCC_130	AY10	MGTAVCC_130	AY10	MGTAVCC_130	
AY11	NA	MGTAVCCPLL_130	AY11	MGTAVCCPLL_130	AY11	MGTAVCCPLL_130	
AY12	NA	MGTAVTTTX_130	AY12	MGTAVTTTX_130	AY12	MGTAVTTTX_130	
AY13	NA	GND	AY13	UNUSED	AY13	UNUSED	NC
AY14	NA	GND	AY14	UNUSED	AY14	UNUSED	NC
AY15	NA	GND	AY15	UNUSED	AY15	UNUSED	NC
AY16	NA	GND	AY16	MGTAVCC_134	AY16	MGTAVCC_134	NC
AY17	NA	GND	AY17	UNUSED	AY17	UNUSED	NC
AY18	NA	GND	AY18	UNUSED	AY18	UNUSED	NC
AY19	NA	GND	AY19	UNUSED	AY19	UNUSED	NC
AY20	NA	GND	AY20	UNUSED	AY20	UNUSED	NC
AY21	6	VCCO_6	AY21	VCCO_6	AY21	VCCO_6	
AY22	NA	GND	AY22	UNUSED	AY22	UNUSED	NC
AY23	NA	GND	AY23	UNUSED	AY23	UNUSED	NC
AY24	NA	GND	AY24	UNUSED	AY24	UNUSED	NC
AY25	NA	GND	AY25	UNUSED	AY25	UNUSED	NC
AY26	NA	GND	AY26	GND	AY26	GND	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
AY27	NA	GND	AY27	UNUSED	AY27	UNUSED	NC
AY28	NA	GND	AY28	UNUSED	AY28	UNUSED	NC
AY29	NA	GND	AY29	UNUSED	AY29	UNUSED	NC
AY30	29	IO_L19P_29	AY30	IO_L19P_29	AY30	IO_L19P_29	
AY31	NA	GND	AY31	UNUSED	AY31	UNUSED	NC
AY32	29	IO_L16P_29	AY32	IO_L16P_29	AY32	IO_L16P_29	
AY33	29	IO_L14P_29	AY33	IO_L14P_29	AY33	IO_L14P_29	
AY34	29	IO_L14N_VREF_29	AY34	IO_L14N_VREF_29	AY34	IO_L14N_VREF_29	
AY35	29	IO_L11P_CC_29	AY35	IO_L11P_CC_29	AY35	IO_L11P_CC_29	
AY36	NA	GND	AY36	GND	AY36	GND	
AY37	29	IO_L9P_CC_29	AY37	IO_L9P_CC_29	AY37	IO_L9P_CC_29	
AY38	29	IO_L6P_29	AY38	IO_L6P_29	AY38	IO_L6P_29	
AY39	29	IO_L7N_29	AY39	IO_L7N_29	AY39	IO_L7N_29	
AY40	29	IO_L2P_29	AY40	IO_L2P_29	AY40	IO_L2P_29	
AY41	NA	GND	AY41	GND	AY41	GND	
AY42	29	IO_L0P_29	AY42	IO_L0P_29	AY42	IO_L0P_29	
BA1	NA	GND	BA1	MGTTXP0_126	BA1	UNPOPULATED	
BA2	NA	GND	BA2	MGTTXN0_126	BA2	MGTTXN0_126	NC
BA3	NA	GND	BA3	GND	BA3	GND	
BA4	NA	GND	BA4	GND	BA4	GND	
BA5	NA	MGTTXN1_126	BA5	MGTTXN1_126	BA5	MGTTXN1_126	
BA6	NA	MGTTXP1_126	BA6	MGTTXP1_126	BA6	MGTTXP1_126	
BA7	NA	MGTTXP0_130	BA7	MGTTXP0_130	BA7	MGTTXP0_130	
BA8	NA	MGTTXN0_130	BA8	MGTTXN0_130	BA8	MGTTXN0_130	
BA9	NA	GND	BA9	GND	BA9	GND	
BA10	NA	GND	BA10	GND	BA10	GND	
BA11	NA	MGTTXN1_130	BA11	MGTTXN1_130	BA11	MGTTXN1_130	
BA12	NA	MGTTXP1_130	BA12	MGTTXP1_130	BA12	MGTTXP1_130	
BA13	NA	GND	BA13	UNUSED	BA13	UNUSED	NC
BA14	NA	GND	BA14	UNUSED	BA14	UNUSED	NC
BA15	NA	GND	BA15	GND	BA15	GND	
BA16	NA	GND	BA16	GND	BA16	GND	
BA17	NA	GND	BA17	UNUSED	BA17	UNUSED	NC
BA18	NA	GND	BA18	UNUSED	BA18	UNUSED	NC
BA19	NA	GND	BA19	UNUSED	BA19	UNUSED	NC

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
BA20	NA	GND	BA20	UNUSED	BA20	UNUSED	NC
BA21	NA	GND	BA21	UNUSED	BA21	UNUSED	NC
BA22	NA	GND	BA22	UNUSED	BA22	UNUSED	NC
BA23	NA	GND	BA23	GND	BA23	GND	
BA24	NA	GND	BA24	UNUSED	BA24	UNUSED	NC
BA25	NA	GND	BA25	UNUSED	BA25	UNUSED	NC
BA26	NA	GND	BA26	UNUSED	BA26	UNUSED	NC
BA27	NA	GND	BA27	UNUSED	BA27	UNUSED	NC
BA28	NA	GND	BA28	UNUSED	BA28	UNUSED	NC
BA29	NA	GND	BA29	UNUSED	BA29	UNUSED	NC
BA30	29	IO_L18P_29	BA30	IO_L18P_29	BA30	IO_L18P_29	
BA31	29	IO_L18N_29	BA31	IO_L18N_29	BA31	IO_L18N_29	
BA32	29	IO_L16N_29	BA32	IO_L16N_29	BA32	IO_L16N_29	
BA33	NA	GND	BA33	GND	BA33	GND	
BA34	29	IO_L13N_29	BA34	IO_L13N_29	BA34	IO_L13N_29	
BA35	29	IO_L12N_VRP_29	BA35	IO_L12N_VRP_29	BA35	IO_L12N_VRP_29	
BA36	29	IO_L10N_CC_29	BA36	IO_L10N_CC_29	BA36	IO_L10N_CC_29	
BA37	29	IO_L8N_CC_29	BA37	IO_L8N_CC_29	BA37	IO_L8N_CC_29	
BA38	NA	GND	BA38	GND	BA38	GND	
BA39	29	IO_L5N_29	BA39	IO_L5N_29	BA39	IO_L5N_29	
BA40	29	IO_L4P_29	BA40	IO_L4P_29	BA40	IO_L4P_29	
BA41	29	IO_L2N_29	BA41	IO_L2N_29	BA41	IO_L2N_29	
BA42	29	GND	BA42	IO_L3P_29	BA42	UNPOPULATED	
BB2	NA	GND	BB2	MGTRXP0_126	BB2	UNPOPULATED	
BB3	NA	GND	BB3	MGTRXN0_126	BB3	MGTRXN0_126	NC
BB4	NA	MGTRXN1_126	BB4	MGTRXN1_126	BB4	MGTRXN1_126	
BB5	NA	MGTRXP1_126	BB5	MGTRXP1_126	BB5	MGTRXP1_126	
BB6	NA	GND	BB6	UNPOPULATED	BB6	GND	
BB7	NA	GND	BB7	UNPOPULATED	BB7	GND	
BB8	NA	MGTRXP0_130	BB8	MGTRXP0_130	BB8	MGTRXP0_130	
BB9	NA	MGTRXN0_130	BB9	MGTRXN0_130	BB9	MGTRXN0_130	
BB10	NA	MGTRXN1_130	BB10	MGTRXN1_130	BB10	MGTRXN1_130	
BB11	NA	MGTRXP1_130	BB11	MGTRXP1_130	BB11	MGTRXP1_130	
BB12	NA	GND	BB12	UNPOPULATED	BB12	GND	
BB13	NA	GND	BB13	UNPOPULATED	BB13	GND	

Table 8-1: **Pin Cross-Reference, Virtex-5QV FPGA to Virtex-5 FPGA *(Continued)***

Super-Set Footprint (FP1760)			Virtex-5 FPGA XC5VFX130T (FF1738)		Virtex-5QV FPGA XQR5VFX130 (CF1752)		Note
Pin	Bank	Name	Pin	Name	Pin	Name	
BB14	NA	GND	BB14	UNUSED	BB14	UNUSED	NC
BB15	NA	GND	BB15	UNUSED	BB15	UNUSED	NC
BB16	NA	GND	BB16	UNUSED	BB16	UNUSED	NC
BB17	NA	GND	BB17	UNUSED	BB17	UNUSED	NC
BB18	NA	GND	BB18	UNPOPULATED	BB18	GND	
BB19	NA	GND	BB19	GND	BB19	GND	
BB20	NA	GND	BB20	UNUSED	BB20	UNUSED	NC
BB21	NA	GND	BB21	UNUSED	BB21	UNUSED	NC
BB22	NA	GND	BB22	UNUSED	BB22	UNUSED	NC
BB23	NA	GND	BB23	UNUSED	BB23	UNUSED	NC
BB24	NA	GND	BB24	UNUSED	BB24	UNUSED	NC
BB25	NA	GND	BB25	GND	BB25	GND	
BB26	NA	GND	BB26	UNUSED	BB26	UNUSED	NC
BB27	NA	GND	BB27	UNUSED	BB27	UNUSED	NC
BB28	NA	GND	BB28	UNUSED	BB28	UNUSED	NC
BB29	NA	GND	BB29	UNUSED	BB29	UNUSED	NC
BB30	NA	GND	BB30	GND	BB30	GND	
BB31	29	IO_L17N_29	BB31	IO_L17N_29	BB31	IO_L17N_29	
BB32	29	IO_L17P_29	BB32	IO_L17P_29	BB32	IO_L17P_29	
BB33	29	IO_L13P_29	BB33	IO_L13P_29	BB33	IO_L13P_29	
BB34	29	IO_L12P_VRN_29	BB34	IO_L12P_VRN_29	BB34	IO_L12P_VRN_29	
BB35	NA	GND	BB35	GND	BB35	GND	
BB36	29	IO_L10P_CC_29	BB36	IO_L10P_CC_29	BB36	IO_L10P_CC_29	
BB37	29	IO_L8P_CC_29	BB37	IO_L8P_CC_29	BB37	IO_L8P_CC_29	
BB38	29	IO_L5P_29	BB38	IO_L5P_29	BB38	IO_L5P_29	
BB39	29	IO_L4N_VREF_29	BB39	IO_L4N_VREF_29	BB39	IO_L4N_VREF_29	
BB40	NA	GND	BB40	GND	BB40	GND	
BB41	29	GND	BB41	IO_L3N_29	BB41	UNPOPULATED	

Chapter 9

Package Marking

The Virtex®-5QV FPGA package is marked as shown in Figure 9-1 and explained in Table 9-1.

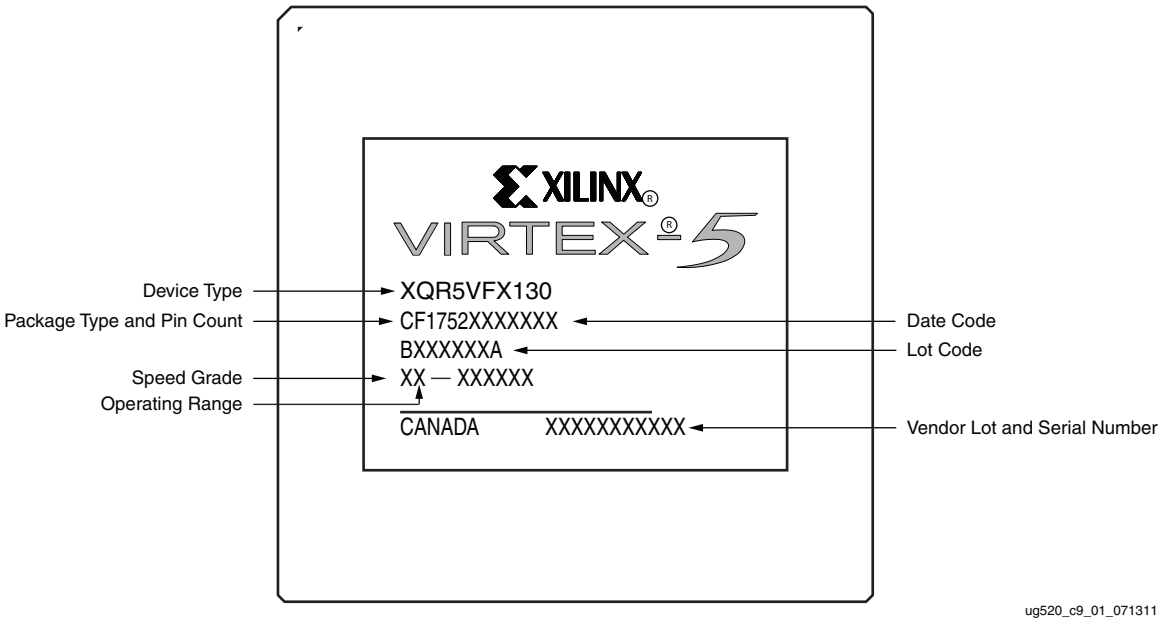


Figure 9-1: **Virtex-5QV FPGA Device Package Marking**

Table 9-1: **Device Marking Definition**

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Family Brand Logo	Virtex-5 family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.
2nd Line	Package type and pin count, circuit design revision, the location code for the wafer fab, the geometry code, and date code.
3rd Line	Eight alphanumeric characters for assembly, lot, and step information. The last digit is usually an *A* or an *M* if a stepping version does not exist.

Table 9-1: **Device Marking Definition *(Continued)***

Item	Definition	
4th Line	Device speed grade and temperature range. If a grade is not marked on the package, the product is considered commercial grade. Other variations for the 4th line:	
	1C-xxxxxx	The *xxxx* indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
5th Line	Eleven alphanumeric characters for vendor lot number and serial number. First eight characters is the vendor lot number. Last three characters is the serial number.	

Chapter 10

Guidelines for Xilinx CF Package Handling and Assembly

Xilinx ceramic flip-chip (CF) packages are robust and reliable. The CF package uses high lead columns (instead of solder balls) to create a higher standoff and more flexible interconnection, which achieves a significant increase in reliability. A silicon carbide (SiC) lid covers the die and ceramic chip capacitors are placed around the periphery of the package.

Like BGA packages, all of the CF interconnections cannot be inspected after board mount, so care must be taken to implement good handling and process controls. With their higher standoff height, columns are more susceptible to handling damage than solder balls. In addition, without proper handling, the ceramic chip capacitors with their small size might be mechanically damaged.

This chapter contains guidelines to properly unpack, handle, inspect, and assemble Xilinx CF packages. The design and process requirements should be compatible with standard surface mount technology (SMT) equipment and with total assembly requirements as driven by other components on the product.

Product Unpacking

Special care must be taken when unpacking CF parts.

1. Handle the box with extreme care. (Read the HANDLE WITH CARE label on the package, shown in Figure 10-1.)

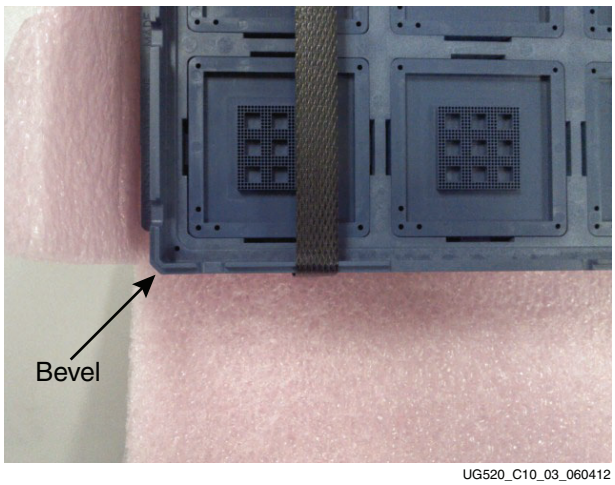
Figure 10-1: ***HANDLE WITH CARE*** **Label**

2. After the dry pack bag is opened and the foam-covered banded tray is removed from the bag, carefully hold positive downward pressure on top of the foam tray while cutting the heat-sealed black plastic bands (see Figure 10-2).

UG520_C10_02_060412

Figure 10-2: **Accessing the Tray**

3. Carefully remove the foam surround blanket.
4. Check for tray orientation. All trays have a corner bevel and must have the correct orientation (see Figure 10-3).



UG520_C10_03_060412

Figure 10-3: **Tray Orientation**

5. Check for tray separation. Trays should be slightly interlocked with no product exposed.
6. Lift the tray from the padding material.

   Note: If the product is not to be used immediately, keep the tray banded until needed.

Proceed with the following steps when ready to assemble hardware:

1. When ready to assemble hardware, carefully cut bands holding trays together.

   Caution! Be careful when cutting the sealed bands. After the sealed bands on the trays are cut, the tray can shift, possibly damaging or bending columns.
2. *Gently* place the unbanded tray on a firm surface.

   Caution! Do not apply a jarring downward force when placing the tray on the surface.
3. After the product tray has been unboxed and the bands cut, fasten the product trays securely at all areas with rubber bands to keep the trays interlocked and the product secured.
4. Foam pads are present between each tray to protect the product. These pads should be removed just before product is to be placed in auto- or manual placement tools.
5. Carefully remove the package inside each tray by removing each in a *vertical upward* motion.

   Caution! Do not use a rolling or angular motion to remove the package. Doing so might bend columns or cause damage.
6. If packing concerns are identified, hold all packing materials with the product and notify the proper area for corrective action.

Product Handling and Inspection

All Xilinx CF package die are flip-chip and bumped with high lead bumping (95% Pb/5% Sn). The CF package substrate is ceramic. The bumped die is flipped and reflowed to the ceramic substrate at assembly. A moisture resistant epoxy underfill encapsulates the bumps. The columns are 90% Pb/10% Sn solid solder columns. The CF package lid is made of silicon carbide and is attached with a thermal epoxy adhesive. See Figure 10-4.

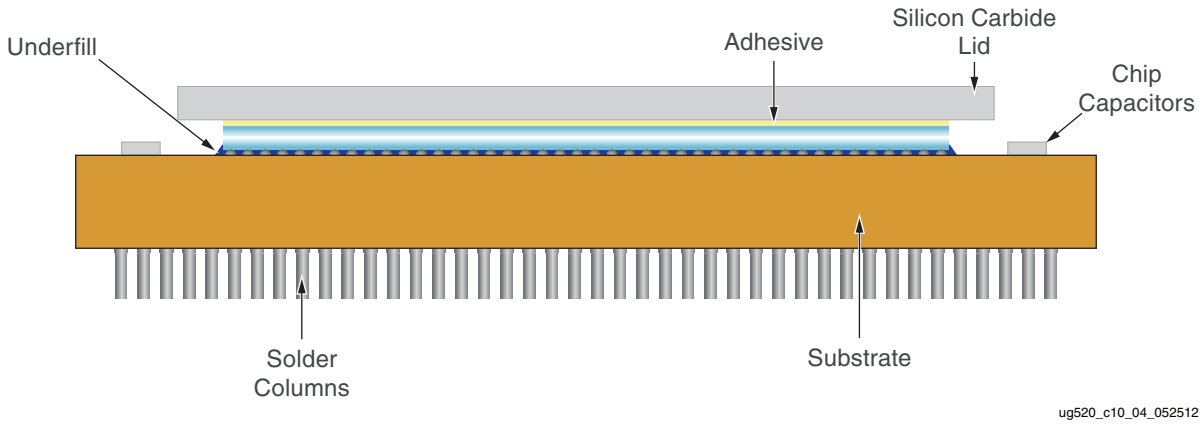


Figure 10-4: **CF Package Construction**

Any inspection of parts should be made while keeping the part in its shipping tray because the columns might be damaged if the part is manually handled or removed from the tray. Careful handling of the parts during board mount is recommended to ensure no damage to the chip capacitors or columns occurs.

Board Level Mounting

Xilinx recommends the customer perform a visual inspection at different steps of the process to ensure that no damage has been induced to the package, columns, board mount, or decoupling chip capacitors due to mishandling issues. Parts should not be removed from the trays until they are mounted to the board.

Note: The design and process requirements should be compatible with standard SMT equipment and with total assembly requirements as driven by other components on the product.

Xilinx recommends PCB design rules for each of our packages. These rules are specified in UG112, *Device Package User Guide*.

For additional CGA board mounting information, refer to the *IBM CBGA Surface Mount Assembly and Rework User Guide* at https://www-01.ibm.com/chips/techlib/techlib.nsf/techdocs/BBA0EE9ED5C3DC8B87256F1800732B94/$file/cbga_assy_rework.pdf

Xilinx recommends that the reflow profile recommended by the solder paste supplier be used. For the cleaning process, Xilinx recommends caustic solvents ***not be used*** during the cleaning cycle. Xilinx recommends DI water rinse and bake are used.

The recommended maximum reflow temperature is 220°C. However, a maximum peak temperature of 235°C can be acceptable. (Refer to page 87 of *IBM CBGA Surface Mount Assembly and Rework User Guide*.)

For solder joint test method (X-rays, X-ray CT, fiberscope, and so on) of inline or failure detection in evaluation test (crack, void, alignment, and so on), IBM® has identified transmission X-ray to detect solder bridging and X-ray laminography to detect solder joint opens. (Refer to page 24 of *IBM CBGA Surface Mount Assembly and Rework User Guide*.)

Most of the heat is dissipated from the columns. Xilinx has measured thermal resistance numbers for these packages.

Rework

Xilinx does not recommend any rework or staking of the CF packages.