Plataforma de hardware recofigurable

Armado - Testeo y Documentación de las placas de prototipaje.

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1. Introducción

La documentación que se presenta en éste reporte describe los pasos a seguir para el *armado, testéo y depuración* de las distintas placas que conformarán la *Plataforma de Hardware Reconfigurable – PHR*. Se presenta un esquema general de tres etapas, sin embargo, cada una de ellas presenta una complejidad diferente.

Figura 1: Esquema de trabajo a seguir.

2. Armado

2.1. Placas

Actualmente se dispone de cuatro placas PCB, ellas son:

- OT-CPLD
- OOCD Links (USB/JTAG)
- S3Power (INTI)
- FPGA (PHR version BETA)

Cada una de éstas placas se encuentra en una versión de *Prototipaje*, lo que implica que su finalidad es únicamente de *testéo* y generar *documentación* que permitan el desarrollo de sus versiones finales, con las correcciones pertinentes.

2.2. Recursos

Se adjunta a la presente documentación la lista de componentes a utilizar.

2.3. Placas

Los esquemáticos se adjuntan al final del documento pero aquí se hace presente a modo de ilustración y que se pueda relacionar con sus correspondientes esquemas PCB.

Se recomienda tener cuidado en el proceso de ensamblado/soldado de los componentes. La mayoría de los mismos son SMD, por lo que puede prestarse a confusiones la polarización de capacitores y diodos, como así también la magnitud de cada uno.

Se presentan las figuras de cada placa, haciendo énfasis en diferentes vistas con la finalidad de facilitar el armado de las mismas.

2.3.1. OT-CPLD

La placa *OT-CPLD* tan solo realiza la adaptación de los pines de un CPLD (XC9572XL) a un formato DIP-40 (40 pines) a fines de ser utilizado en cualquier protoboard. Junto a las dos hileras de pines, la placa contiene un reguladore de tensión para el dispositivo lógico; y un puerto de conexión al interface JTAG del CPLD.

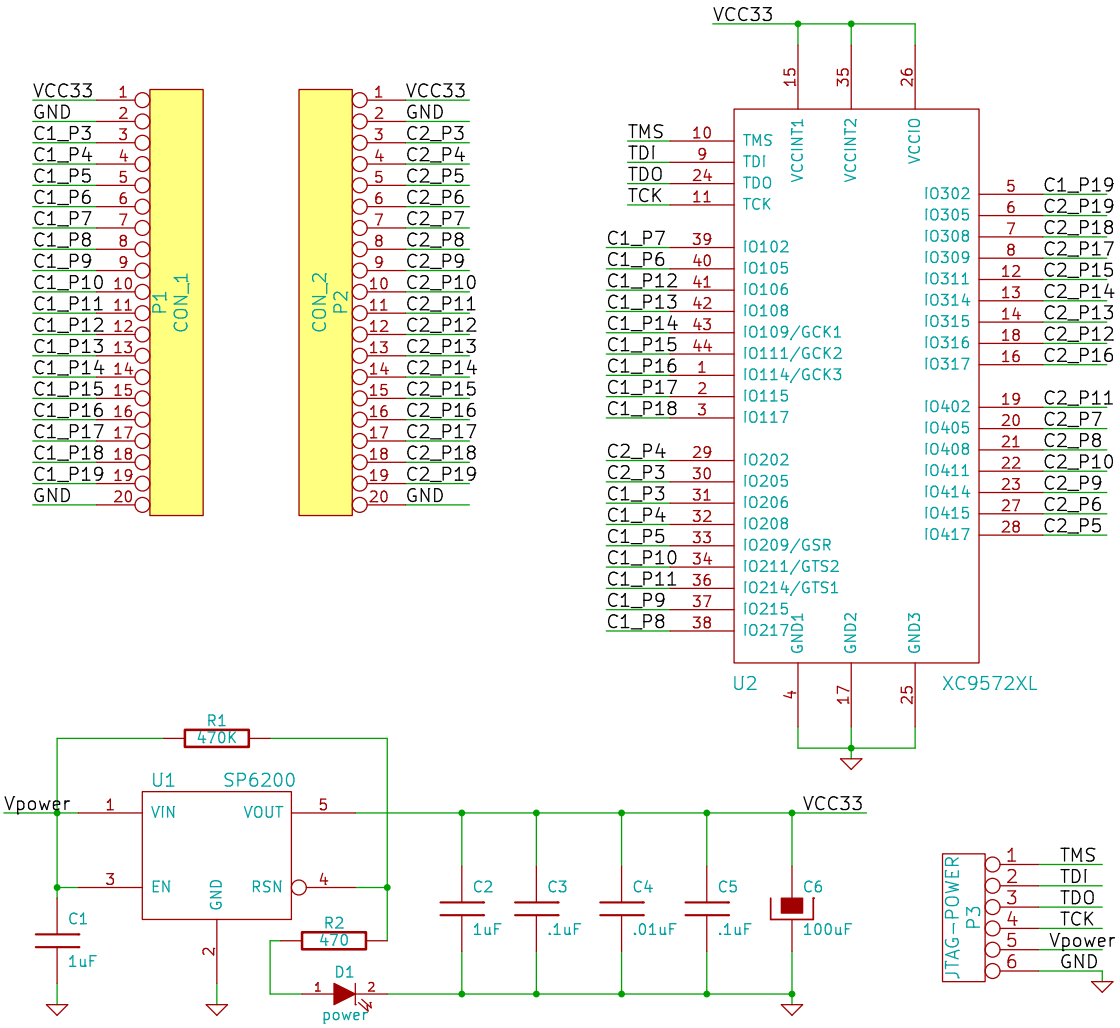
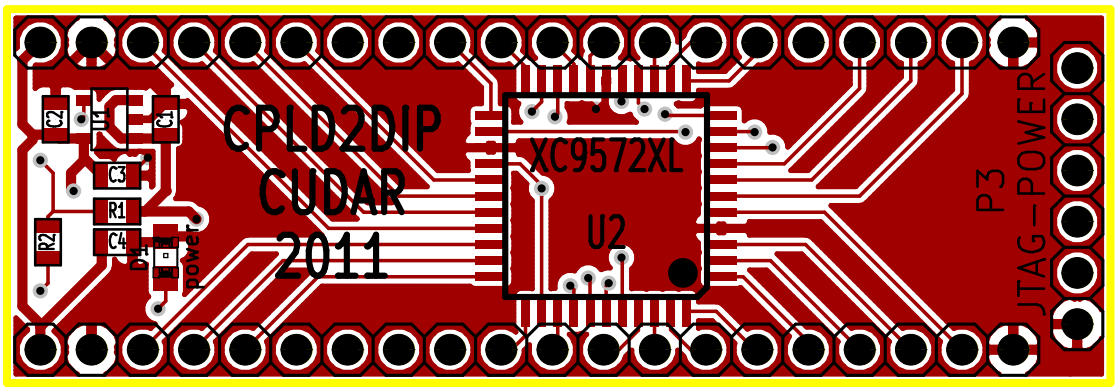
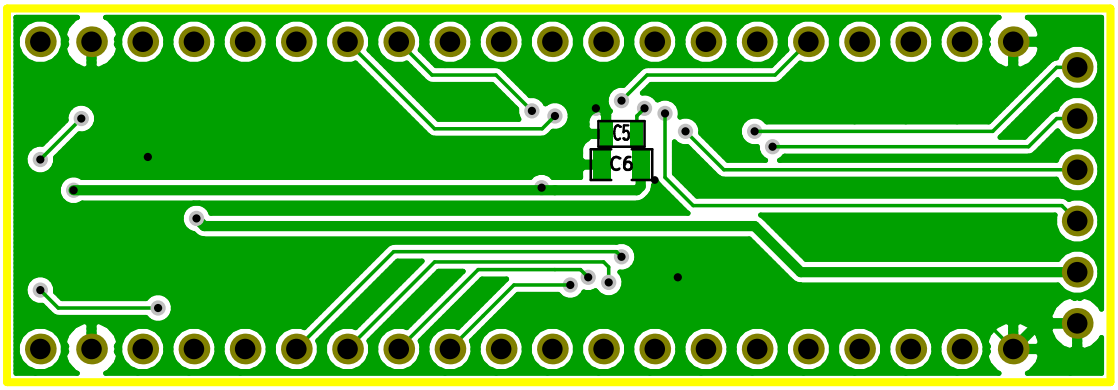


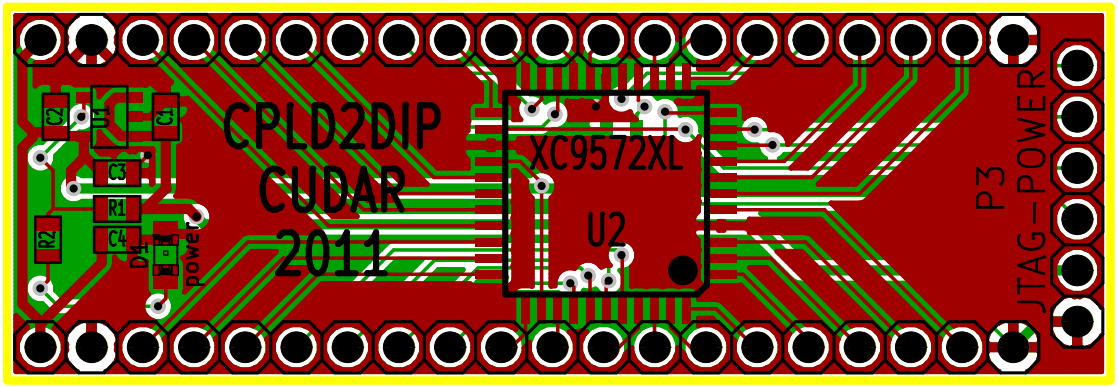
Figura 2: Esquemático



(a) Top



(b) Botton

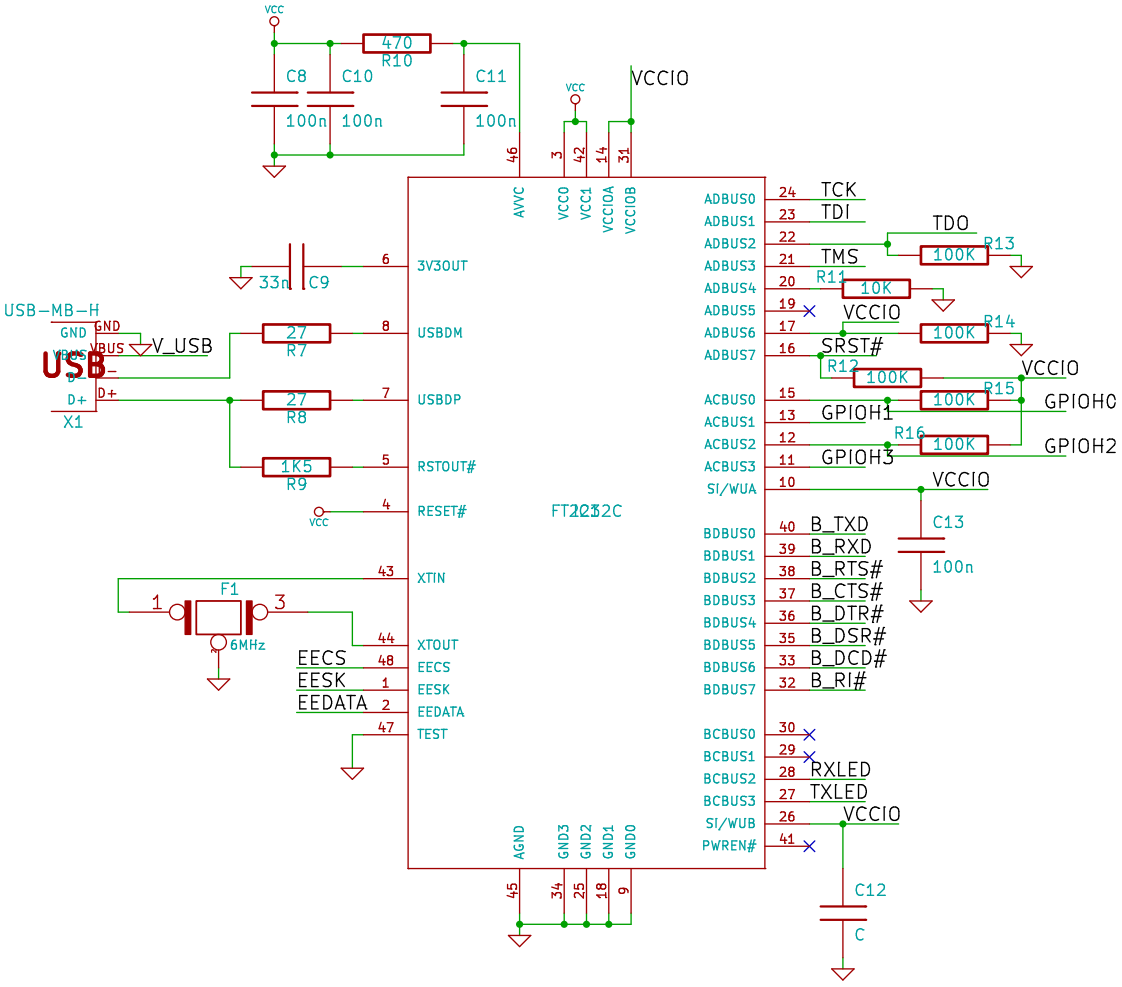


(c) Top & Botton

Figura 3: PCB

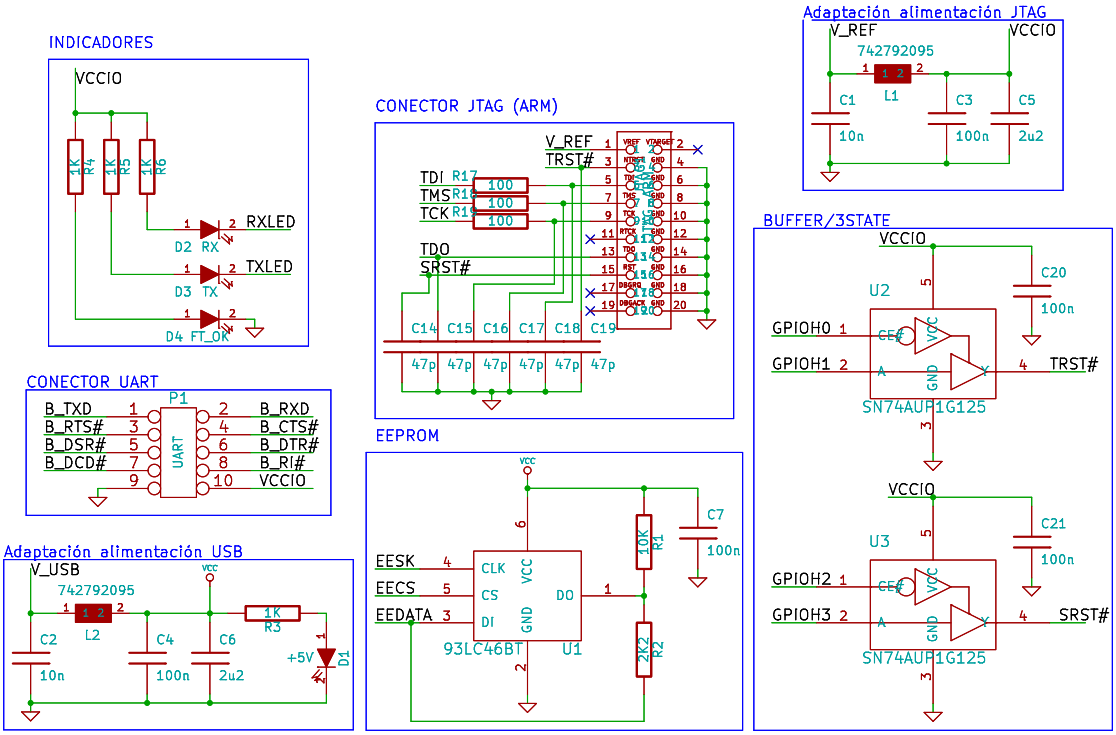
2.3.2. OOCD Links

La placa *OOCD Links* permite acceder a un interface JTAG mediante un puerto USB (hardware & software). Nacido como un interface para el testéo de hardware mediante software, JTAG se ha convertido en un core clave en la programación de muchos dispisitivos actuales como son FPGAs, CPLDs, μCs, μPs, etc. La placa contiene un dispositivo central (FT2232), quién realiza la conversión de los protocolos en forma bidireccional. Los demás bloque simplemente hacen al funcionamiento del FT2232.



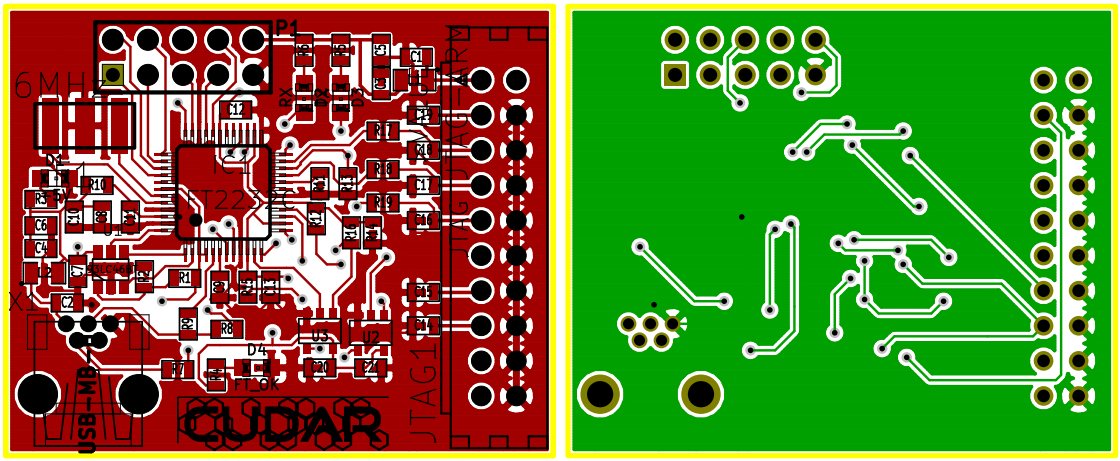
(a) FT2232, IC dispositivo interface USB/JTAG

Figura 4: Esquemático



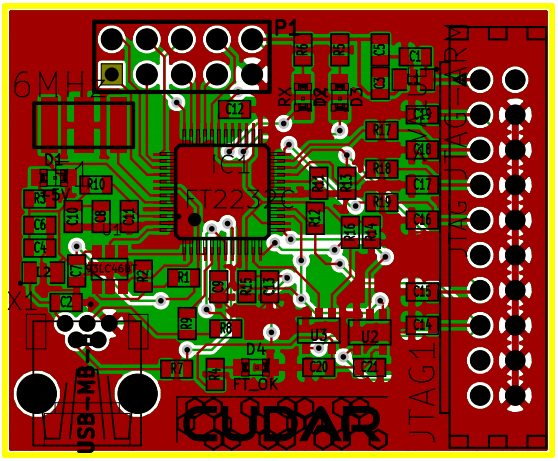
(b) Periféricos

Figura 4: Esquemático (Continuación)



(a) Top (b) Botton

Figura 5: PCB



(c) Top & Botton

Figura 5: PCB (Continuación)

2.3.3. S3Power

La placa *S3Power* fue diseñada por un los miembros del **INTI**, originalmente destinada a la placa **S3Proto**, y liberada con licencia *GPL (General Public License)* en la web `fpgalibre.sourceforce.net`. Las características eléctricas, en particular, de potencia son muy importantes debido a los distintos niveles de tensión que manejan las FPGAs que se utilizarán. Texas Instruments ha desarrollado un IC (TPS75003) específico para la familia de las FPGA de Xilinx (Spantan 3 - Xilinx Inc). Aquí se resuelven los tiempos de encendido como la regulación en el consumo de potencia de la FPGA.

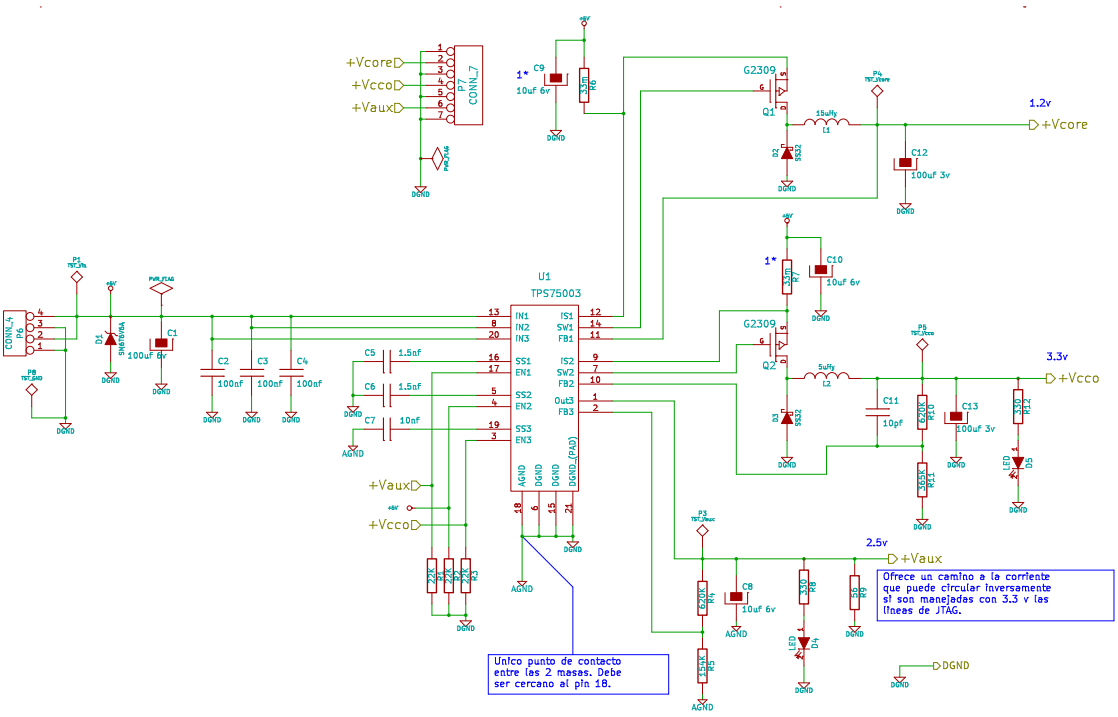
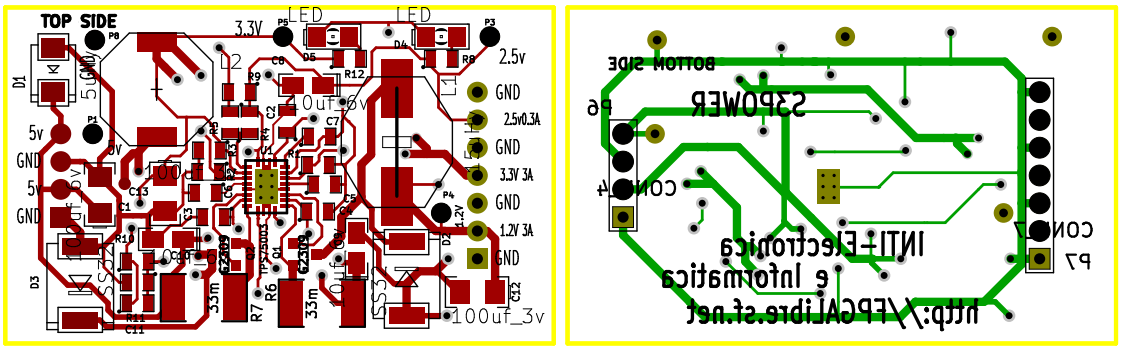


Figura 6: Esquemático



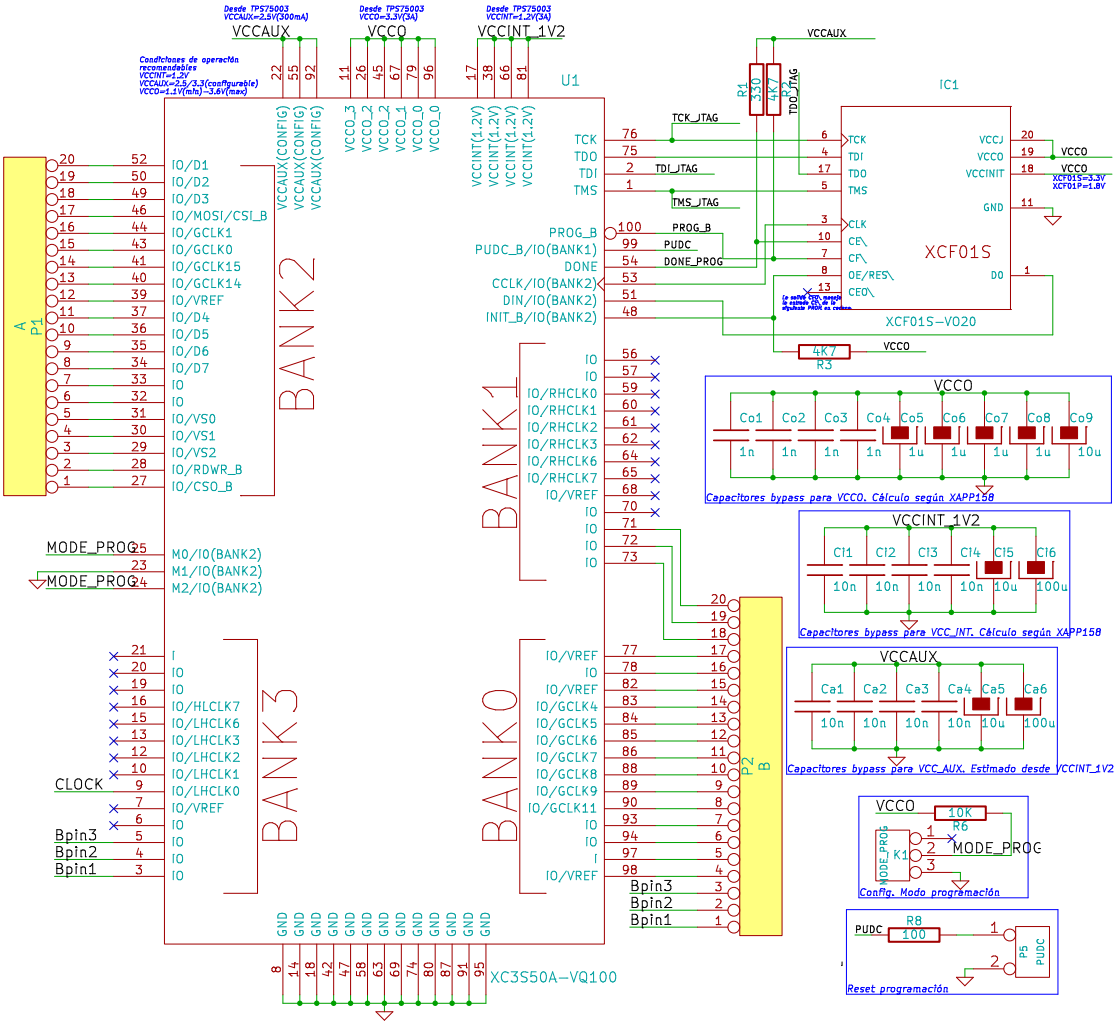
(a) Top (b) Botton

(c) Top & Botton

Figura 7: PCB

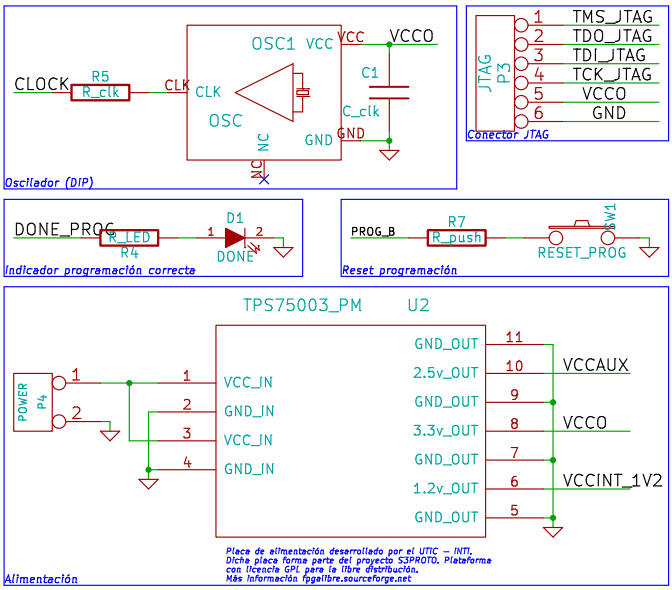
2.3.4. FPGA (PHR version BETA)

La placa *FPGA* que se presenta a continuación, es una versión prototipo que de la placa **PHR** final. La versión BETA pretende realizar un testeo de las características de potencia y el interface al puerto JTAG que dispone el dispositivo programable. Para la alimentación del mismo, se utiliza la placa **S3power** que se ha descrito en puntos anteriores.



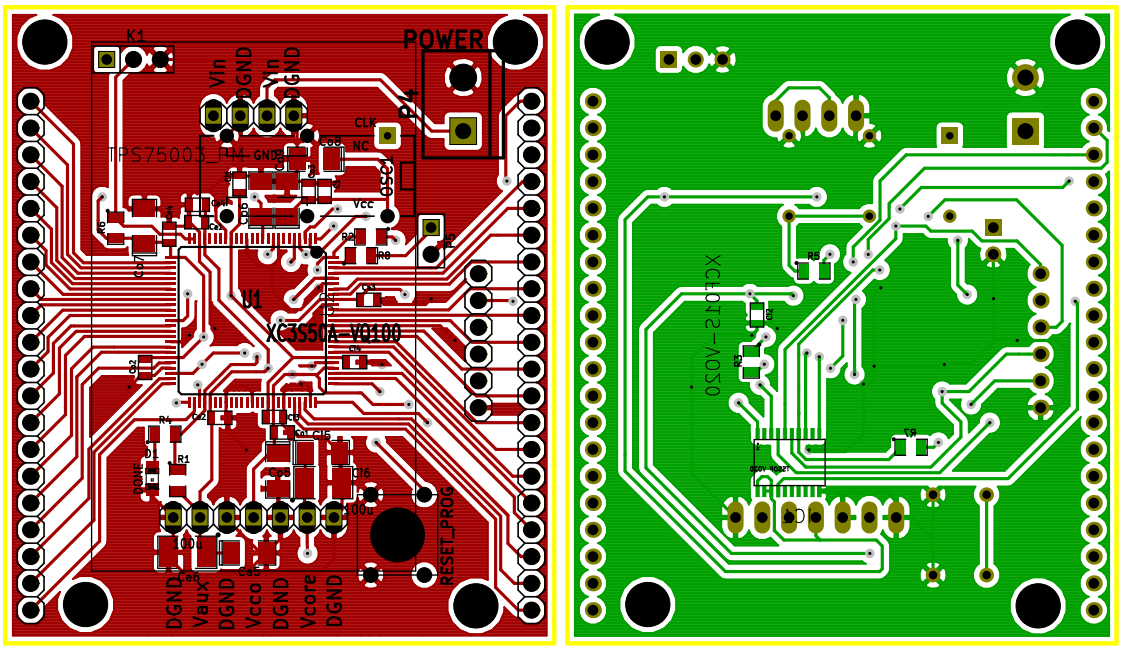
(a) FPGA (XC3S50A) & Memoria de programación (XCF01S)

Figura 8: Esquemático



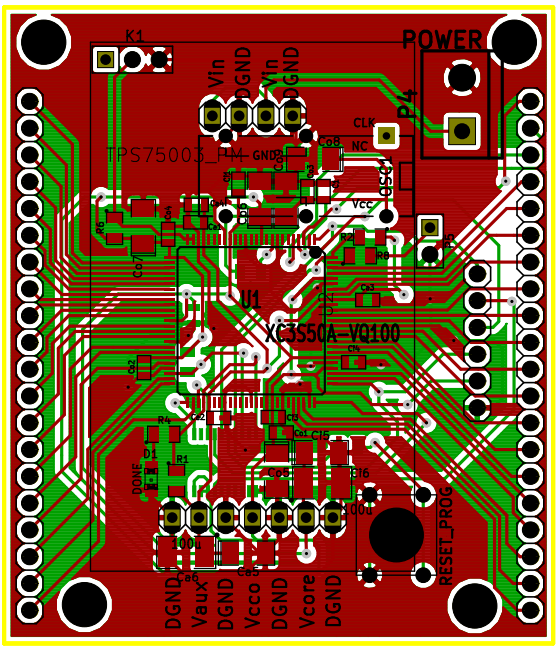
(b) Circuito de potencia (Placa S3power)

Figura 8: Esquemático (Continuación)



(a) Top (b) Botton

Figura 9: PCB



(c) Top & Botton

Figura 9: PCB (Continuación)

3. Documentación

La documentación resulta fundamental en ésta etapa del desarrollo. Si bien se quiere lograr el correcto funcionamiento de las placas, la documentación sirve para realizar correciones a las versiones futuras de cada placa. Otro objetivo es documentar el funcionamiento de cada dispositivo que sirvan al reporte final como así también a los usuarios de la *Plataforma de Hardware Reconfigurable*.

A. Repositorio de proyecto

El proyecto se encuentra alojado en los servidores de *OpenCores*. Por lo que se puede acceder a los repositorios mediante el siguiente link, `http://opencores.org/project,phr` De todas formas se pueden comunicar por correo, `guanucoluis@gmail.com`.

B. Archivos a conciderar

Se dispone de varios archivos relacionados con esta etapa de ensamblado y testeo.

```
luis@luis-laptop:to_print$ ls -lX
total 2872
-rw-r--r-- 1 luis luis    1421 jul 10 16:38 cpld.cmp
-rw-r--r-- 1 luis luis    4599 jul 10 17:09 fpga.cmp
-rw-r--r-- 1 luis luis    6126 ago 28 21:34 OOCD_placa.cmp
-rw-r--r-- 1 luis luis    4159 jul 10 16:40 S3Proto_Power.cmp
-rw-r--r-- 1 luis luis  234181 ago 28 21:29 fpga_brd.pdf
-rw-r--r-- 1 luis luis  137037 ago 28 21:55 fpga_sch.pdf
-rw-r--r-- 1 luis luis  177723 ago 28 21:23 OOCD-Links_brd.pdf
-rw-r--r-- 1 luis luis   88397 ago 28 21:55 OOCD-Links_sch.pdf
-rw-r--r-- 1 luis luis  145699 ago 28 21:04 ot-cpld_brd.pdf
-rw-r--r-- 1 luis luis   55105 ago 28 21:55 ot-cpld_sch.pdf
-rw-r--r-- 1 luis luis  121516 ago 28 21:17 S3Proto_Power_brd.pdf
-rw-r--r-- 1 luis luis   63912 ago 28 00:40 S3Proto_Power_sch.pdf
-rw-r--r-- 1 luis luis 1520722 ago 28 20:39 schedule.pdf
-rw-r--r-- 1 luis luis   57478 ago 28 21:35 cpld.png
-rw-r--r-- 1 luis luis   86035 ago 28 21:37 fpga.png
-rw-r--r-- 1 luis luis   66724 ago 28 21:33 OOCD_placa.png
-rw-r--r-- 1 luis luis   70647 ago 28 21:36 S3Proto_Power.png
```

En estos archivos se tiene las figuras presentadas en las anteriores secciones pero con mejor resolución, estos terminan en `_sch` o `_brd` correspondientes a si se trata del esquemático o el PCB, respectivamente. También se tiene los archivos `.cmp`, los que contienen la lista de componentes a utilizar y su referencia en el esquemático como así también el encapsulado. Los archivos `.png` son las distintas placas vista en 3D para tener una idea de como debería quedar al finalizar el desarrollo.

C. Lista de componentes

C.1. OT-CPLD

```
BeginCmp
TimeStamp = /4EA65376;
Reference = C1;
ValeurCmp = 1uF;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = /4EA6543A;
Reference = C2;
ValeurCmp = 1uF;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = /4EA882B4;
Reference = C3;
ValeurCmp = .1uF;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = /4EA882BB;
Reference = C4;
ValeurCmp = .01uF;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = /4EA882C2;
Reference = C5;
ValeurCmp = .1uF;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = /4EA882CF;
Reference = C6;
ValeurCmp = 100uF;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = /4EA654D2;
Reference = D1;
ValeurCmp = power;
IdModule  = LED-0805;
EndCmp

BeginCmp
TimeStamp = /4EA74DB8;
Reference = P1;
ValeurCmp = CON_1;
IdModule  = 1X20;
EndCmp

BeginCmp
TimeStamp = /4EA74DAC;
Reference = P2;
ValeurCmp = CON_2;
IdModule  = 1X20;
EndCmp

BeginCmp
TimeStamp = /4EA1F196;
Reference = P3;
ValeurCmp = JTAG-POWER;
IdModule  = 1X06;
EndCmp

BeginCmp
TimeStamp = /4EA653DA;
Reference = R1;
ValeurCmp = 470K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = /4EA654AE;
Reference = R2;
ValeurCmp = 470;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = /4EA652AE;
Reference = U1;
ValeurCmp = SP6200;
```

```
IdModule  = SOT23-5;
EndCmp

BeginCmp
TimeStamp = /4EA62E7A;
Reference = U2;
ValeurCmp = XC9572XL;
IdModule  = TQFP44;
EndCmp

EndListe
```

C.2. OOCD Links

```
 BeginCmp
TimeStamp = 4EB85B2D
Path = /4EAE3B06
Reference = X1;
ValeurCmp = USB-MB-H;
IdModule  = con-usb-USB-MB-H;
EndCmp

BeginCmp
TimeStamp = 4EAEBF60
Path = /4EAB3FF2
Reference = IC1;
ValeurCmp = FT2232C;
IdModule  = ft2232c-LQFP;
EndCmp

BeginCmp
TimeStamp = 4EAEBF62
Path = /4EAE3363
Reference = D4;
ValeurCmp = FT_OK;
IdModule  = LED-0805;
EndCmp

BeginCmp
TimeStamp = 4EB0CE47
Path = /4EAE3357
Reference = D3;
ValeurCmp = TX;
IdModule  = LED-0805;
EndCmp

BeginCmp
TimeStamp = 4EAEBF66
Path = /4EAE3349
Reference = D2;
ValeurCmp = RX;
IdModule  = LED-0805;
EndCmp

BeginCmp
TimeStamp = 4EAEBF68
Path = /4EAE32A1
Reference = D1;
ValeurCmp = +5V;
IdModule  = LED-0805;
EndCmp

BeginCmp
TimeStamp = 4EAEBF69
Path = /4EAE3DC9
Reference = JTAG1;
ValeurCmp = JTAG-ARM;
IdModule  = nxp-JTAG-ARM;
EndCmp

BeginCmp
TimeStamp = 4EAEBF6A
Path = /4EAE5354
Reference = P1;
ValeurCmp = UART;
IdModule  = PIN_ARRAY_5x2;
EndCmp

BeginCmp
TimeStamp = 4EAEBF6B
Path = /4EAE495A
Reference = R19;
ValeurCmp = 100;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF6D
Path = /4EAE4953
Reference = R18;
ValeurCmp = 100;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF6F
Path = /4EAE4946
Reference = R17;
ValeurCmp = 100;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF71
```

```
Path = /4EAE4FF4
Reference = R16;
ValeurCmp = 100K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF73
Path = /4EAE4ED6
Reference = R15;
ValeurCmp = 100K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF75
Path = /4EAE4DA5
Reference = R14;
ValeurCmp = 100K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF77
Path = /4EAE4D2D
Reference = R13;
ValeurCmp = 100K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF79
Path = /4EAE4E0E
Reference = R12;
ValeurCmp = 100K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF7B
Path = /4EAE3F20
Reference = R11;
ValeurCmp = 10K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF7D
Path = /4EAE3201
Reference = R10;
ValeurCmp = 470;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF7F
Path = /4EAE3B8F
Reference = R9;
ValeurCmp = 1K5;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF81
Path = /4EAE3B4B
Reference = R8;
ValeurCmp = 27;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF83
Path = /4EAE3B44
Reference = R7;
ValeurCmp = 27;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF85
Path = /4EAE346C
Reference = R6;
ValeurCmp = 1K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EB0CE4A
Path = /4EAE3468
Reference = R5;
ValeurCmp = 1K;
IdModule  = SM0603;
EndCmp
```

```
BeginCmp
TimeStamp = 4EAEBF89
Path = /4EAE3464
Reference = R4;
ValeurCmp = 1K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF8B
Path = /4EAE3297
Reference = R3;
ValeurCmp = 1K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF8D
Path = /4EAE2459
Reference = R2;
ValeurCmp = 2K2;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF8F
Path = /4EAE2494
Reference = R1;
ValeurCmp = 10K;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF91
Path = /4EAE516F
Reference = C21;
ValeurCmp = 100n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF93
Path = /4EAE5167
Reference = C20;
ValeurCmp = 100n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF95
Path = /4EAE4AF1
Reference = C19;
ValeurCmp = 47p;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF97
Path = /4EAE4B24
Reference = C18;
ValeurCmp = 47p;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF99
Path = /4EAE4B2F
Reference = C17;
ValeurCmp = 47p;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF9B
Path = /4EAE4B56
Reference = C16;
ValeurCmp = 47p;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF9D
Path = /4EAE4B6A
Reference = C15;
ValeurCmp = 47p;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBF9F
Path = /4EAE4B76
Reference = C14;
ValeurCmp = 47p;
IdModule  = SM0603;
```

```
EndCmp

BeginCmp
TimeStamp = 4EAEBFA1
Path = /4EAE3EE0
Reference = C13;
ValeurCmp = 100n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFA3
Path = /4EAE384B
Reference = C12;
ValeurCmp = C;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFA5
Path = /4EAE31EE
Reference = C11;
ValeurCmp = 100n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFA7
Path = /4EAE31F7
Reference = C10;
ValeurCmp = 100n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFA9
Path = /4EAE3A16
Reference = C9;
ValeurCmp = 33n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFAB
Path = /4EAE31FD
Reference = C8;
ValeurCmp = 100n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFAD
Path = /4EAE24AC
Reference = C7;
ValeurCmp = 100n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFAF
Path = /4EAE30A8
Reference = C6;
ValeurCmp = 2u2;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFB1
Path = /4EAE3C52
Reference = C5;
ValeurCmp = 2u2;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFB3
Path = /4EAE308F
Reference = C4;
ValeurCmp = 100n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFB5
Path = /4EAE3C53
Reference = C3;
ValeurCmp = 100n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFB7
Path = /4EAE2C55
Reference = C2;
```

```
ValeurCmp = 10n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFB9
Path = /4EAE3C56
Reference = C1;
ValeurCmp = 10n;
IdModule  = SM0603;
EndCmp

BeginCmp
TimeStamp = 4EAEBFBA
Path = /4EAE3061
Reference = L2;
ValeurCmp = 742792095;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 4EAEBFBC
Path = /4EAE3C54
Reference = L1;
ValeurCmp = 742792095;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 4EAEBFBD
Path = /4EAE4851
Reference = U3;
ValeurCmp = SN74AUP1G125;
IdModule  = SOT23-5;
EndCmp

BeginCmp
TimeStamp = 4EAEBFBF
Path = /4EAE4848
Reference = U2;
ValeurCmp = SN74AUP1G125;
IdModule  = SOT23-5;
EndCmp

BeginCmp
TimeStamp = 4EAEBFC0
Path = /4EAE22F9
Reference = U1;
ValeurCmp = 93LC46BT;
IdModule  = SOT23_6;
EndCmp

BeginCmp
TimeStamp = 4EAEBF61
Path = /4EAE26A6
Reference = F1;
ValeurCmp = 6MHz;
IdModule  = -CSTCC;
EndCmp

BeginCmp
TimeStamp = 4EB863DD
Path =
Reference = ref;
ValeurCmp = logo_min;
IdModule  = ;
EndCmp

EndListe
```

C.3. S3Power

```
BeginCmp
TimeStamp = 48FC941B;
Reference = C1;
ValeurCmp = 100uf_6v;
IdModule  = -B/3528-21W;
EndCmp

BeginCmp
TimeStamp = 48FC9514;
Reference = C2;
ValeurCmp = 100nf;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FC9531;
Reference = C3;
ValeurCmp = 100nf;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FC9532;
Reference = C4;
ValeurCmp = 100nf;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FC94F6;
Reference = C5;
ValeurCmp = 1.5nf;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FCB2A9;
Reference = C6;
ValeurCmp = 1.5nf;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FC94AF;
Reference = C7;
ValeurCmp = 10nf;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FC948C;
Reference = C8;
ValeurCmp = 10uf_6v;
IdModule  = -A/3216-18R;
EndCmp

BeginCmp
TimeStamp = 48FC948A;
Reference = C9;
ValeurCmp = 10uf_6v;
IdModule  = -A/3216-18R;
EndCmp

BeginCmp
TimeStamp = 48FDDDFF;
Reference = C10;
ValeurCmp = 10uf_6v;
IdModule  = -A/3216-18R;
EndCmp

BeginCmp
TimeStamp = 48FC9564;
Reference = C11;
ValeurCmp = 10pf;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FC9463;
Reference = C12;
ValeurCmp = 100uf_3v;
IdModule  = -B/3528-21W;
EndCmp

BeginCmp
TimeStamp = 48FDDDFE;
Reference = C13;
ValeurCmp = 100uf_3v;
IdModule  = -B/3528-21W;
EndCmp
```

```
BeginCmp
TimeStamp = 48FC939B;
Reference = D1;
ValeurCmp = SM6T6V6A;
IdModule  = DO_214AA;
EndCmp

BeginCmp
TimeStamp = 48FC97B2;
Reference = D2;
ValeurCmp = SS32;
IdModule  = DO214AB;
EndCmp

BeginCmp
TimeStamp = 48FDDE02;
Reference = D3;
ValeurCmp = SS32;
IdModule  = DO214AB;
EndCmp

BeginCmp
TimeStamp = 4900D275;
Reference = D4;
ValeurCmp = LED;
IdModule  = -1206;
EndCmp

BeginCmp
TimeStamp = 4900C810;
Reference = D5;
ValeurCmp = LED;
IdModule  = -1206;
EndCmp

BeginCmp
TimeStamp = 48FC9598;
Reference = L1;
ValeurCmp = 15uHy;
IdModule  = wuerth_elektronik_WE-PD4;
EndCmp

BeginCmp
TimeStamp = 48FDDE00;
Reference = L2;
ValeurCmp = 5uHy;
IdModule  = wuerth_elektronik_v5-WE-TPC_XL/XLH;
EndCmp

BeginCmp
TimeStamp = 4907220B;
Reference = P1;
ValeurCmp = TST_Vin;
IdModule  = PINTST;
EndCmp

BeginCmp
TimeStamp = 48FDE089;
Reference = P3;
ValeurCmp = TST_Vaux;
IdModule  = PINTST;
EndCmp

BeginCmp
TimeStamp = 48FDDD65;
Reference = P4;
ValeurCmp = TST_Vcore;
IdModule  = PINTST;
EndCmp

BeginCmp
TimeStamp = 48FDDE09;
Reference = P5;
ValeurCmp = TST_Vcco;
IdModule  = PINTST;
EndCmp

BeginCmp
TimeStamp = 491C3ECB;
Reference = P6;
ValeurCmp = CONN_4;
IdModule  = header_1x4;
EndCmp

BeginCmp
TimeStamp = 49256388;
Reference = P7;
ValeurCmp = CONN_7;
IdModule  = header_1x7;
EndCmp

BeginCmp
TimeStamp = 499DB3E3;
```

```
Reference = P8;
ValeurCmp = TST_GND;
IdModule  = PINTST;
EndCmp

BeginCmp
TimeStamp = 48FC9789;
Reference = Q1;
ValeurCmp = G2309;
IdModule  = SOT23GDS;
EndCmp

BeginCmp
TimeStamp = 48FDDE01;
Reference = Q2;
ValeurCmp = G2309;
IdModule  = SOT23GDS;
EndCmp

BeginCmp
TimeStamp = 48FDE587;
Reference = R1;
ValeurCmp = 22K;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FDE584;
Reference = R2;
ValeurCmp = 22K;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FDE56A;
Reference = R3;
ValeurCmp = 22K;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FDE06A;
Reference = R4;
ValeurCmp = 620K;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FDE06B;
Reference = R5;
ValeurCmp = 154K;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FDD021;
Reference = R6;
ValeurCmp = 33m;
IdModule  = SM2512;
EndCmp

BeginCmp
TimeStamp = 48FDDE03;
Reference = R7;
ValeurCmp = 33m;
IdModule  = SM2512;
EndCmp

BeginCmp
TimeStamp = 4900D274;
Reference = R8;
ValeurCmp = 330;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FDE2B6;
Reference = R9;
ValeurCmp = 56;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FDDF37;
Reference = R10;
ValeurCmp = 620K;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FDDF3E;
Reference = R11;
ValeurCmp = 365K;
IdModule  = SM0805;
```

```
EndCmp

BeginCmp
TimeStamp = 4900C7F6;
Reference = R12;
ValeurCmp = 330;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = 48FC9227;
Reference = U1;
ValeurCmp = TPS75003;
IdModule  = TPS75003;
EndCmp

EndListe
```

C.4. FPGA

```
BeginCmp
TimeStamp = /4F4D3964;
Reference = C1;
ValeurCmp = C_clk;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F58A802;
Reference = Ca1;
ValeurCmp = 10n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F69141B;
Reference = Ca2;
ValeurCmp = 10n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F69141F;
Reference = Ca3;
ValeurCmp = 10n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F691428;
Reference = Ca4;
ValeurCmp = 10n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F58BF85;
Reference = Ca5;
ValeurCmp = 10u;
IdModule  = SM1206POL;
EndCmp

BeginCmp
TimeStamp = /4F69144A;
Reference = Ca6;
ValeurCmp = 100u;
IdModule  = SM1210L;
EndCmp

BeginCmp
TimeStamp = /4F6913AD;
Reference = Ci1;
ValeurCmp = 10n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F6913AC;
Reference = Ci2;
ValeurCmp = 10n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F6913AA;
Reference = Ci3;
ValeurCmp = 10n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F6913AB;
Reference = Ci4;
ValeurCmp = 10n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F6913A7;
Reference = Ci5;
ValeurCmp = 10u;
IdModule  = SM1206POL;
EndCmp

BeginCmp
TimeStamp = /4F6913A9;
Reference = Ci6;
ValeurCmp = 100u;
IdModule  = SM1210L;
EndCmp
```

```
BeginCmp
TimeStamp = /4F58BBF5;
Reference = Co1;
ValeurCmp = 1n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F58BC49;
Reference = Co2;
ValeurCmp = 1n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F58BC4C;
Reference = Co3;
ValeurCmp = 1n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F58BC4F;
Reference = Co4;
ValeurCmp = 1n;
IdModule  = SM0603_Capa;
EndCmp

BeginCmp
TimeStamp = /4F58BEE2;
Reference = Co5;
ValeurCmp = 1u;
IdModule  = SM1206POL;
EndCmp

BeginCmp
TimeStamp = /4F58BF10;
Reference = Co6;
ValeurCmp = 1u;
IdModule  = SM1206POL;
EndCmp

BeginCmp
TimeStamp = /4F58BF12;
Reference = Co7;
ValeurCmp = 1u;
IdModule  = SM1206POL;
EndCmp

BeginCmp
TimeStamp = /4F58BF17;
Reference = Co8;
ValeurCmp = 1u;
IdModule  = SM1206POL;
EndCmp

BeginCmp
TimeStamp = /4F58BF30;
Reference = Co9;
ValeurCmp = 10u;
IdModule  = SM1206POL;
EndCmp

BeginCmp
TimeStamp = /4E4D4DD3;
Reference = D1;
ValeurCmp = DONE;
IdModule  = LED-0805;
EndCmp

BeginCmp
TimeStamp = /4F4D2E32;
Reference = H1;
ValeurCmp = PCB_HOLE;
IdModule  = HOLE;
EndCmp

BeginCmp
TimeStamp = /4F4D2E38;
Reference = H2;
ValeurCmp = PCB_HOLE;
IdModule  = HOLE;
EndCmp

BeginCmp
TimeStamp = /4F4D2E36;
Reference = H3;
ValeurCmp = PCB_HOLE;
IdModule  = HOLE;
EndCmp

BeginCmp
TimeStamp = /4F4D2E3A;
```

```
Reference = H4;
ValeurCmp = PCB_HOLE;
IdModule  = HOLE;
EndCmp

BeginCmp
TimeStamp = /4E178DD4;
Reference = IC1;
ValeurCmp = XCF01S-VO20;
IdModule  = xilinx_virtexii-xc2v80&flashprom-VO20;
EndCmp

BeginCmp
TimeStamp = /4E178908;
Reference = K1;
ValeurCmp = MODE_PROG;
IdModule  = PIN_ARRAY_3X1;
EndCmp

BeginCmp
TimeStamp = /4F4D2E41;
Reference = OSC1;
ValeurCmp = OSC;
IdModule  = DIP4-8_OSC;
EndCmp

BeginCmp
TimeStamp = /4F4807B3;
Reference = P1;
ValeurCmp = A;
IdModule  = 1X20_MOD;
EndCmp

BeginCmp
TimeStamp = /4F480E3E;
Reference = P2;
ValeurCmp = B;
IdModule  = 1X20_MOD;
EndCmp

BeginCmp
TimeStamp = /4F4D2C3A;
Reference = P3;
ValeurCmp = JTAG;
IdModule  = PIN_ARRAY-6X1;
EndCmp

BeginCmp
TimeStamp = /4F47FC62;
Reference = P4;
ValeurCmp = POWER;
IdModule  = bornier2;
EndCmp

BeginCmp
TimeStamp = /4F4810C2;
Reference = P5;
ValeurCmp = PUDC;
IdModule  = PIN_ARRAY_2X1;
EndCmp

BeginCmp
TimeStamp = /4F46B535;
Reference = R1;
ValeurCmp = 330;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = /4F46B5A2;
Reference = R2;
ValeurCmp = 4K7;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = /4F46B626;
Reference = R3;
ValeurCmp = 4K7;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = /4E4D4DC9;
Reference = R4;
ValeurCmp = R_LED;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = /4F4D3968;
Reference = R5;
ValeurCmp = R_clk;
IdModule  = SM0805;
```

```
EndCmp

BeginCmp
TimeStamp = /4E4D5328;
Reference = R6;
ValeurCmp = 10K;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = /4F4801C9;
Reference = R7;
ValeurCmp = R_push;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = /4F481067;
Reference = R8;
ValeurCmp = 100;
IdModule  = SM0805;
EndCmp

BeginCmp
TimeStamp = /4F4801A4;
Reference = SW1;
ValeurCmp = RESET_PROG;
IdModule  = SW_PUSH_SMALL;
EndCmp

BeginCmp
TimeStamp = /4F4675A1;
Reference = U1;
ValeurCmp = XC3S50A-VQ100;
IdModule  = VQFP100;
EndCmp

BeginCmp
TimeStamp = /4F47E8FD;
Reference = U2;
ValeurCmp = TPS75003_PM;
IdModule  = TPS75003_PM_INV;
EndCmp

EndListe
```