IEEE 1149.1 JTAG Test Access Port
Reset Requirement Application Note

Introduction

A number of Pericom's bridge and packet switch devices support built-in IEEE 1149.1 JTAG Test Access Port (TAP) controller for debugging and testing purposes. The IEEE Standard Test Access Port and Boundary-Scan Architecture specification requires that the JTAG controller must be reset at system power-on to ensure correct device operation. This application note provides information and implementation instructions for resetting the JTAG controller.

IEEE Requirements of JTAG TAP Reset

Pericom's devices that feature JTAG controller do not have internal circuitry to detect power-on condition and reset the TAP controller. As a result, dedicated TRST# signal must be asserted during power-on to reset the TAP controller.

The IEEE specification also requires that the TAP controller must not be reset by any other chip I/Os such as the system reset signal. Therefore, TRST# can not be asserted directly or logically by PERST# (system reset).

JTAG TAP Controller Reset Implementations

Two implementations can be used to reset the JTAG controller. The first implementation (see Figure 1) pulls TRST# low and keeps the TAP controller in reset if a JTAG debugger is not connected to the Pericom device. While the TAP controller is in rest, all the other chip I/Os are in normal mode. However, designer must be cautious not to attach the JTAG debugger to the circuitry during power-on, since the debugger may hold TRST# de-asserted and, as a result, fail to reset the TAP controller.

The second implementation is designed (see Figure 2) such that the TAP controller is reset either by a power-on rest or by the assertion of TRST# from a JTAG debugger. In this implementation, TRST# is not affected by PERST# (system reset), and is compliant to the IEEE specification requirements.

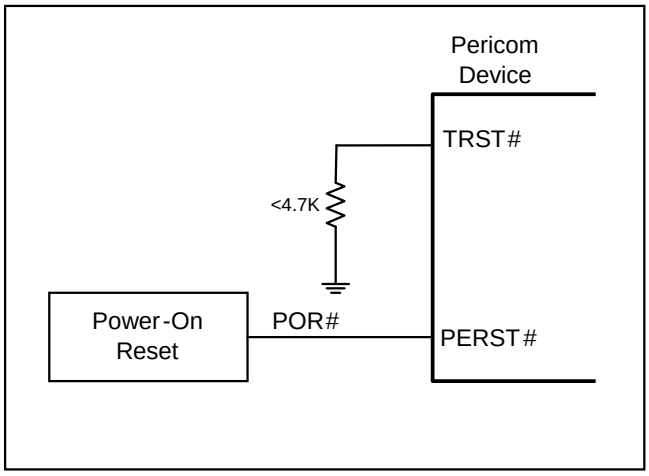

Figure 1 First TRST# Implementation

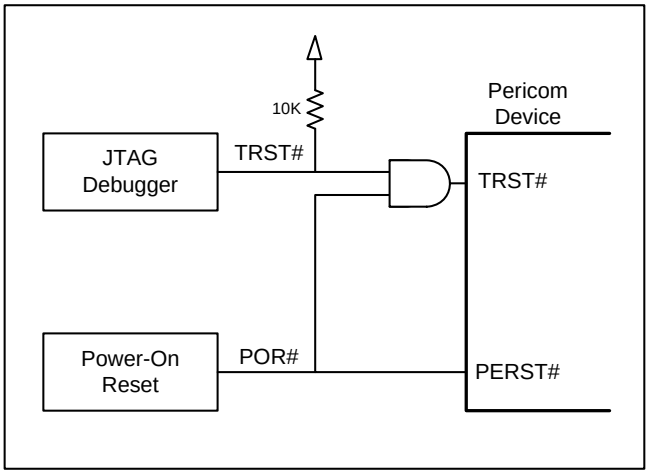

Figure 2 Second TRST# Implementation