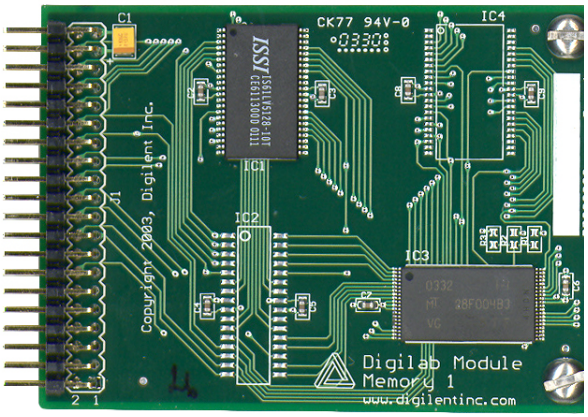
Digilent Memory Module 1 Reference Manual

Revision: 04/12/05

www.digilentinc.com
215 E Main Suite D | Pullman, WA 99163
(509) 334 6306 Voice and Fax

Overview

The Digilent Memory Module 1 circuit board (the MEM1) is a byte wide memory board containing static RAM memory and flash ROM memory. It can be attached to a Digilent system board to provide memory for use in logic designs implemented on the system board:



The MEM1 circuit board is available in various memory configurations:

- C1: 512Kb SRAM, 512Kb Flash
- C2: 1Mb SRAM, no Flash
- C3: no SRAM, 1Mb Flash

Functional Description

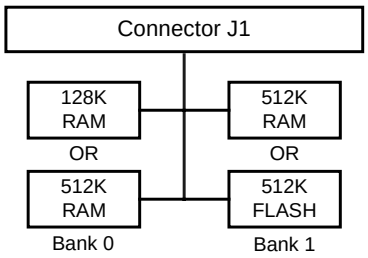
The following is a brief description of the operation of the memory devices on the MEM1 board. For complete documentation on the operation of the various memory devices, refer to the respective manufacturers data sheets.

The MEM1 board contains two memory banks, Bank 0 and Bank 1. Bank 0 can be loaded with either an ISSI IS63LV1024L-J 128K x 8 SRAM or an ISSI IS61LV5128T 512K x 8 SRAM. Chip select line CS0 enables the memory device installed on Bank 0 for access.

Memory Bank 1 can be loaded with either an ISSI IS61LV5128T 512K x 8 SRAM, a Micron MT28F004B3 512K x 8 Flash ROM, or a Micron MT28F008B3 1M x 8 Flash ROM. Chip select line CS1 enables the memory device installed on Bank 1 for access.

Configuration C1 has the IS61LV5128T installed in Bank 0 and the MT28F004B3 installed in Bank 1.

Configuration C2 has the IS61LV5128T installed in both Bank 0 and Bank 1.



MEM1 Circuit Diagram

Configuration C3 has the MT28F008B3 installed in Bank1. Chip select line CS0 is used for the highest-order address bit.

The MEM1 has 19 address inputs (A0-A18), 8 bi-directional data input/outputs (D0-D7), two chip/bank select inputs (CS0 and CS1), a single read strobe input (OE) and a single write strobe input (WE). Note: for the 128K IS64LV1024L-J device, only address lines A0-A16 are used.

A memory read cycle is performed by placing the address on the address lines, bringing the appropriate chip select line low to enable the memory device, bringing the OE line low and then reading the data placed on the bi-directional data lines by the selected memory device.

A memory write cycle is preformed by placing the address and data on the address and data lines, bringing the appropriate chip select line low and then writing the data by bringing the WE line low and then high.

Please refer to the manufacturers' data sheets for the memory devices for exact wave forms and timing requirements for read and write cycles.

Flash Memory Operation

Read operations on the flash memory are performed similarly to read operations on the SRAM. The timing of write operations on the flash memory is similar to the timing of write operations on the SRAM, however, there are additional considerations for writing flash memory.

The flash memory device is divided into multiple blocks of varying sizes. A block must be erased before locations within that block can be written. When a block is erased, all memory locations within that block are set to the value 0xFF (all bits 1). When writing to the flash memory, a 1 bit can be written to a 0, but a 0 bit can not be changed back to a 1 except by erasing the entire block. Writing a 0 over the top of a bit whose value is already 0 will lead to wear-out of the device and should be avoided. In general, only bytes whose value is 0xFF should be written to.

A block erase is performed by writing the erase command sequence to any address within the block. A block erase can take several milliseconds to complete and the device status should be checked to ensure that the erase has completed before attempting to issue another erase command sequence or a write command sequence to the device.

A location in the flash memory is written by writing the write command sequence to the address of the location to be written. Similarly to the erase command, a write command takes several microseconds to complete and the device status should be checked to ensure that the write has completed before initiating another write operation.

Power Supplies

The MEM1 draws power from two pins on the 40-pin interface connector: pin 37 supplies 3.3V; pin 39 provides system GND. Pin 40 supplies unregulated voltage (VU) from the system board, however, VU is not used on the MEM1.

Expansion Connector

Connector pinouts are shown below. Separately available tables show FPGA pin connections for the devices on the MEM1 when it is attached to various Digilent system boards.

Note that connectors on system boards and peripheral boards use the same numbering scheme – that is, if the board is held with the component side towards you and the connectors pointing up, then pin #1 is always on the bottom left corner of the connector.

This means that when a peripheral board is plugged into a system board, the numbering patterns are mirrored. Pin #1 on the peripheral board mates with pin #39 on the system board, peripheral board pin #2 mates with system pin #40, etc. Note that odd pin number mating pairs add to 40, and even pin number mating pairs add to 42 (so pin 36 mates with pin 6, pin 27 mates with pin 13, etc.).

MEM1 Connector Signals		
P1	**Signal**	**Dir**
1	nc	
2	nc	
3	nc	
4	nc	
5	A18	in
6	nc	
7	A17	in
8	A16	in
9	A15	in
10	A14	in
11	A13	in
12	A12	in
13	A11	in
14	A10	in
15	A9	in
16	A8	in
17	A7	in
18	A6	in
19	nc	
20	CS1	in
21	DB7	inout
22	CS0	in
23	DB6	inout
24	OE	in
25	DB5	inout
26	WE	in
27	DB4	inout
28	A5	in
29	DB3	inout
30	A4	in
31	DB2	inout
32	A3	in
33	DB1	inout
34	A2	in
35	DB0	inout
36	A1	in
37	**VCC33**	
38	A0	in
39	**GND**	
40	**VU**	