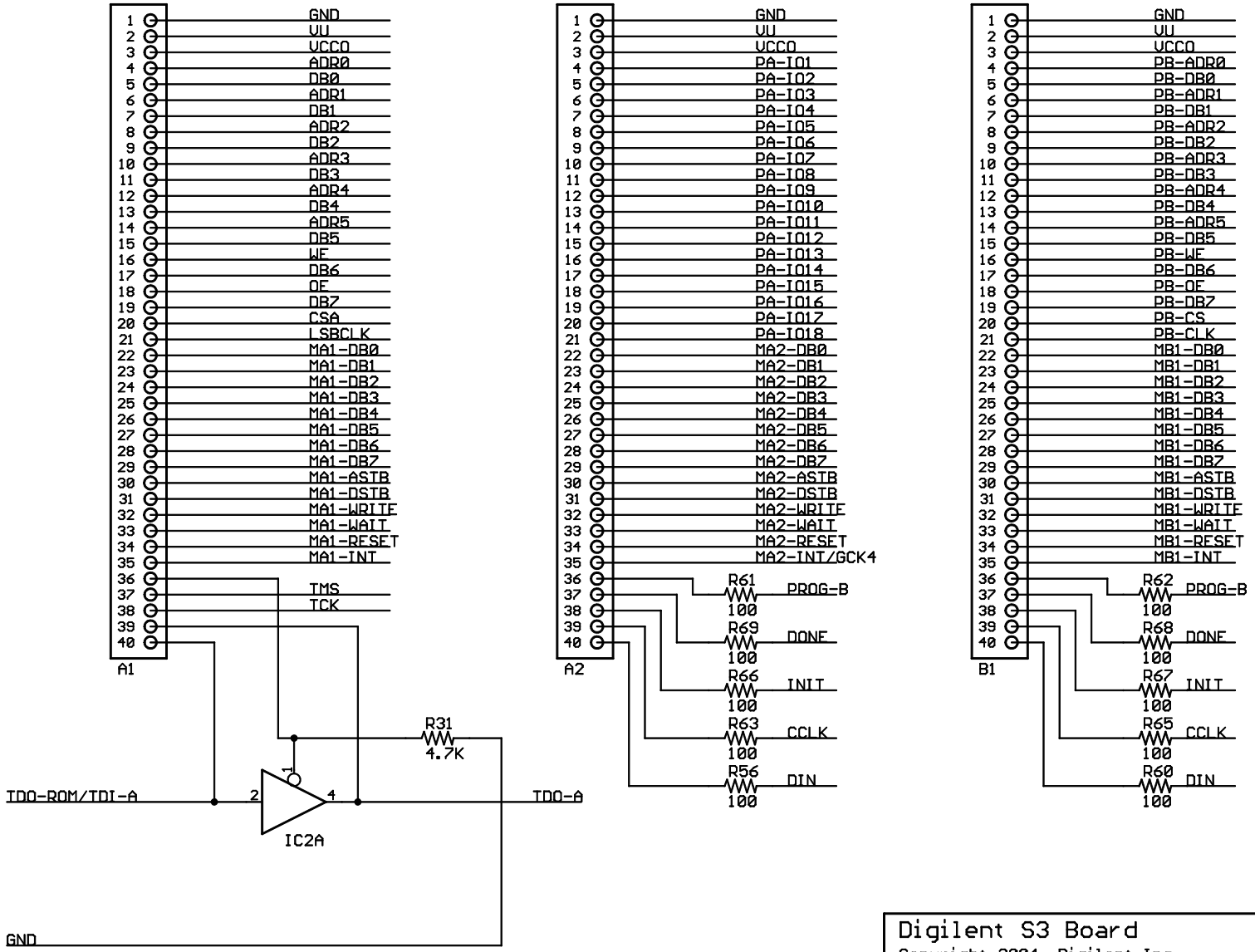

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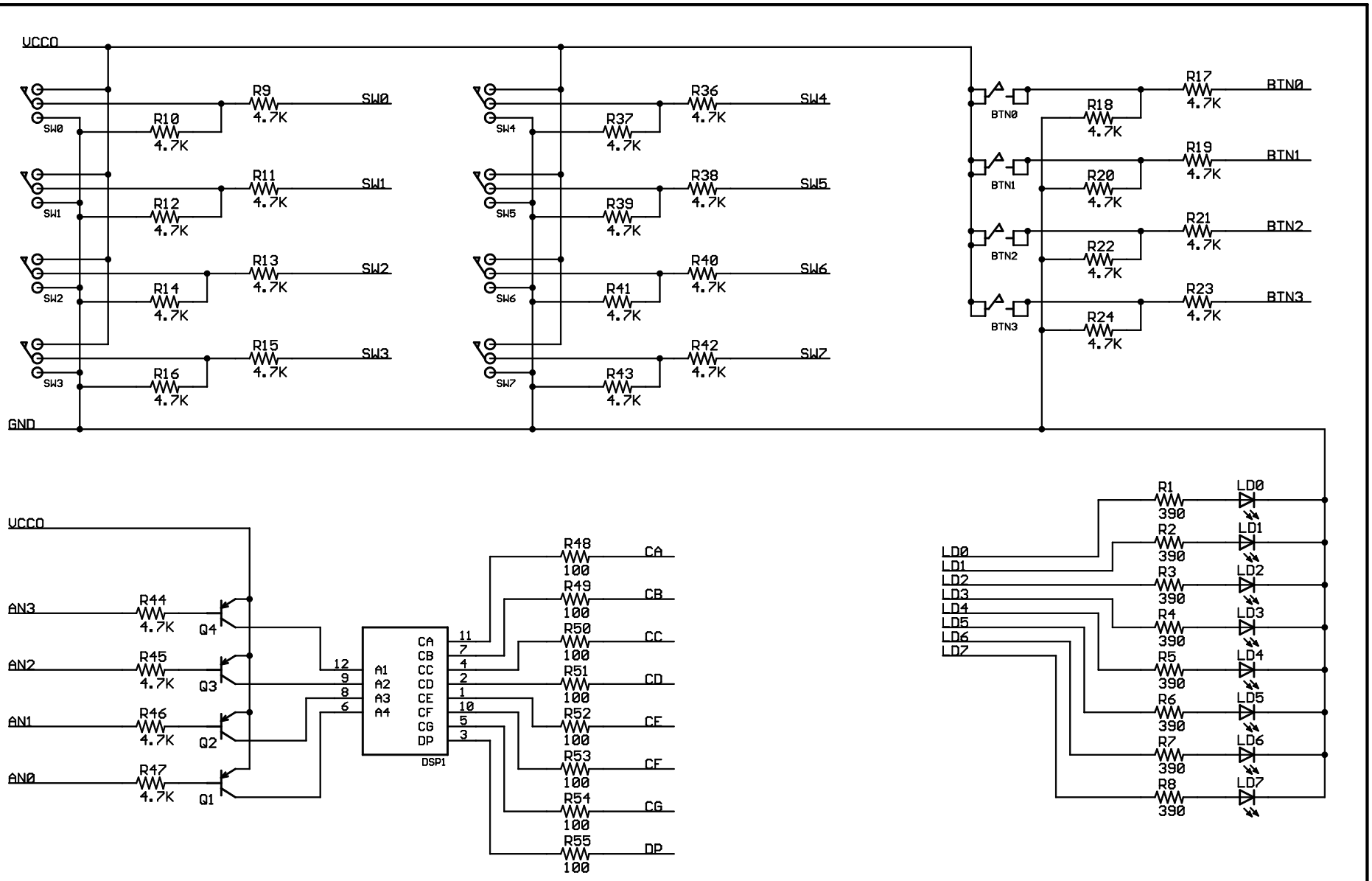

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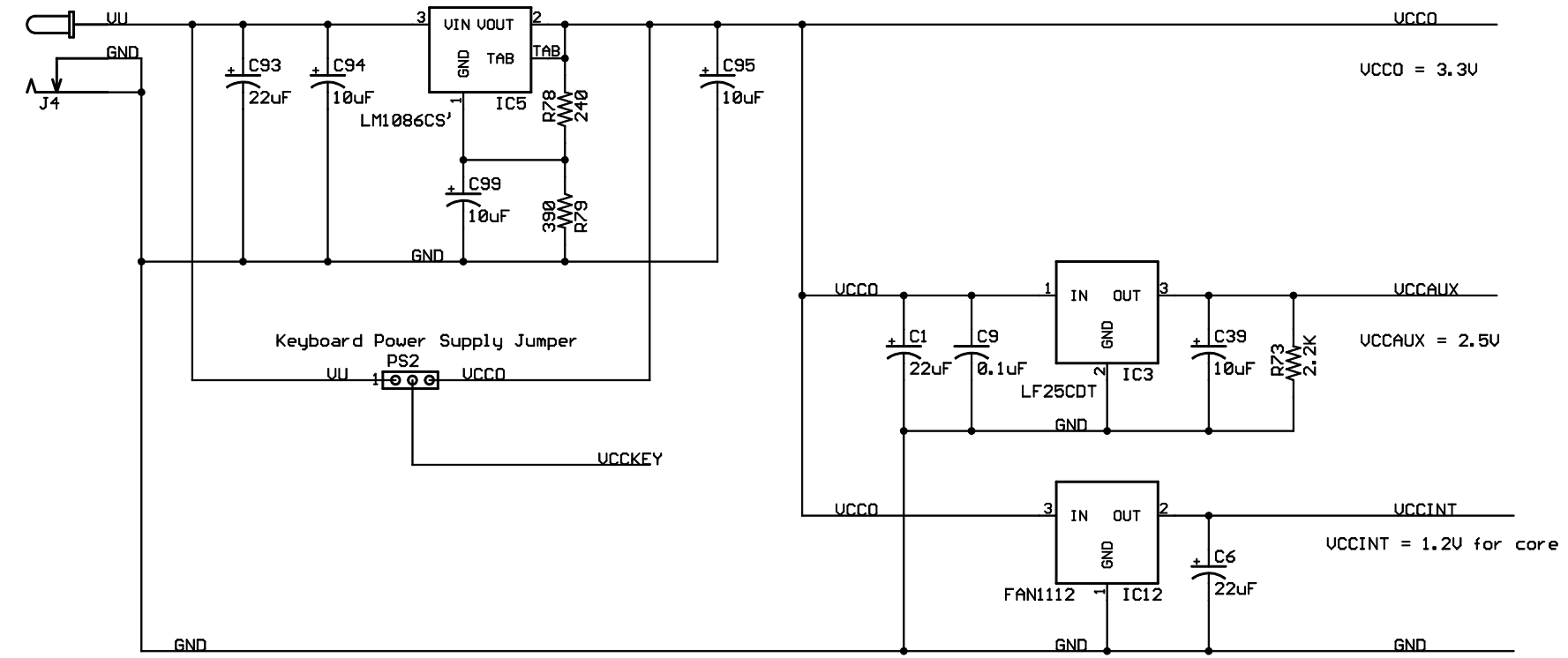

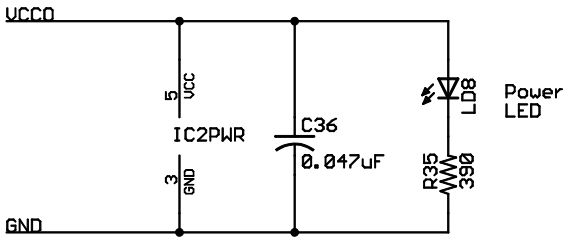

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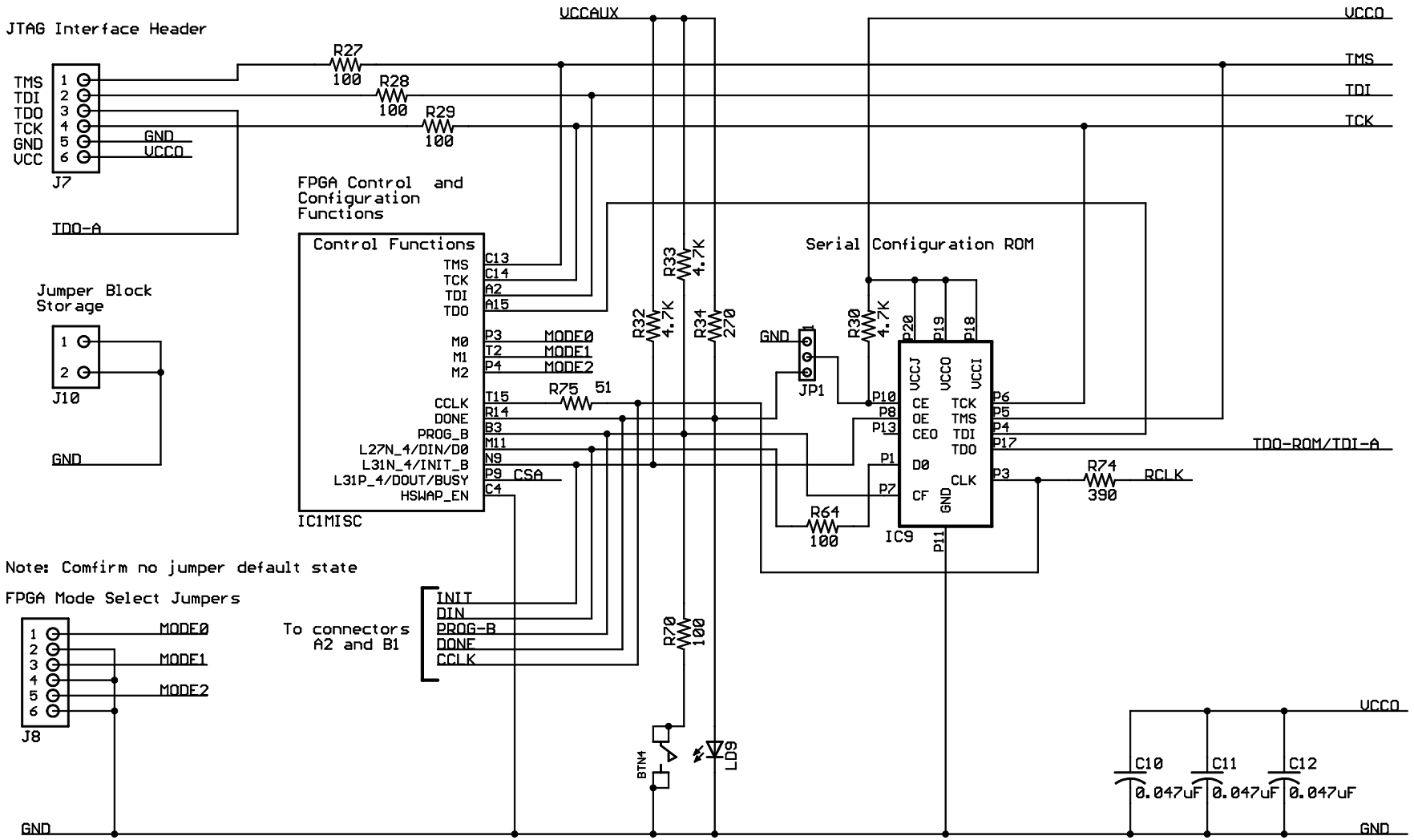

Notes: A shorting block must be installed between TDI and TDO on J7 to complete the scan chain when the JTAG signals are being driven from a peripheral board position rather than the JTAG Interface Header

Shorting blocks are installed on pins 2-3 of JP1 and JP2 to bypass the the serial configuration rom (IC9).

Shorting blocks should be installed on MODE0 and MODE1 of J8 to select Slave Serial Mode when configuring from the ROM

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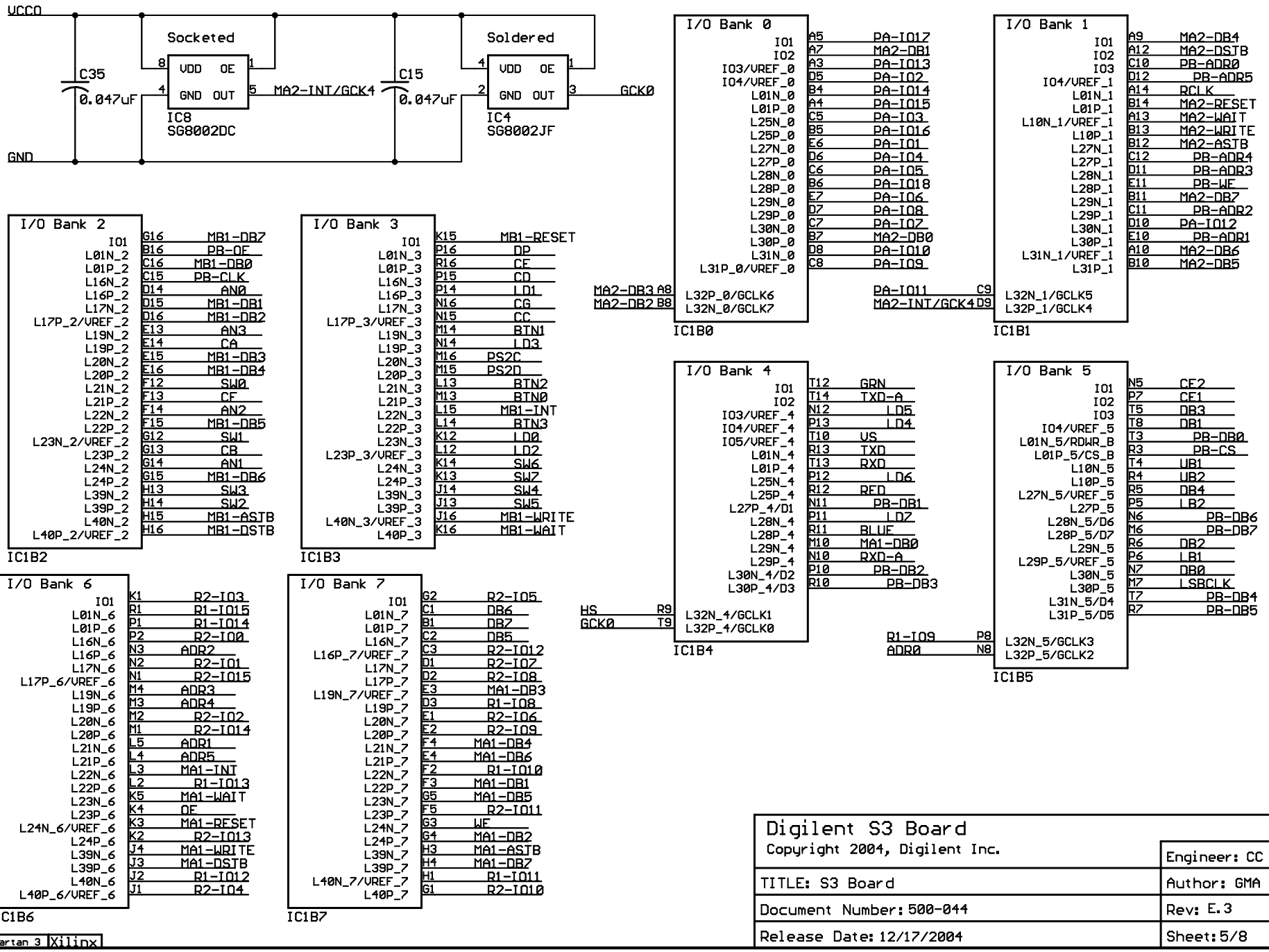
Release Date: 12/17/2004	Sheet: 4/8


VCCO
GND
C35
0.047uF
C15
0.047uF
Socketed
IC8
SG8002DC
MA2-INT/GCK4
Soldered
IC4
SG8002JF
GCK0
I/O Bank 0
L31P_0/VREF_0
L32P_0/GCLK6
L32N_0/GCLK7
MA2-DB3 A8
MA2-DB2 B8
IC1B0
I/O Bank 1
L31N_1/VREF_1
L32N_1/GCLK5
L32P_1/GCLK4
PA-IO11 C9
MA2-INT/GCK4 D9
IC1B1
I/O Bank 2
L23N_2/VREF_2
L40P_2/VREF_2
IC1B2
I/O Bank 3
L40N_3/VREF_3
IC1B3
I/O Bank 4
L30P_4/D3
L32N_4/GCLK1
L32P_4/GCLK0
HS R9
GCK0 T9
IC1B4
I/O Bank 5
L32N_5/GCLK3
L32P_5/GCLK2
R1-IO9 P8
ADR0 N8
IC1B5
I/O Bank 6
L40P_6/VREF_6
IC1B6
I/O Bank 7
L40N_7/VREF_7
IC1B7
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Release Date: 12/17/2004
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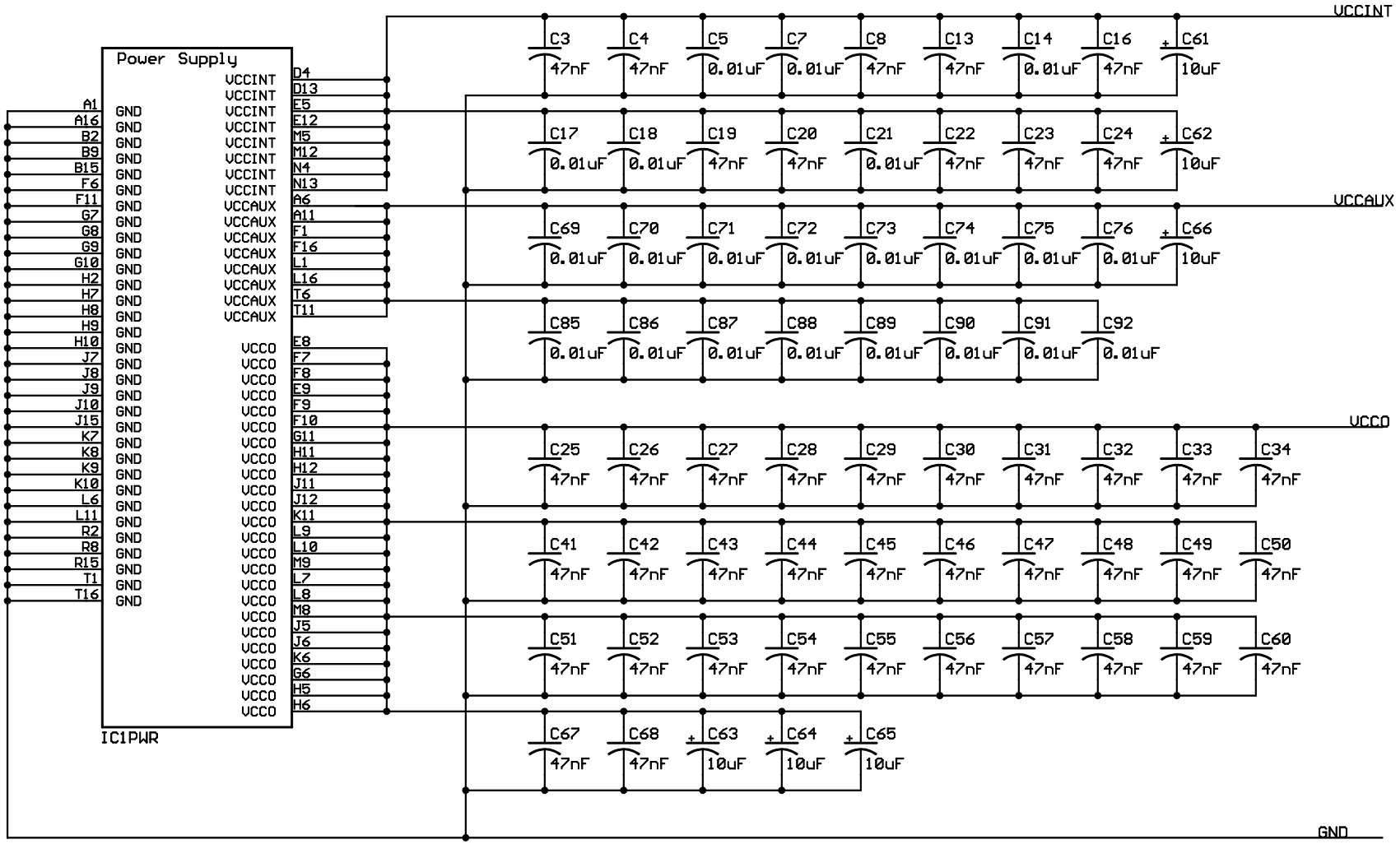
Sheet: 5/8
Spartan 3 Xilinx



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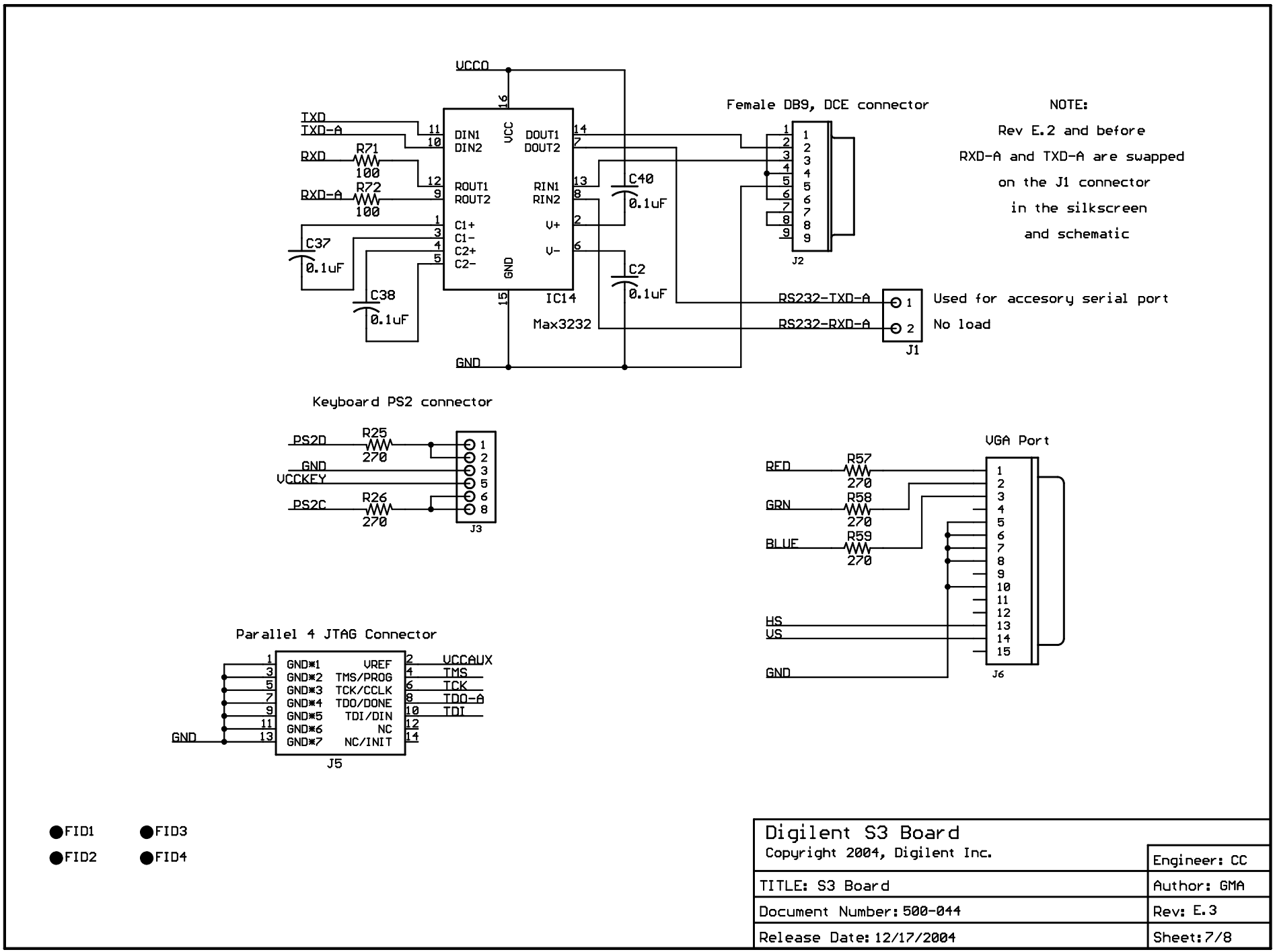
Release Date: 12/17/2004	Sheet: 6/8



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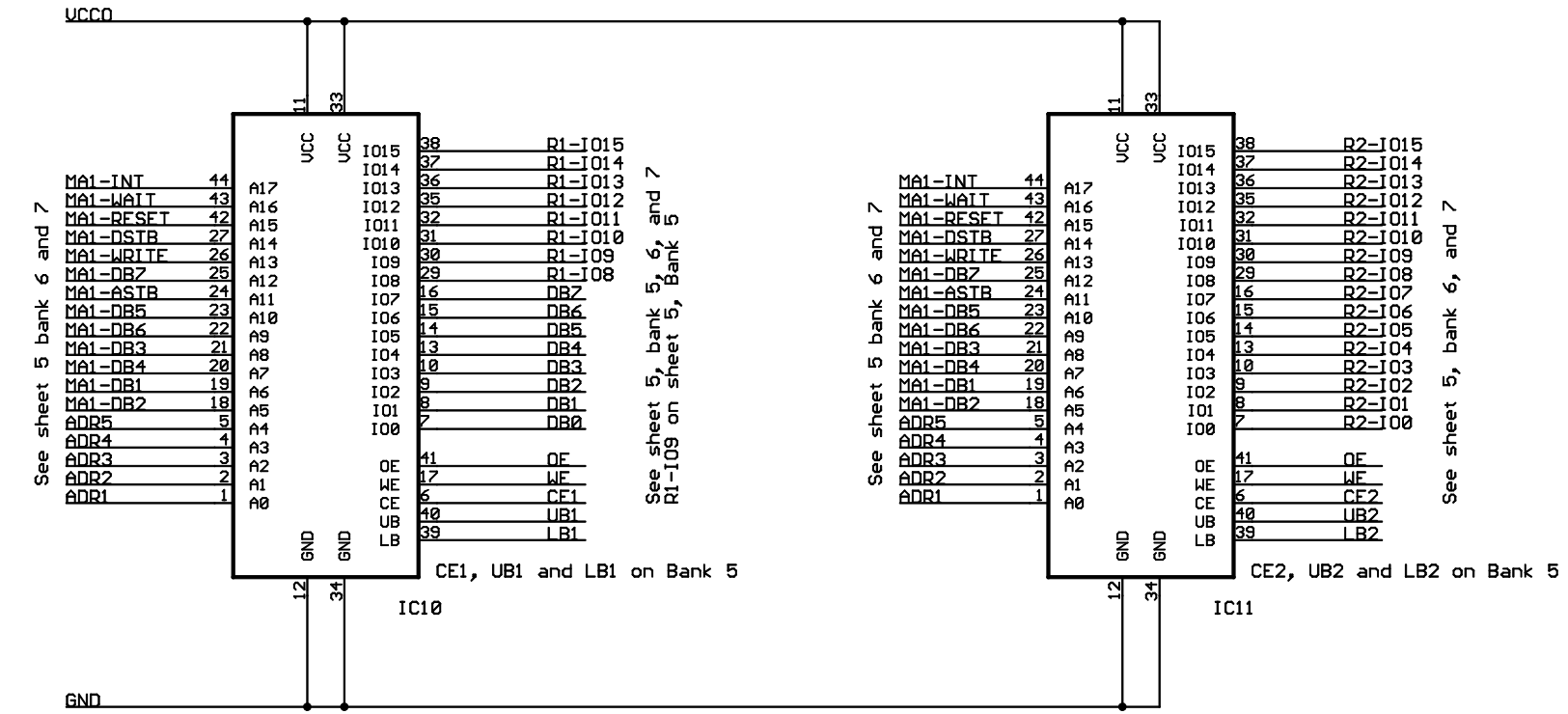

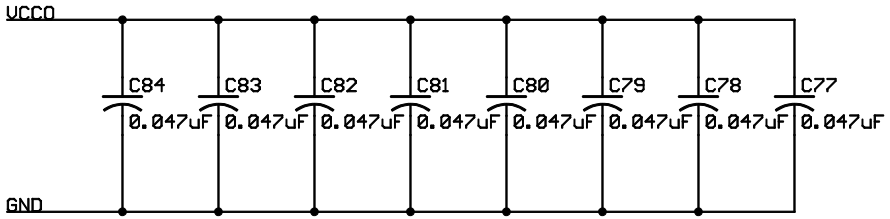

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