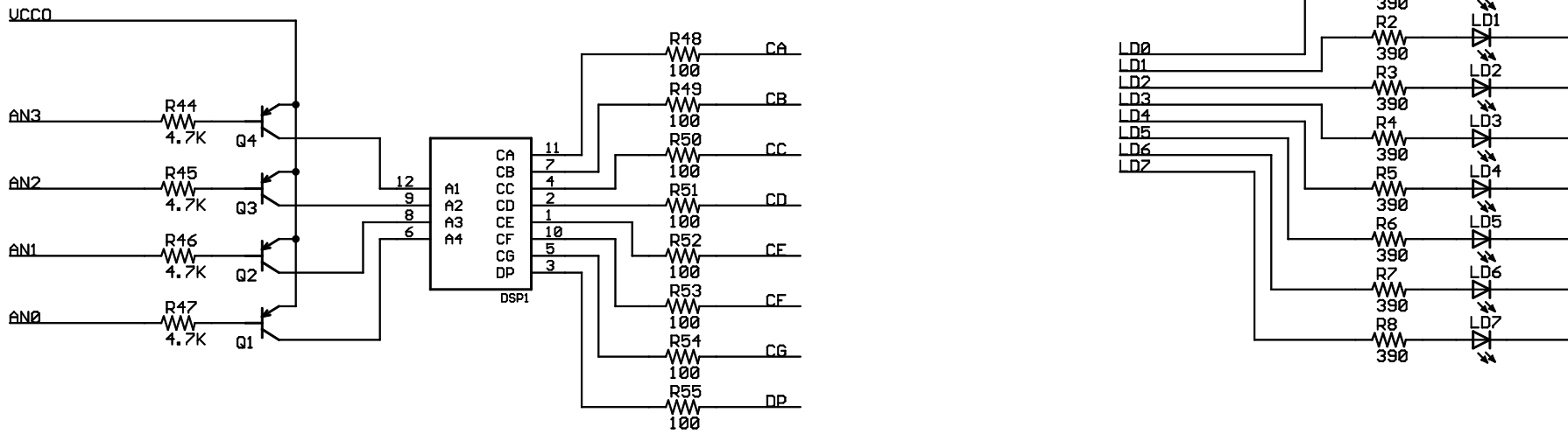
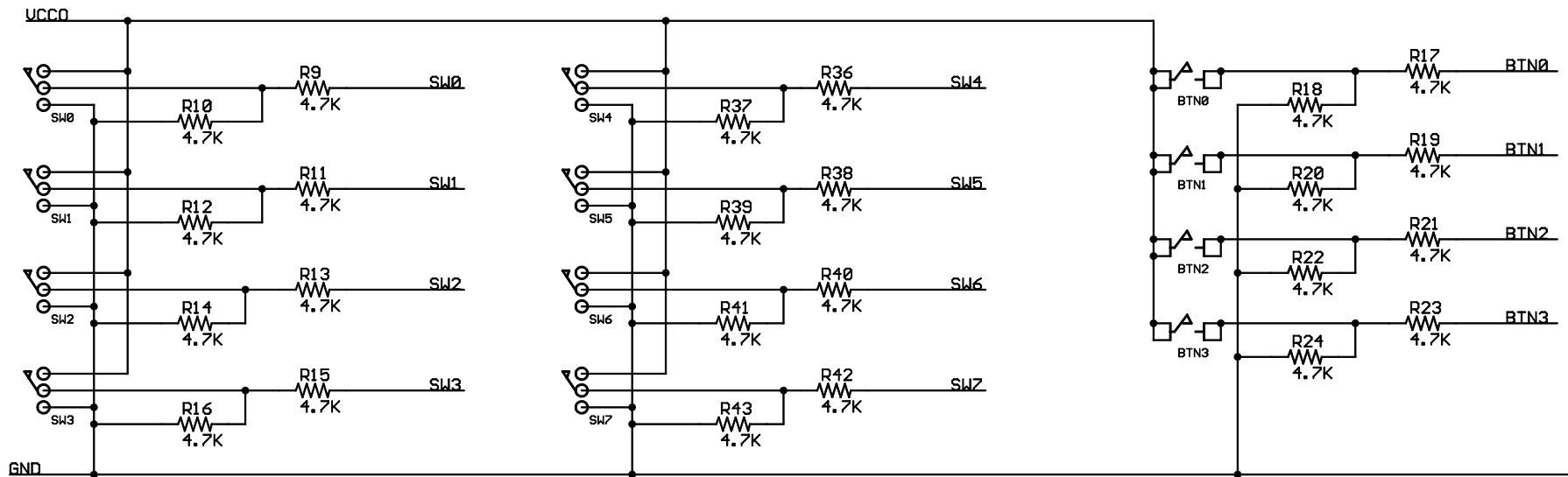
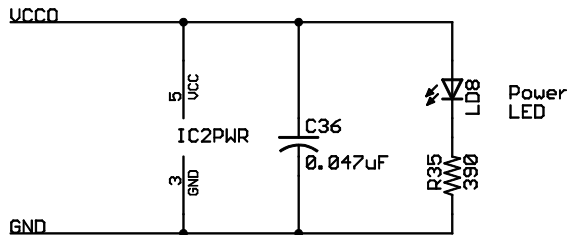
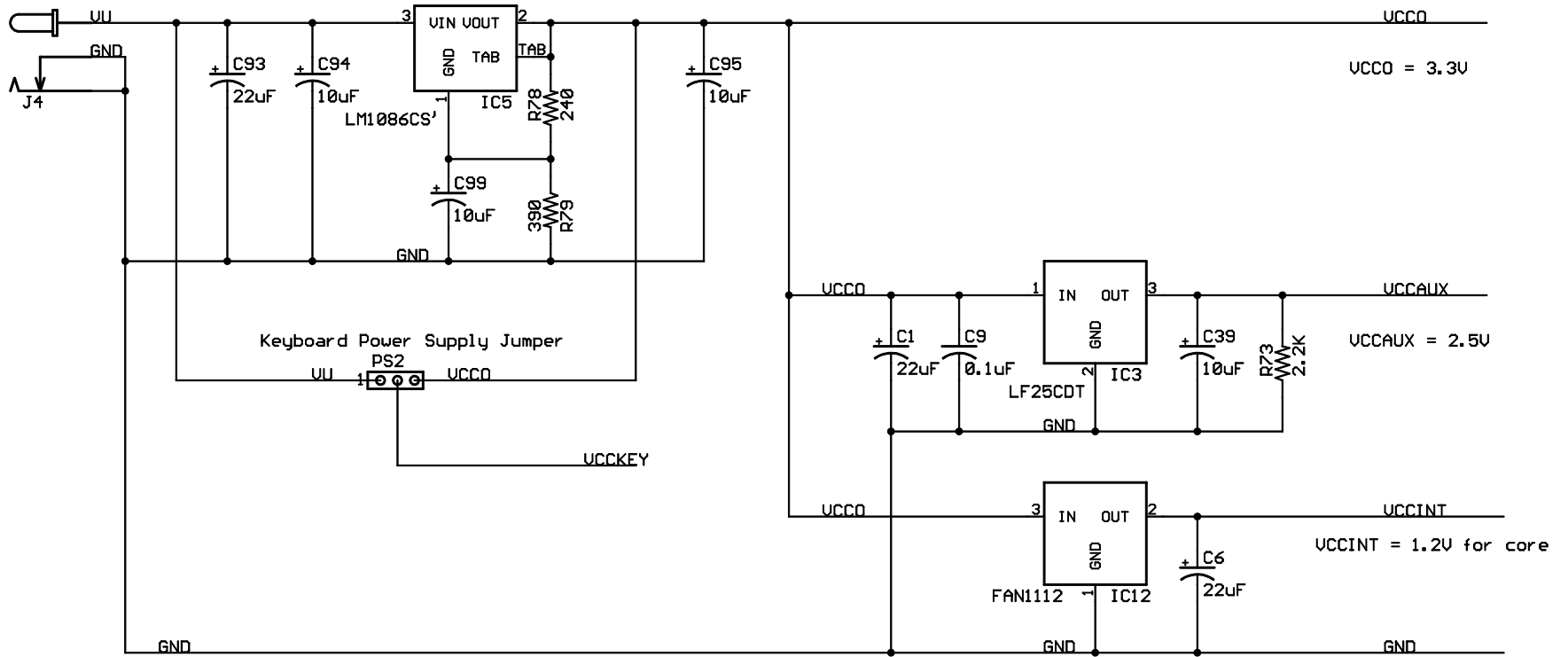


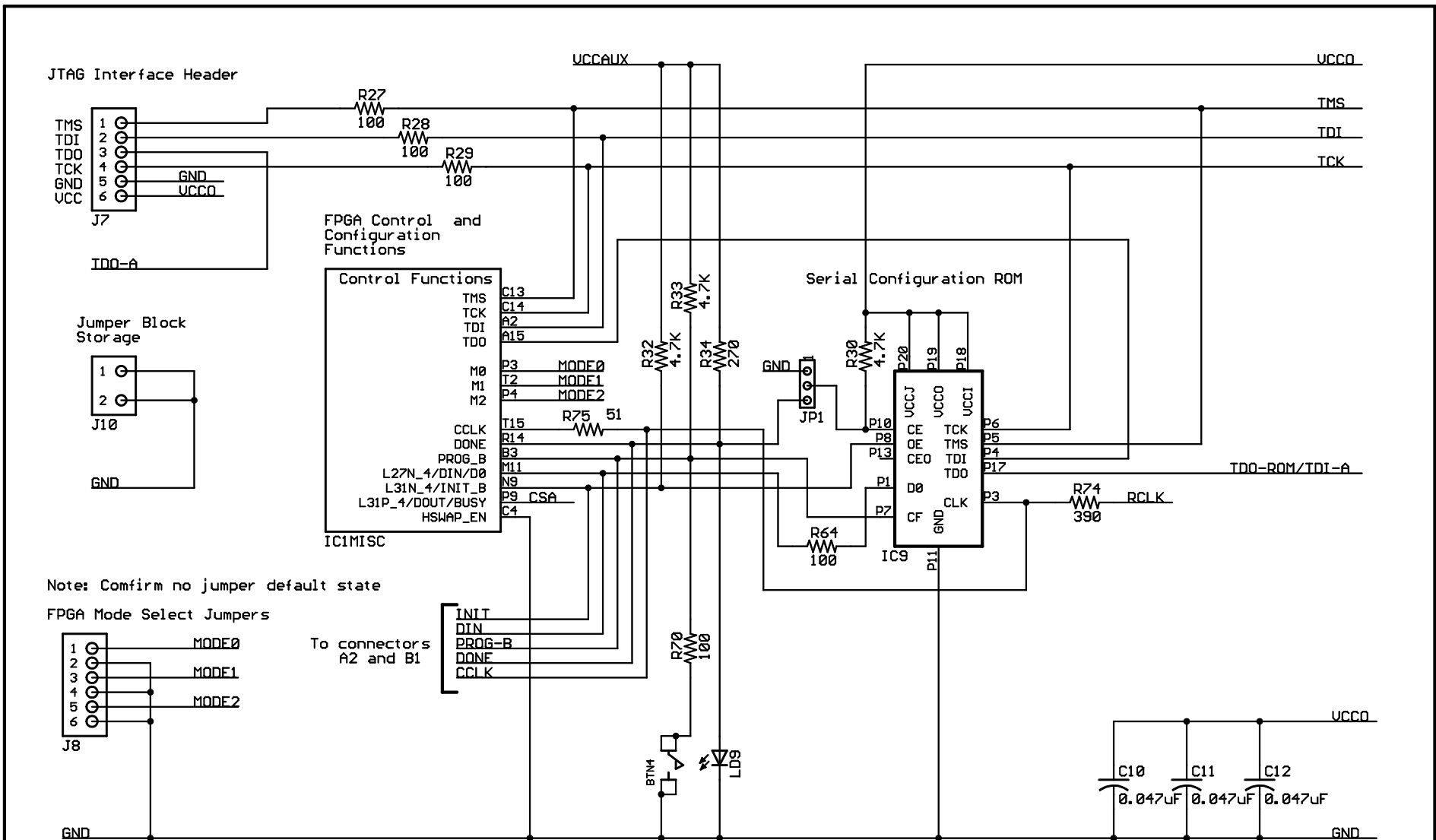
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Note: Confirm no jumper default state

FPGA Mode Select Jumpers

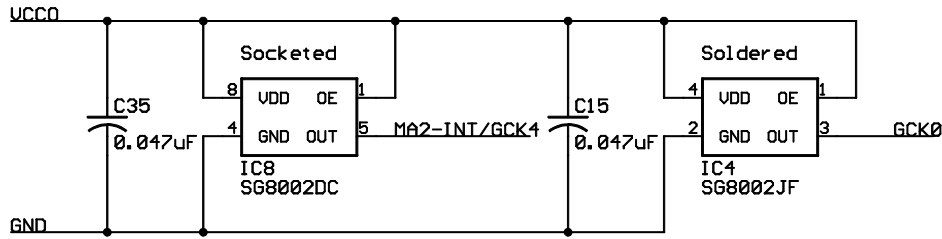
To connectors A2 and B1

Notes: A shorting block must be installed between TDI and TDO on J7 to complete the scan chain when the JTAG signals are being driven from a peripheral board position rather than the JTAG Interface Header

Shorting blocks are installed on pins 2-3 of JP1 and JP2 to bypass the the serial configuration rom (IC9).

Shorting blocks should be installed on MODE0 and MODE1 of J8 to select Slave Serial Mode when configuring from the ROM

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I/O Bank 0	
I01	A5 PA-I012
A7	MA2-DB1
A3	PA-I013
I03	D5 PA-I02
I04/VREF_0	B4 PA-I014
L01N_0	A4 PA-I015
L01P_0	C5 PA-I03
L25N_0	B5 PA-I016
L25P_0	E6 PA-I01
L27N_0	D6 PA-I04
L27P_0	C6 PA-I05
L28N_0	B6 PA-I018
L28P_0	E7 PA-I06
L29N_0	D7 PA-I08
L29P_0	C7 PA-I07
L30N_0	B7 MA2-DB0
L30P_0	D8 PA-I010
L31N_0	C8 PA-I09
L31P_0/VREF_0	
L32P_0/GCLK6	PA-I011 C9
L32N_0/GCLK7	MA2-INT/GCK4 D9

I/O Bank 1	
I01	A9 MA2-DB4
I02	A12 MA2-DSTB
I03	C10 PB-ADDR0
I04/VREF_1	D12 PB-ADDR5
L01N_1	A14 RCLK
L01P_1	B14 MA2-RESET
L10N_1/VREF_1	A13 MA2-WAIT
L10P_1	B13 MA2-WRITE
L27N_1	B12 MA2-ASTB
L27P_1	C12 PB-ADDR4
L28N_1	D11 PB-ADDR3
L28P_1	E11 PB-WF
L29N_1	B11 MA2-DB7
L29P_1	C11 PB-ADDR2
L30N_1	D10 PA-I012
L30P_1	E10 PB-ADDR1
L31N_1/VREF_1	A10 MA2-DB6
L31P_1	B10 MA2-DB5
L32N_1/GCLK5	
L32P_1/GCLK4	

I/O Bank 2	
I01	G16 MB1-DB7
L01N_2	B16 PB-OF
L01P_2	C16 MB1-DB0
L16N_2	C15 PB-CLK
L16P_2	D14 AN0
L17N_2	D15 MB1-DB1
L17P_2/VREF_2	D16 MB1-DB2
L19N_2	E13 AN3
L19P_2	E14 CA
L20N_2	E15 MB1-DB3
L20P_2	E16 MB1-DB4
L21N_2	F12 SW0
L21P_2	F13 CF
L22N_2	F14 AN2
L22P_2	F15 MB1-DB5
L23N_2/VREF_2	G12 SW1
L23P_2	G13 CB
L24N_2	G14 AN1
L24P_2	G15 MB1-DB6
L39N_2	H13 SW3
L39P_2	H14 SW2
L40N_2	H15 MB1-ASTB
L40P_2/VREF_2	H16 MB1-DSTB

I/O Bank 3	
I01	K15 MB1-RESET
L01N_3	P16 DP
L01P_3	R16 CF
L16N_3	P15 CD
L16P_3	P14 I D1
L17N_3	N16 CG
L17P_3/VREF_3	N15 CC
L19N_3	M14 BTN1
L19P_3	N14 I D3
L20N_3	M16 PS2C
L20P_3	M15 PS2D
L21N_3	L13 BTN2
L21P_3	M13 BTN0
L22N_3	L15 MB1-INT
L22P_3	L14 BTN3
L23N_3	K12 I D0
L23P_3/VREF_3	L12 I D2
L24N_3	K14 SW6
L24P_3	K13 SW2
L39N_3	J14 SW4
L39P_3	J13 SW5
L40N_3/VREF_3	J16 MB1-WRITE
L40P_3	K16 MB1-WAIT

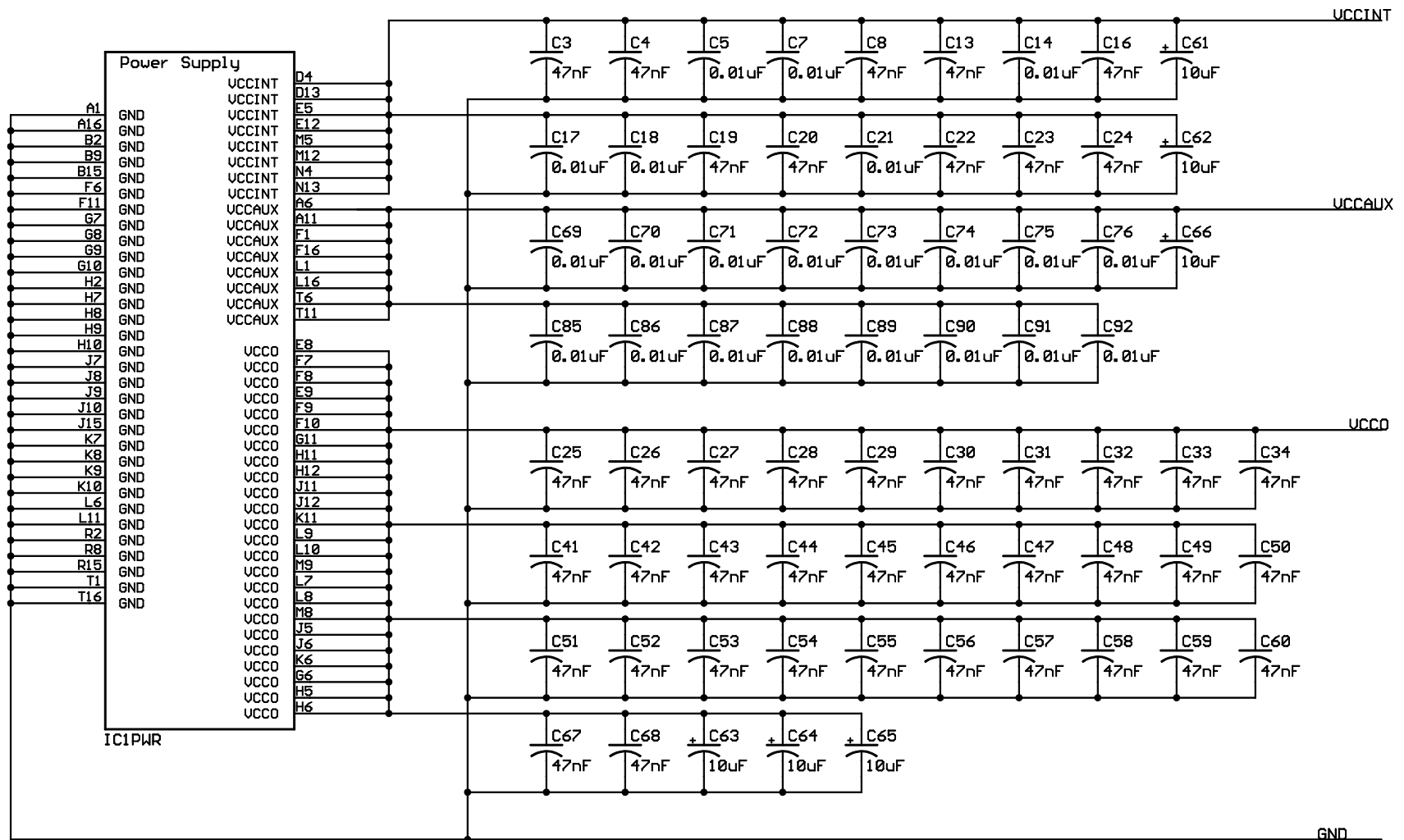
I/O Bank 4	
I01	T12 GRN
I02	T14 TXD-A
I03/VREF_4	N12 I D5
I04/VREF_4	P13 I D4
I05/VREF_4	T10 US
L01N_4	R13 TXD
L01P_4	T13 RXD
L25N_4	P12 I D6
L25P_4	R12 RFD
L27P_4/D1	N11 PB-DB1
L28N_4	P11 I DZ
L28P_4	R11 BLUF
L29N_4	M10 MA1-DB0
L29P_4	N10 RXD-A
L30N_4/D2	P10 PB-DB2
L30P_4/D3	R10 PB-DB3
L32N_4/GCLK1	
L32P_4/GCLK0	

I/O Bank 5	
I01	N5 CE2
I02	P7 CE1
I03	T5 DB3
I04/VREF_5	T8 DB1
L01N_5/RDWR_B	T3 PB-DB0
L01P_5/CS_B	R3 PB-CS
L10N_5	T4 UB1
L10P_5	R4 UB2
L27N_5/VREF_5	R5 DB4
L27P_5	P5 LB2
L28N_5/D6	N6 PB-DB6
L28P_5/D7	M6 PB-DB7
L29N_5	R6 DB2
L29P_5/VREF_5	P6 LB1
L30N_5	N7 DB0
L30P_5	M7 LSCLK
L31N_5/D4	T7 PB-DB4
L31P_5/D5	R7 PB-DB5
L32N_5/GCLK3	
L32P_5/GCLK2	

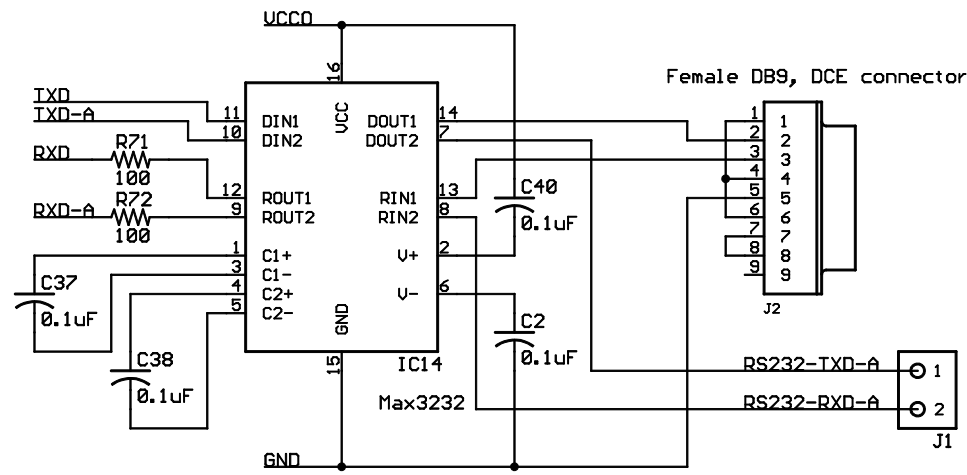
I/O Bank 6	
I01	K1 R2-I03
L01N_6	R1 R1-I015
L01P_6	P1 R1-I014
L16N_6	P2 R2-I00
L16P_6	N3 ADDR2
L17N_6	N2 R2-I01
L17P_6/VREF_6	N1 R2-I015
L19N_6	M4 ADDR3
L19P_6	M3 ADDR4
L20N_6	M2 R2-I02
L20P_6	M1 R2-I014
L21N_6	L5 ADDR1
L21P_6	L4 ADDR5
L22N_6	L3 MA1-INT
L22P_6	L2 R1-I013
L23N_6	K5 MA1-WAIT
L23P_6	K4 OF
L24N_6/VREF_6	K3 MA1-RESET
L24P_6	K2 R2-I013
L39N_6	J4 MA1-WRITE
L39P_6	J3 MA1-DSTB
L40N_6	J2 R1-I012
L40P_6/VREF_6	J1 R2-I04

I/O Bank 7	
I01	G2 R2-I05
L01N_7	C1 DB6
L01P_7	B1 DB7
L16N_7	C2 DB5
L16P_7/VREF_7	C3 R2-I012
L17N_7	D1 R2-I07
L17P_7	D2 R2-I08
L19N_7/VREF_7	E3 MA1-DB3
L19P_7	D3 R1-I08
L20N_7	E1 R2-I06
L20P_7	E2 R2-I09
L21N_7	F4 MA1-DB4
L21P_7	E4 MA1-DB6
L22N_7	F2 R1-I010
L22P_7	F3 MA1-DB1
L23N_7	G5 MA1-DB5
L23P_7	F5 R2-I011
L24N_7	G3 WF
L24P_7	G4 MA1-DB2
L39N_7	H3 MA1-ASTB
L39P_7	H4 MA1-DB7
L40N_7/VREF_7	H1 R1-I011
L40P_7	G1 R2-I010

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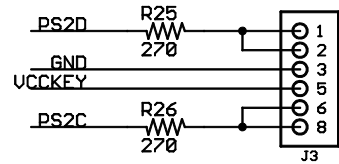
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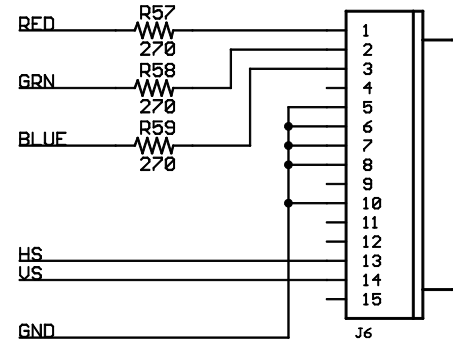
NOTE:
 Rev E.2 and before
 RXD-A and TXD-A are swapped
 on the J1 connector
 in the silkscreen
 and schematic

Used for accessory serial port
 No load

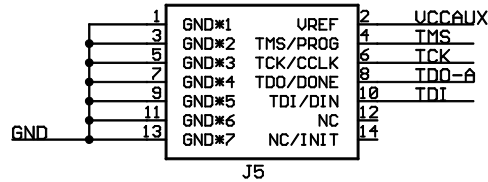
Keyboard PS2 connector



UGA Port

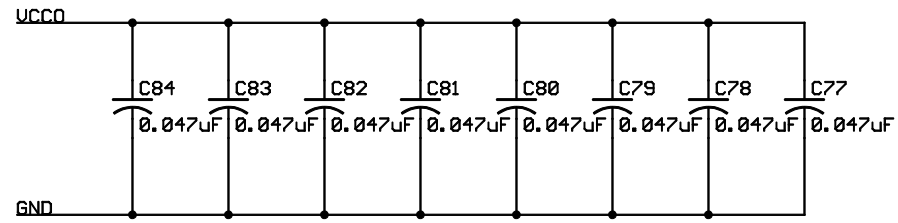
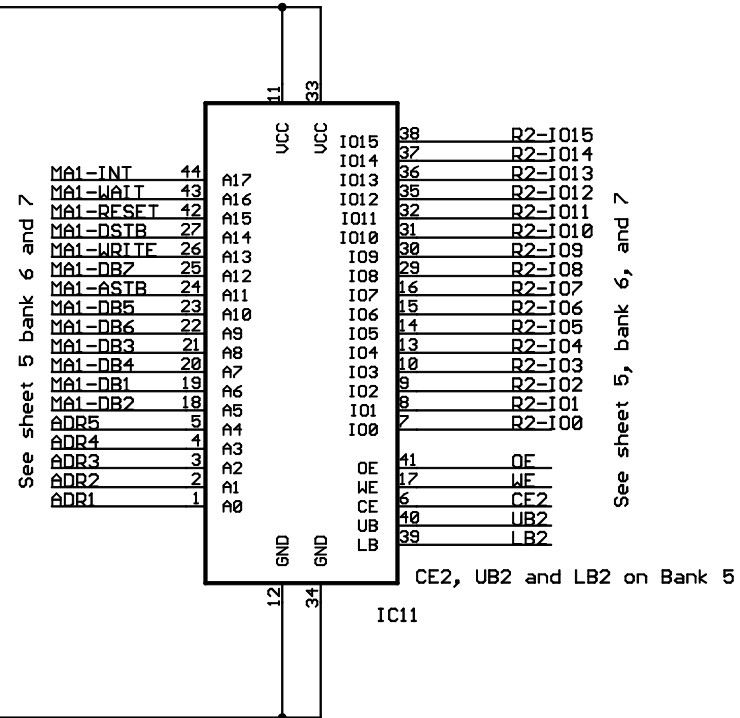
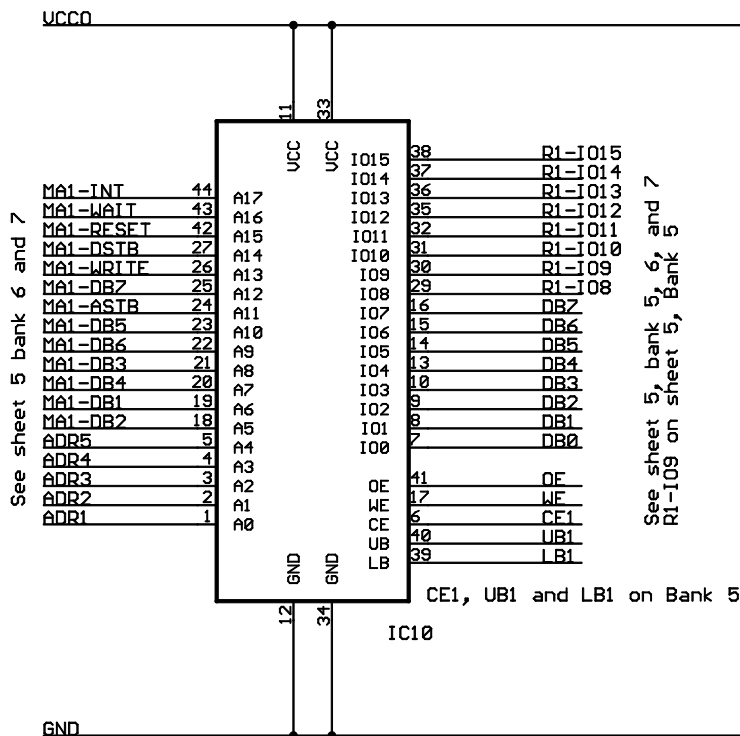


Parallel 4 JTAG Connector



- FID1 ● FID3
- FID2 ● FID4

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