Morph-IC Data Sheet
Version 1.0

Introduction

MORPH-IC combines the flexibility of FTDI's FT2232C USB interface I.C. together with an Altera ACEX 1K series FPGA (EP1K10TC100-3) in a compact ready to use module. The power and IO pins of the module are brought out onto 2 x 20pin, 0.1in pitch headers on the underside of the pcb, allowing easy connection to the pins on a 0.1in grid. The module can also be plugged into a pcb using readily available mating pcb connectors (two included). Included on the module are the 3.3V and 2.5V voltage regulators required by the FPGA as well as a 50MHz CMOS oscillator hard wired to one of its two clock pins. Power control to meet USB suspend current requirements is provided by the FT2232C and an on board MOSFET power switch.

MORPH-IC uses the Multi Protocol Synchronous Serial Engine (MPSSE) interface of the FT2232C to program / reprogram the FPGA over USB in a fraction of a second. Not only can the contents of the FPGA be defined over USB on initialising the application software by loading them from an Altera format configuration file, but the contents of the FPGA can be reloaded / redefined "almost" in real time (under 0.2 seconds). This effectively allows a single product to Morph between different hardware configurations under software control (via USB) from a single application.

The second channel of the FT2232C is hard wired to the IO pins of the FPGA. These can be used by the FPGA to communicate with the application software over USB at transfer rates of up to 1M Byte / second.

These features make MORPH-IC ideal for instrumentation, communications and other demanding application areas where flexibility and in-circuit hardware upgradability are of paramount importance.

MORPH-IC comes complete with USB drivers for Windows 98/ME/2000/XP, VHDL code examples, FPGA loader program (including Delphi source code) and a Windows DLL interface which can be used to interface it to most common Windows programming languages. Examples of DLL interfacing in Visual C++, Visual Basic and Borland Delphi are provided. Linux Drivers and a Linux version of the FPGA loader written in Kylix are also provided. An example project demonstrating IO over USB is included complete with VHDL and Delphi source code.

To complete the package, a second CD contaning the Quartus II Software Starter Suite is included. This contains the free Altera Quartus II Web Edition software which provides a complete environment for programmable logic device (PLD) design, including schematic- and text-based design entry, HDL synthesis, place-and-route, verification and simulation. This package runs under Windows NT/2000/XP and can be used to develop code for the on-board FPGA. Registration with Altera is required in order to run this package.

MORPH-ICs competitive pricing and quantity discount structure make it ideal for incorporating into low - medium volume designs. As it comes complete with all FPGA development software required and example code it is also ideal as a classroom training tool for colleges and universities as well as engineers wanting to learn more about hardware development using FPGAs.

A range of optional training kits is under development which will allow students / engineers to study various areas of electronic engineering including A/D and D/A converters, video controllers and TV interfacing. Training kits consist of an assembled pcb with all the components required for the projects into which you plug a MORPH-IC module (extra). Training kits also come with a CD containing VHDL code and software source code for the projects in the kit. 3rd party contributions are also welcome - if you have a MORPH-IC project you would like to share with others please contact us.

Key Features

- FT2232C Dual USB UART / FIFO I.C.
- Altera Acex™ EP1K10TC100-3 FPGA
- Ultra fast FPGA configuration / reconfiguration over USB (under 0.2 sec)
- 576 Embedded FPGA Logic Elements (== 10,000 gates typical)
- 3 Embedded Logic RAM / ROM Elements (== 1.5k bytes memory)
- FPGA – PC USB Data Transfer at up to 1M Byte/sec
- Onboard 93C56 configuration EEPROM
- MOSFET switched 5v and 3.3v power outputs for powering external logic.
- Onboard 6MHz crystal and essential support components for FT2232C.
- Onboard 50MHz oscillator as FPGA primary clock.
- Onboard LEDs indicate USB driver enumeration and successful FPGA device programming.
- 36 dedicated external IO pins
- 8 shared external IO pins
- 4 dedicated external input pins
- 1 dedicated external clock input
- Powered from USB bus or external PSU
- Standard 0.1in pitch format connector pins, ideal for rapid prototyping and small-medium size production runs.
- FTDI's VCP and D2XX USB Windows and Linux USB drivers (provided) eliminate the need for driver development in most cases.
- Windows FPGA loader interface DLL supplied including interface examples in VB, VC++ and Delphi.
- Stand-alone FPGA loader programs provided for Windows and Linux.
- VHDL programming examples (I/O over USB) provided.
- Delphi application software examples including source code provided.
- MORPH-IC schematics provided.
- Free Altera Quartus II Web Edition development software included.

FIGURE 1 - MORPH-IC BLOCK DIAGRAM (simplified)

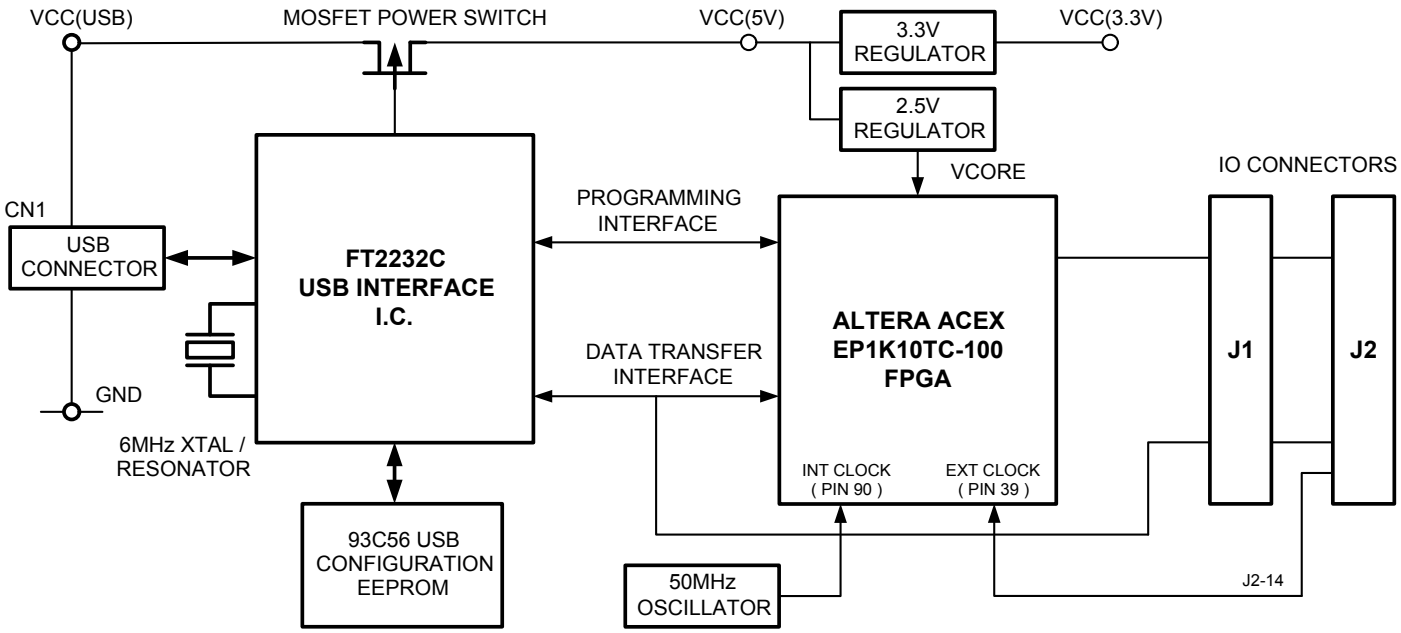


FIGURE 2 - MORPH-IC KEY COMPONENT LOCATION

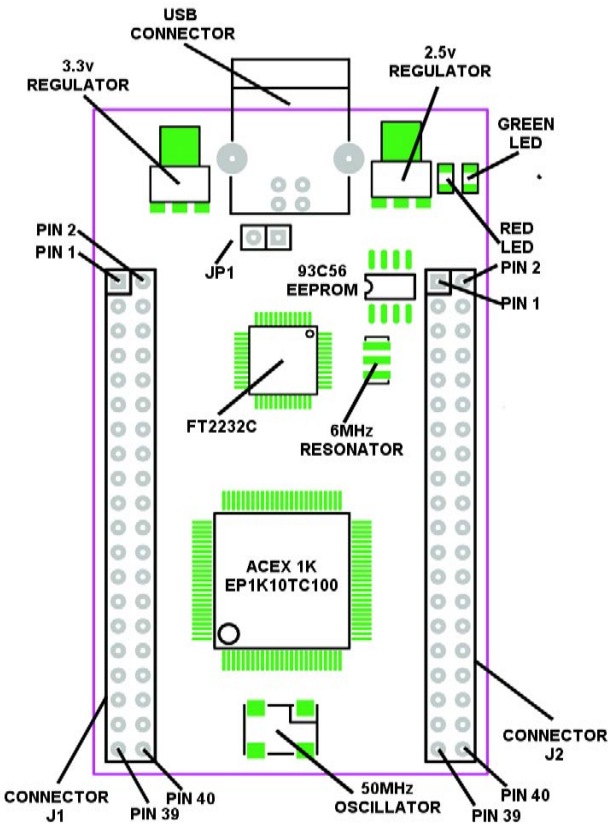


Figure 2 (left) shows the location of the key components on the MORPH-IC module viewed from above. The module is connected to USB by plugging a USB "A" to "B" cable (available separately) into the USB type "B" connector shown at the top. Fitting a jumper on JP1 selects USB Bus Powered Mode (the default) where the module obtains its power from USB. To change the module to USB self powered mode, remove the jumper on JP1 and supply +5v from an external PSU to J1 pin 1. The 93C56 EEPROM is pre-programmed at the factory with the correct defaults for MORPH-IC operation. If re-programming this using FTDI's MPROG utility, great care must be taken or the module and its utilities may cease to work.

Two voltage regulators are provided on the module - the 2.5V regulator provides the power to the FPGA core logic, whilst the 3.3V regulator provides power to the FPGA IO cells. The output of the 3.3V regulator is available through dedicated pins on J1 and J2 to supply up to 250mA of current to external logic. The 3.3v supply is switched off during USB suspend to conserve current.

A 50Mhz oscillator is provided on the module and is hard wired to clock pin 90 of the EP1K10TC-100 FPGA. For applications requiring a different clock frequency, use clock pin 39 of the FPGA which is connected to J2 pin 14. A full listing of the pinouts of J1 and J2 is provided in Figure 5.

A 6MHz resonator on the module provides the master clock for the FT2232C. For detailed descriptions of the FT2232C and EP1K10TC-100, please consult the relevant data sheets. The FT22232C data sheet and application note can be found on the enclosed CD. The EP1K10TC-100 data sheet can be found on the Altera web site at http://www.altera.com/literature/lit-acx.jsp

FIGURE 3 - MORPH-IC FPGA PROGRAMMING INTERFACE

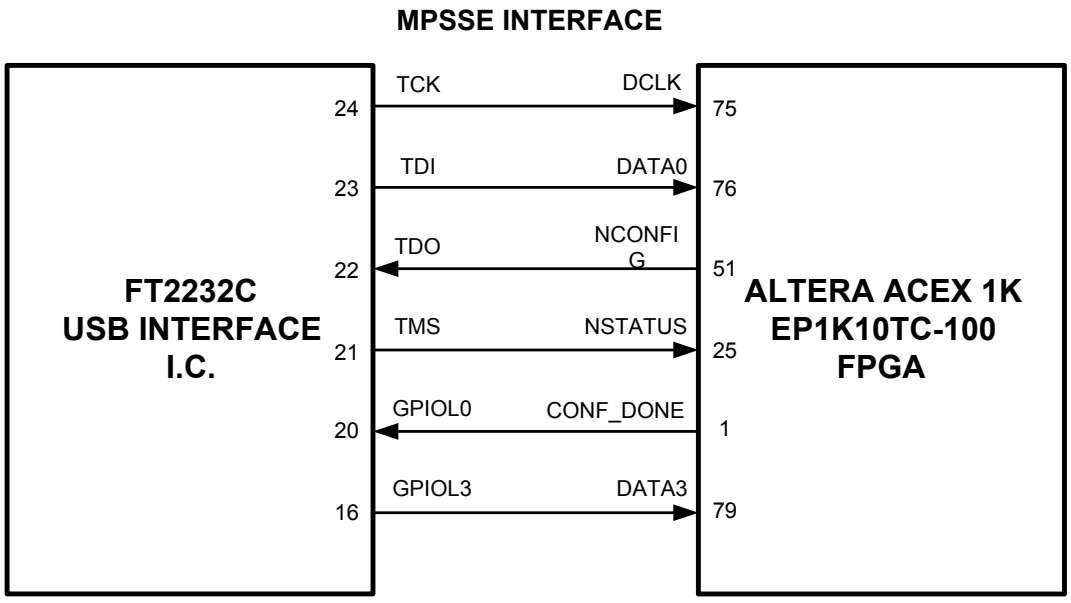


Figure 3 shows the programming interface between the FT2232C and the EP1K10TC-100. It uses the multi-protocol synchronous serial engine feature (MPSSE) of the FT2232C channel A to program the FPGA "on-the-fly". The FPGA can be programmed / reprogrammed in under 0.2 seconds which makes it possible to design some type of products that would not normally fit into this size of FPGA by using several different configuration files for different modes of operation and loading / re-loading these transparently to the end-user. The configuration files are output from the Altera Quartus ™ software and can be downloaded into the FPGA either manually by using the loader program supplied or under application software control by using the DLL supplied.
For further details of MPSSE operation, consult the FT2232C data sheet and the application note AN2232C-01 downloadable from FTDI's web site at page http://www.ftdichip.com/FT2232C2.htm. The source code for the loader program and the DLL illustrate how to program the MPSSE as an Altera ACEX series loader. MORPH-IC uses the GPIOL0 pin of the FT2232C to detect / verify the completion of FPGA device configuration and the GPIOL3 pin of the FT2232C to provide a reset to the FPGA via pin 79.

FIGURE 4 - MORPH-IC FPGA DATA TRANSFER INTERFACE

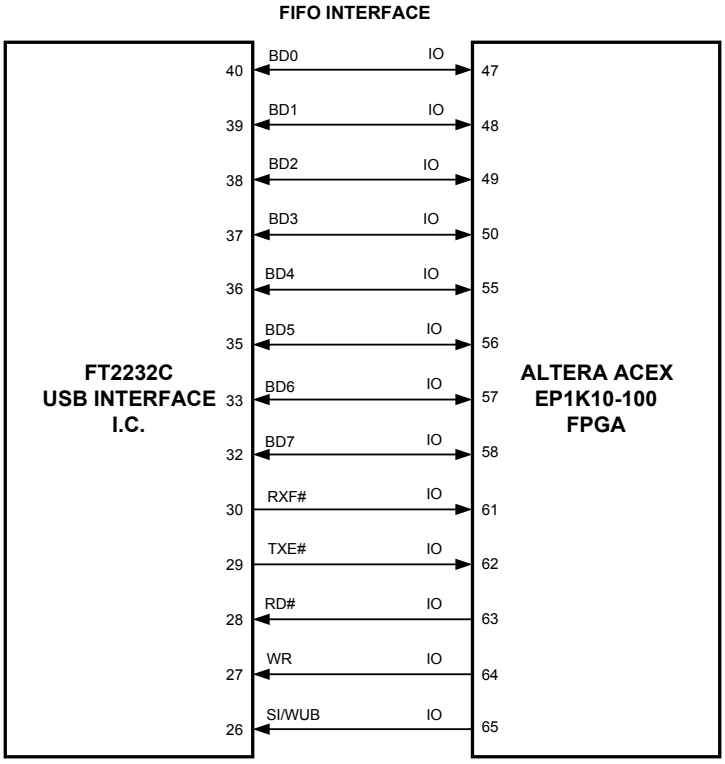


Figure 4 shows the bi-directional data transfer interface between the FT2232C and the EP1K10TC-100. It uses the FIFO mode of the FT2232C channel B to allow the FPGA to communicate with a PC over USB. Data is read / written between the devices over an 8 bit data bus BD0 .. BD7.

A typical application would send "commands" to the FPGA which would be interpreted by a state machine inside the FPGA. Some commands may return data from the FPGA to the application.

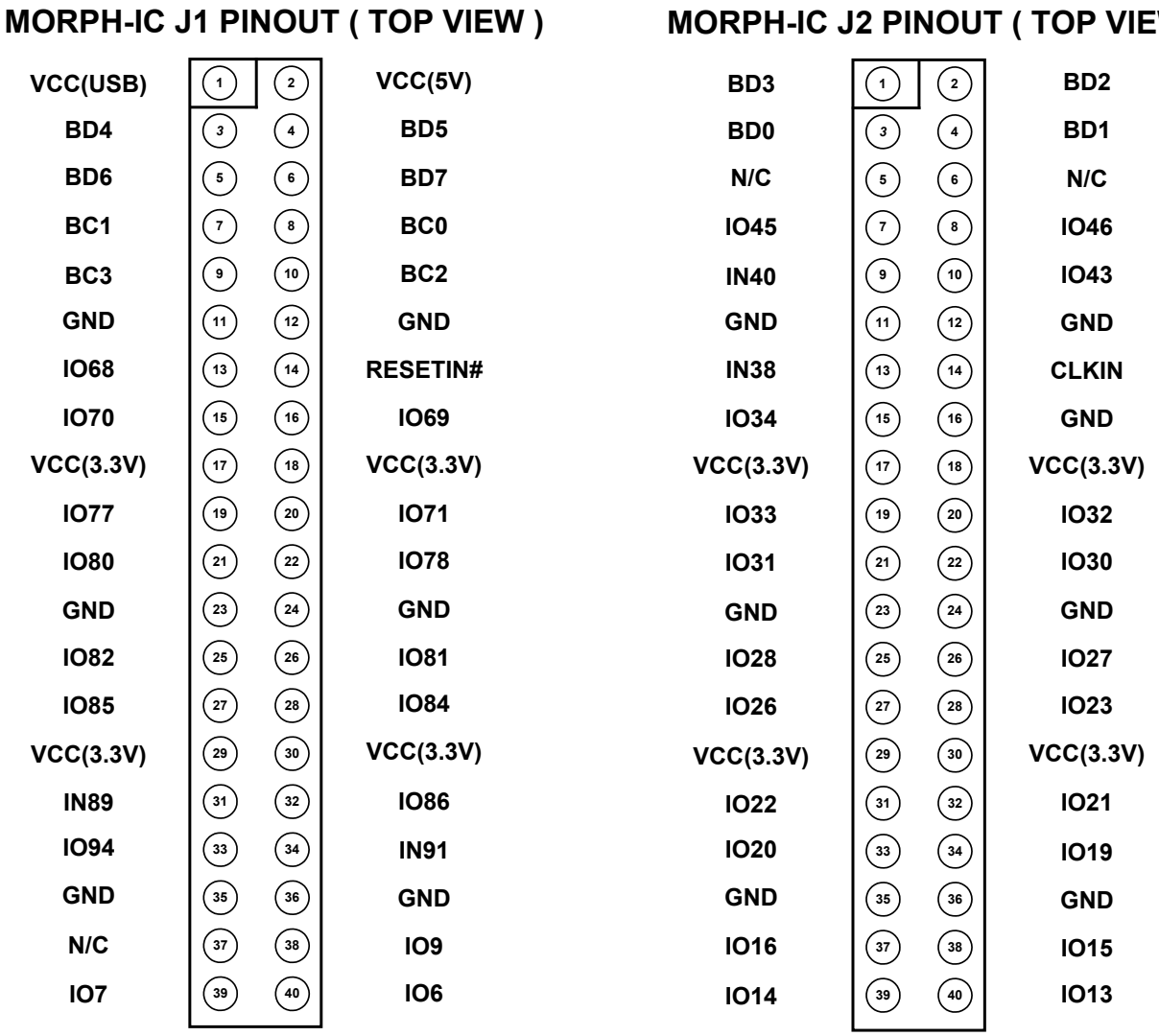
To send data to the application poll TXE# until it is low then place the data to be transmitted on BD0 .. BD7. Enable the bus, strobe the WR pin high then low then disable (tri-state) the data bus pins. Data is written into the FT2232C on the falling edge of WR.

To receive commands / data from the application, poll RXF# until it is low which means that there is data in the FT2232C to be read. Take RD# low to enable the data from the FT2232C on BD0 .. BD7. Strobe the data into the FPGA and make RD# high (its default state) to tri-state the bus.

For further details of the FT2232C FIFO mode including timings please consult the FT2232C data sheet. The example project on the CD illustrates such an application. Full VHDL source code of the project and the Delphi 5 application program are pubished on the CD and are a good starting point for developing MORPH-IC projects.

Note : The data bus and interface pins are all brought out on the J1 / J2 IO connectors. The data bus can be used to send / receive data to other external devices when the FT2232C interface is in its idle state.

FIGURE 5 - MORPH-IC IO CONNECTOR PINOUT



MORPH-IC has two dedicated 40 pin IO connectors labelled J1 and J2. These are industry standard 40 pin connectors (two rows of 20 pins) with square pins on a 0.1in pitch. The two connectors are spaced 1.3in apart (centre to centre). See Figure 6 for dimensional drawings.

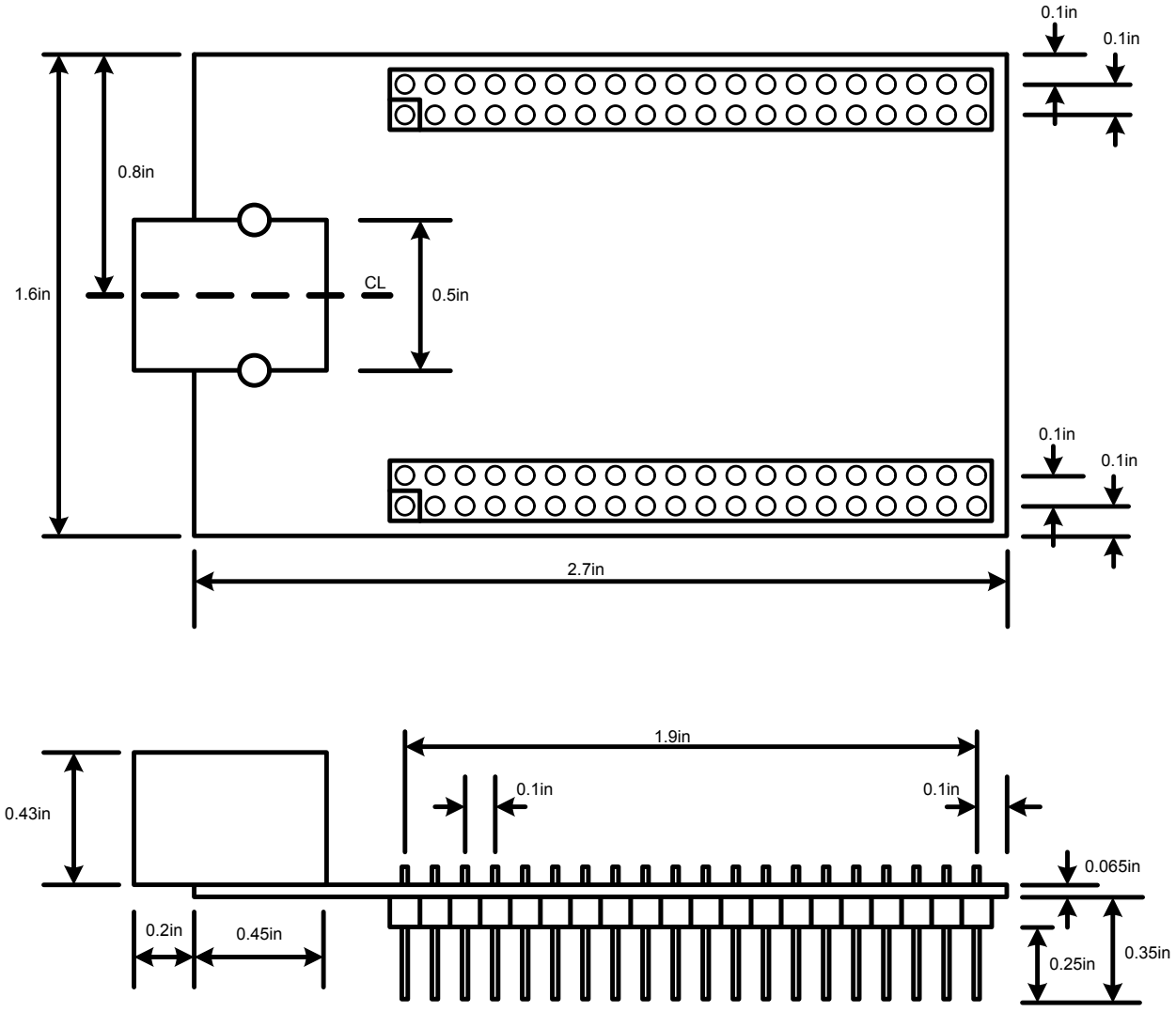
The pinout of the connectors as viewed from above is shown in Figure 5 and the pin descriptions are outlined in Table 1, overleaf.

TABLE 1 - MORPH-IC IO CONNECTOR PINOUT DESCRIPTION

MORPH-IC PIN DESCRIPTIONS		
Non-Shared IO Pins	IO6, IO7, IO9, IO13, IO14, IO15, IO16, IO19, IO20, IO21, IO22, IO23, IO26, IO27, IO28, IO30, IO31, IO32, IO33, IO34, IO43, IO45, IO46, IO68, IO69, IO70, IO71, IO77, IO78, IO80, IO81, IO82, IO84, IO85, IO86, IO94	These are IO pins from the EP1K10TC100. The naming convention is IOxx where xx equals the pin number of the FPGA. For example, IO70 is the IO pin on pin 70 of the device.
Shared IO Pins	BD0(IO47), BD1(IO48), BD2(IO49), BD3(IO50), BD4(IO55), BD5(IO56), BD6(IO57), BD7(IO58)	These are shared with the FT2232C data bus and can be used when the FT2232C data bus is in idle mode. See above notes on the FT2232C data transfer interface.
Dedicated Input Pins	IN38, IN40, IN89, IN91	These are input pins from the EP1K10TC100. The naming convention is INxx where xx equals the pin number of the FPGA. For example, IN40 is the input pin on pin 40 of the device. All inputs are pulled up to 3.3v by an on-board 10k resistor.
FT2232C Handshaking	BC0(RXF#), BC1(TXE#), BC2(RD#), BC3(WR)	These would not normally be connected to external logic, but are brought out for debug purposes i.e. for connecting a logic analyzer.
CLKIN	J2-14	Secondary input clock source from pin 39 of the EP1K10TC100.
RESETIN#	J1-14	Pulling this low resets the FT2232C I.C. and disconnects the device from the USB bus. Not normally required but available if needed. Pulled up to 5v by an internal 10k resistor.
VCC (USB) ***** Note 1***	J1-1	4.4V to 5.25V un-switched power from USB with J1 shorted. With J1 open, supply 5V power to this pin from an external power source.
VCC (5V) ***** Note 1***	J1-2	Power switched version of VCC (USB). Power to this pin is turned off during USB suspend.
VCC (3.3V) ***** Note 1***	J1-17, J1-18, J1-29, J1-31, J2-17, J2-18, J2-29, J2-31	3.3V (+/-10%) regulated power output. Power switched version of VCC (USB). Power to this pin is turned off during USB suspend.
GND	J1-11, J1-12, J1-23, J1-24, J1-35, J1-36, J2-11, J2-12, J2-23, J2-24, J2-35, J2-36	GND (0V) power rail.
N/C	J1-37, J2-5, J2-6	These pins are not connected to anything on this version. Do not use to ensure compatibility with future versions.

NOTE 1 - The maximum combined current that can be drawn from these power sources to power external circuitry is 250mA in total. If a 5V supply is required, use VCC (5V) instead of VCC (USB) to guarantee meeting USB current draw in USB suspend / sleep state (< 0.5mA).

FIGURE 6 - MORPH-IC DIMENSIONAL INFORMATION



Document Revision History

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Disclaimer

Contact Information

Future Technology Devices International Ltd.
373 Scotland Street,
Glasgow G5 8QB
United Kingdom.

Tel : +44 (0)141 429 2777
Fax : +44 (0)141 429 2758

E-Mail (Sales) : sales1@ftdichip.com
E-Mail (Support) : support1@ftdichip.com
FTDI Web Site URL : http://www.ftdichip.com
MORPH-IC Web Site URL : http://www.morph-ic.com

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